

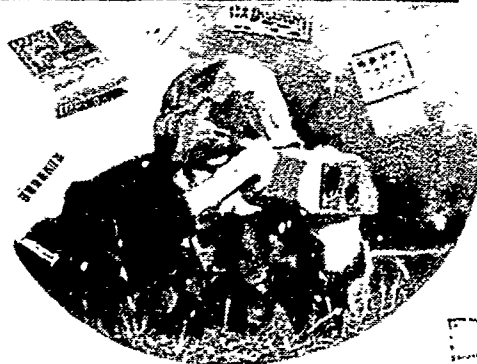
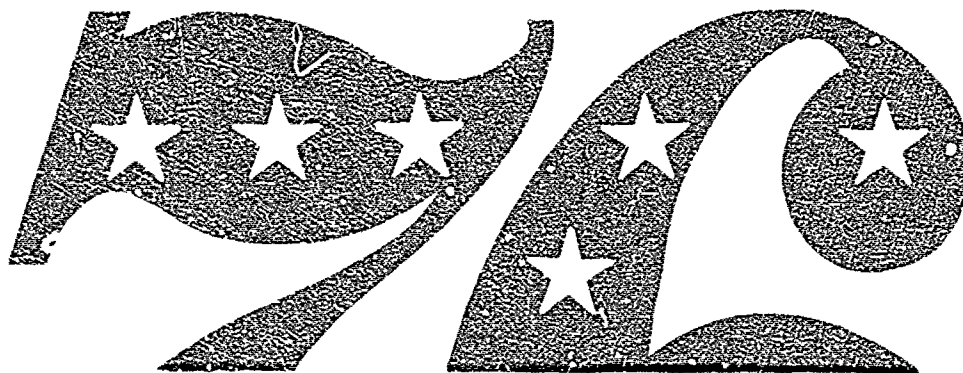
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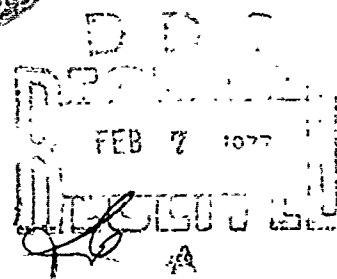
OF THE

HYBRID MICROCIRCUIT

SYMPOSIUM



JUNE 8 - 9 1976



U S ARMY ELECTRONICS COMMAND

FORT MONMOUTH, N.J.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Papers discuss application of hybrid microcircuits in Army communication and surveillance and other military and government equipment. Hybrid Microcircuit process and quality control documents and guides are described and qualification requirements for thick film networks and epoxy adhesives defined. Automation of a hybrid microcircuit line, non-wire bonding techniques, ruggedization and standard electronic modules are detailed.		

PROCEEDINGS
OF THE
ECON HYBRID MICROCIRCUIT SYMPOSIUM

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FOREWORD

These Proceedings contain papers presented at the ECOM Hybrid Microcircuit Symposium, Ft. Monmouth, New Jersey in June 1976. The papers include specific fabrication and manufacturing developments related to hybrid circuits in ECOM and other government equipment.

Hybrid microcircuits are now being planned into many Army equipment developments and are being utilized in some equipment nearing field status. For many of these items of equipment now under development, weight and volume requirements can only be met by utilizing the hybrid assembly technology. In particular, radio communication equipment, mortar and artillery locating radars, laser designator tracker system, pulse form restorer, hand-held laser range finder, telephone hand set, and remotely monitored battlefield sensor system can be cited which have taken advantage of hybrid microcircuits. Hybrid assembly technology is expected to continue to play a major role in the design and application of Army and other DOD electronic equipment during the next several decades. US Army Electronics Technology and Devices Laboratory is supporting various projects to insure the availability of reliable, low cost hybrid microcircuits.

The symposium program emphasized those areas of major concern to ECOM: the applications of hybrid microcircuits in Army communications and surveillance equipment, hybrid microcircuit process and quality controls, and automation. We were fortunate in having speakers from government and industry indicate the growth and progress in the development and application of hybrid microcircuits in military and other government equipment.

The Symposium attracted a large representation from the hybrid microcircuit community within the country. We were gratified by the many fine comments on the quality of the Symposium. The quality and success of the program is attributed to the efforts of the authors and speakers and to the effectiveness of the technical session chairmen.

On the behalf of the USAECOM management and ourselves, we thank all of the Symposium participants.

OWEN P. LAIDEN
Symposium Chairman

ISAAC H. PRATT
Technical Program Chairman

ECOM HYBRID MICROCIRCUIT SYMPOSIUM

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Hybrid Microcircuit Applications

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Hybrid Microcircuits for ECOM Equipment

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Hybrid Microcircuit Process and Quality Controls

Mr. John P. Farrell, Rome Air Development Center

Automated Assembly

Dr. Charles M. Tapp, Sandia Laboratories

Special Hybrid Design Considerations

Dr. W. Dean McKee, Naval Electronics Laboratory Center

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ECOM HYBRID MICROCIRCUIT DEVELOPMENT PROGRAM

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ABSTRACT

The US Army Electronics Command has, for several years, pursued a progressive program of research and development in the field of hybrid microelectronics. The current increased emphasis stems from our assessment that over 50% of all Army electronics equipment will require use of hybrid techniques to meet size and weight requirements brought about by unique Army needs for manpack and munitions delivered expendable applications.

In the past, DOD has spent many millions of dollars in developing military specifications for silicon monolithic devices and circuits with reasonable success. Unfortunately, the problems of assuring producibility, availability, and reliability for hybrid microcircuits are considerably more complex than for silicon integrated circuits. The problems arise both from the much larger number of materials and interfaces and from inherent limitations in the level of step stress testing that can be safely applied.

The ECOM program is designed both to improve the inherent level of hybrid reliability and to develop the knowledge of failure modes and mechanisms required to certify specific materials, parts and processes for Army applications. A longer range goal is to make a major impact on the cost of military electronics through the development of low cost modular packaging techniques tailored to specific applications and environments.

*Invited Speaker

MANAGERIAL ASPECTS OF ELECTRONIC EQUIPMENT RELIABILITY

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ABSTRACT

The four commanders responsible for meeting the needs of the United States operating forces are the Commander, US Army Materiel Development and Readiness Command (DARCOM), the Chief of Naval Material (CNM), the Commanders of the Air Force Logistics Command (AFLC) and the Air Force Systems Command (AFSC). These four commanders are often referred to as the Joint Logistics Commanders or JLC. This paper provides a report of the efforts of the JLC, Joint Technical Coordinating Group, Electronic Equipment Reliability, (JTTCG-EER) to alleviate problems relative to microcircuit standardization, acquisition, and technology applications. The prime emphasis of the Group's activities was concerned with the feasibility of taking effective management actions relative to the procurement of low-cost electronic equipment. Particular attention will be directed to the recommendations and follow-on actions relative to two areas investigated: hybrid microcircuits and beam lead sealed junction devices.

INTRODUCTION

The four commanders responsible for meeting the needs of the United States operating forces are the Commander, US Army Materiel Development and Readiness Command (DARCOM), the Chief of Naval Material (CNM), and the Commanders of the Air Force Logistics Command (AFLC) and the Air Force Systems Command (AFSC). These four commanders are often referred to as the Joint Logistics Commanders or JLC. This paper provides a report of the efforts of the JLC, Joint Technical Coordinating Group, Electronic Equipment Reliability (JTTCG-EER) to alleviate problems relative to microcircuit standardization, acquisition, and technology application. The prime emphasis of the Group's activities was concerned with the feasibility of taking effective management actions relative to the procurement of low-cost electronic equipment. This JLC Group spearheaded the current thrust by the services in the area of hybrid microcircuits and related areas.

BACKGROUND

The JTTCG-EER was formed in December 1973 and completed the bulk of its activity in August 1975. It was composed of selected members of the four commands, represented by the JLC. The mission of the Group was to coordinate the implementation of the following actions:

- (1) Expedite the preparation of a list of standard parts for microcircuits.
- (2) Expedite the preparation of microcircuit specification to eliminate or replace contractor nonstandard parts specifications and drawings.
- (3) Expand the use of Military Parts Control Advisory Group (MPCAG) for technical support in parts selection and control of nonstandard parts.
- (4) Develop a procedure and submit forecasted microcircuit requirements to the Defense Electronics Supply Center (DESC) for preparation of a consolidated forecast to industry.
- (5) Use existing captive/controlled lines efficiently by providing visibility and usage of their products via the use of standard parts lists (MIL-STD-1562)
- (6) Expand efforts to develop a Hybrid Microcircuit Technology Base.
- (7) Initiate efforts to make beam lead sealed junction devices more readily available during the FY 75-80 time period.

The latter two areas should be of immediate and direct interest to the participants of this symposium. Further information will be provided in other papers in the proceedings covering the subject areas.

MICROCIRCUIT STANDARDIZATION

The two areas covering the preparation of a list of standard parts and the preparation of Military Specifications for Microcircuits will be combined since they are both closely related. When the Group began its deliberations, there was a prohibition by DOD Directive against issuing a List of Standard Parts for Microcircuits. The Group concluded that this DOD policy should be rescinded. Through its efforts, the policy was rescinded by a 30 Aug 74 letter from the Secretaries of the Office of Assistant Secretary of Defense (Installation and Logistics) and Director of Defense Research and Engineering. Subsequently, MIL-STD-1562 was prepared and dated 5 Nov 74. This list, now used by military contractors, will reduce proliferation of nonstandard parts.

MILITARY PARTS CONTROL

Related to the previously discussed standard effort is the control of nonstandard parts proliferation. When the JLC Group began its deliberations, the use of MPCAG was limited to the AFSC. As a result of the Group's activity, the Army concluded a total MPCAG agreement in Dec 75, and the Navy is expected to conclude its total agreement imminently, if it hasn't already been done. A draft DOD Instruction was issued 1 Mar 76. pertaining to the implementation of an integrated DOD Parts Control System. The issuance of this instruction is based, in part, on the visibility given to this problem by the JLC.

For FY-73, -74, and -75, MPCAG recommended the replacement with standard parts of 19,400 nonstandard parts out of 43,000 evaluations. The reduction of contractor prepared drawings, elimination of part testing because of availability of qualified products list, and elimination of logistic support for these nonstandard parts has resulted in a \$162 million cost avoidance to the Government.

MICROCIRCUIT FORECASTING

The actions involving the preparation of a list of standard parts, the expanded use of MPCAG, and the preparation of needed military specifications culminates in a forecast requirement to industry through DESC. Forecasting microcircuit requirements appears to be advantageous to both military agencies and the semiconductor industry, and the semiconductor industry can be expected to improve the availability of microelectronic devices. However, before considering full service participation in any forecasting activity, essential information in a number of critical areas must be obtained. It was concluded that a pilot forecast is a logical method, within the resources available, for developing this needed information.

A forecast plan was developed and will be implemented on a one-time basis for the following purposes:

- (1) To determine if a meaningful forecast can be provided;
- (2) To establish to resources (manpower and dollars) that a forecasting activity will require;
- (3) To establish to time interval for providing forecast outputs, and
- (4) To solicit industry's (users and vendors) comments on a pilot forecast particularly on the impact an expanded forecast activity would have on a microcircuit availability.

EXPANDED USE OF CAPTIVE/CONTROLLED LINES

The classical application of a captive/controlled line concept for the production of microcircuits or other electronic parts has been in support of specified weapons/systems programs. In this study, captive/controlled line products were evaluated on their overall potentials in support of defense electronics. Captive/controlled lines were considered in the fabrication of special technology, low usage, small quantity procurement, and obsolete microcircuit devices. The study concluded that it was not cost-effective to set up captive/controlled lines for fabricating these device types. Additionally, it was concluded that captive/controlled lines be used as a last resort after all other viable alternatives have been exhausted.

HYBRID MICROCIRCUIT TECHNOLOGY BASE

Hybrid microcircuits are important to the military, since the requirements of many critical equipments and systems currently under development can only be satisfied if such circuits are incorporated. The problem with these devices has been that because of inadequate process control and insufficient device level testing, too often it is found that reliability problems exist only after these devices are installed in equipment and systems.

In order to overcome these problems, the services have taken a multifaceted approach. The first approach required changing MIL-M-38510 and MIL-STD-883, the general specification and test methods for microcircuits. These documents are being modified to more accurately reflect problems e.g. associated with hybrid microcircuits. Under consideration are changes to Method 5008, MIL-STD-883, Package Qualification Procedure.

The second approach involved the development of in-process controls and processing standards for hybrids, e.g. currently under consideration are criteria for certifying a thick film processing line as well as a specification for the selection and use of organic adhesives for hybrid microcircuits.

Finally, the Hybrid Microcircuit Technology Base is being improved through an approximately 50% increase in the service programs.

Presented here is an overview of the approach being taken by the services to improve the reliability of hybrid microcircuits. Other papers in the proceedings provide a greater amount of detail.

BEAM LEAD SEALED JUNCTION DEVICES

Another technical area directly related to the problem of hybrid microcircuits is that of Beam Lead Sealed Junction Technology. Beam lead devices are very attractive for military use in hybrids, because they offer the possibility of high packing density and high reliability. They also offer the possibility of simplified hybrid assembly production processing and increased yield.

The major problem with such devices is that only a limited number are available for general application in military and commercial equipment and systems. To alleviate this problem for the military, it was decided that a Multiyear Production Based Program sponsored by one of the services was necessary to insure the potential of device availability. Accordingly, the US Army Electronics Command, (ECOM), awarded a two-year \$1.4 million contract to Motorola Semiconductor, Phoenix, AZ in May 75. Under this program, manufacturing requirements are being developed for three diodes, eleven transistors, and twenty-one microcircuits, all of which are beam lead sealed junction devices. The object of this program is to improve

overall yield to 20% for the transistors and diodes, 10% for the simple digital microcircuits, and 5% for a 60 gate digital array. More information is provided in another paper in the proceedings.

Additionally, ECOM awarded a one-year R&D Contract for \$92,693 to Hughes Aircraft Co. in Jul 75. The objectives of this program are to verify the thermal models for these devices and to prove by accelerated testing, that the ten times reliability improvement expected from beam lead sealed devices has been achieved.

CONCLUSIONS

An overview of the managerial aspects being taken jointly by the services in improving electronic equipment reliability has been provided. The progress presented in this paper resulted from the efforts of the JTCG-EER members of the US Army Materiel Development and Readiness Command, Naval Material Command, Air Force Logistics Command, Air Force Systems Command and the Defense Electronics Supply Center. Members of this group operated diligently and effectively for approximately two years between 1973-1975.

The efforts of the joint group have not ended, but have been re-directed in a similar exercise aimed at end item equipment and systems, rather than electronic parts.

HYBRID MICROCIRCUIT APPLICATIONS FOR THE
ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
NUCLEAR WEAPON PROGRAM

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ABSTRACT

Sandia Laboratories has used hybrid microcircuits in nuclear weapon applications since 1970. The technology selected by Sandia for development was the gold thin film system compatible with the beam lead devices. Initially, all interconnections were thermocompression bonds. Further applications have required addition to this base-line technology; a thicker gold for rf applications, solder, back-side metallization, conductive vias, and at the present time future applications are motivating the study of thick film multilayered interconnection boards, leadless hermetic packages and aluminum-to-gold interconnection systems.

Sandia Laboratories is a prime contractor to the Energy Research and Development Administration and is responsible for the design, development, and production assurance of nonnuclear components and systems used in nuclear weapons. The nuclear systems are designed either by Los Alamos Scientific Lab or the Lawrence Livermore Laboratory. Sandia is managed for ERDA by Western Electric. In addition to these three design laboratories ERDA owns several captive production facilities which are called integrated contractors. One of these integrated contractors is responsible for most of the electronic subsystems for nuclear weapons programs and is operated by the Bendix Corporation in Kansas City. Bendix, Kansas City, is our production agency for hybrid microcircuits.

This paper will review the hybrid microcircuit applications in the nuclear program to date. A brief summary will be given of the observed reliability and performance and then the present development activities at Sandia in hybrid microcircuit technology for near term applications will be described.

Hybrid microcircuits were first used in nuclear weapons in the Mk-3 Poseidon system. The radar in this system required hybrid microcircuits in order to achieve its function in the allocated volume. There were many problems encountered in the procurement of these hybrids. Necessary changes late in the development and early in the production program required many months between when the problem was identified and when the cure appeared in production. To solve the technology problems encountered, the design lab had to apply significant resources similar in quantity to the amount necessary to develop the technology independently. These problems in procurement led to three decisions in August of 1970 that have guided Sandia's microelectronic effort from that time to the present.

1. To develop internally a single hybrid technology,
2. To develop a technology compatible with beam leaded devices,
3. To develop a single AEC (ERDA) hybrid production source.

The first application of this technology, the Multiple Code Coded Switch (MCCS) illustrates the specific technologies developed and transferred to the production agency. The MCCS is a component used in many nuclear weapons to provide controlled access to these weapons. The switch must be closed in order for the weapon to function and in order to close the switch an appropriate electronic signal must be provided.

Figure 1 illustrates the technology used in the MCCS. This technology includes a tantalum nitride thin film resistor system with thermal stabilization to $\pm 20\%$. Individual laser trimming of the resistors was developed for resistors requiring a 0.5% tolerancing. A 3-micron gold conductor system is evaporated on top of the tantalum nitride system with a chromium intermediary layer. All bonding in the MCCS is thermocompression and includes lead frame bonding, and fine wire bonding for crossovers and for capacitor attachment. Beam lead devices are used wherever practical.

The second application of this technology is the Mk-4 system for the Trident program. Again, the fuzing radar will be hybridized. The additions to the technology required for this system are: thicker gold for reasonable conductivity at high frequency, backside metallization for ground and power planes, conductive vias to the backside metallization, and solder interconnects for low inductance leads.

These technologies have completed development and have been transferred to the production agency where they are being evaluated in the process capability laboratory. A critical element of achieving high reliability microelectronics is the careful transfer to the production agency of information on the critical processes, materials, tests, etc.

Figure 2 illustrates how this technology is transferred between Sandia Labs and Bendix, Kansas City. While the technology is being developed at Sandia, full time residents from the production agency assist in this development insuring the practicality of what is being developed and providing at a later time knowledgeable personnel at the production agency of why the various choices and controls were selected. The technology is formally transferred to the production agency through written specifications. The informal technical exchange is at least equally important. After the technology is transferred to the production agency, it is exercised in a special production facility called the Process Capability Laboratory. This facility is operated like the production floor but without production delivery schedules so that new technology elements can be fully exercised in a production environment. If the technology passes this test, it can then be introduced with minimum risk to the production floor. Many in-process controls are also required to insure continuing high reliability product. Figure 3 illustrates the in-process

controls presently utilized at Bendix, Kansas City. At each test point manufacturing control charts are maintained to indicate data trends. Pictures of the manufacturing control charts are forwarded to the design agency monthly. Details of this technology development are available in the following references:

1. "A Review of Hybrid Microelectronics," C. M. Tapp and T. A. Wiley, SLA-73-1063, dated June 1974.
2. "A Compilation of Specifications Describing Hybrid Microcircuit Technology," C. M. Tapp and D. J. Sharp, SLA-74-0300, dated June 1974.
3. "The Hybrid Microcircuit Design Guide," SLA 74-0333, dated June 1974.
4. "Bibliography, Sandia Laboratories Hybrid Microcircuits and Related Thin Film Technology (Revised)," J.A. Oswalt, SAND75-0485, dated December 1975.

These references may be obtained in microfiche or hard copy from:

National Technical Information Service
U. S. Department of Commerce
5285 Port Royal Rd. P. O. Box 1553
Springfield, VA 22151

At the present time three additional elements are being added to our hybrid microcircuit technology in order to have the ability to use MOS devices extensively. These are:

1. the development of hermetic packages,
2. the development of an aluminum-to-gold interconnections system,
3. the development of a multilayered thick film interconnection board.

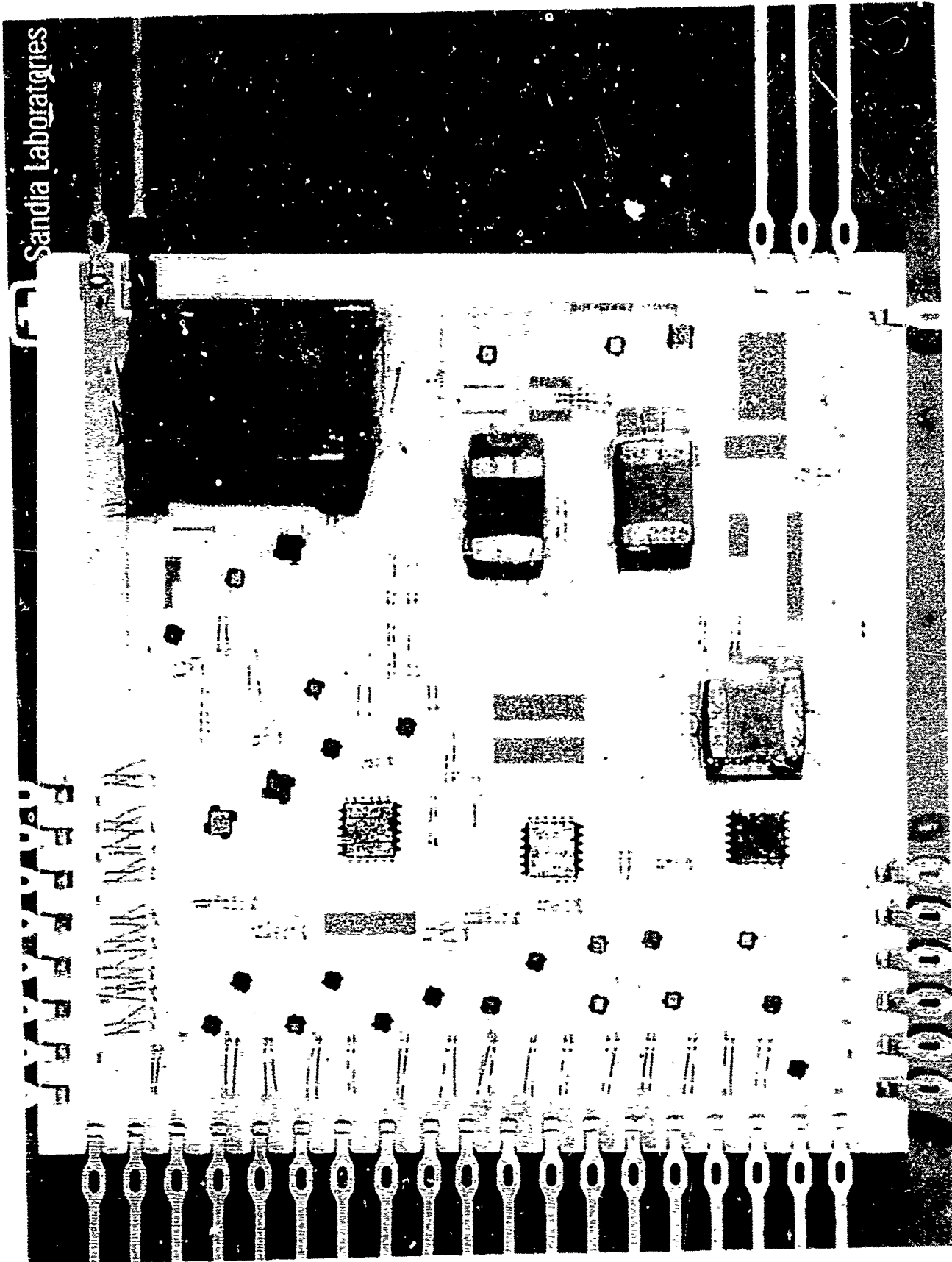
Systems currently under development will require the use of LSI MOS devices. Since these devices are very sensitive to surface contaminants, they will be packaged in individual hermetic containers. At the present time, our baseline approach is to use the leadless hermetic package which is shown in Figure 4. These can be utilized on the previously illustrated hybrid microcircuits or may be interconnected on a multilayered thick film interconnection board. Since the terminal pads of the available MOS devices are aluminum, careful attention is being paid to the aluminum-gold interface which has created problems in the past.

Is this approach to high rel microelectronics working? The data from the field on the Mk-3 Radar as evaluated in a joint ERDA/Navy Quality Program states, "The reentry vehicles... meet fleet operational requirements." There are hundreds of Multiple Code Coded Switches presently in the field being regularly exercised and there have been no field failures. In summary, hybrid microcircuits have allowed Sandia designers to achieve high rel electrical functions in minimum volume and configurations.

Figure Captions

- Figure 1. A typical 1" x 1" hybrid microcircuit illustrating the thin gold film technology
- Figure 2. Schematic representation of technology flow from the design agency into production
- Figure 3. Schematic representation of product flow from various substrate to finished product.
- Figure 4. Illustration of the leadless hermetic package compared to a comparable dual in-line package.

Sandia Laboratories



TECHNOLOGY DEVELOPMENT

BENDIX RESIDENTS

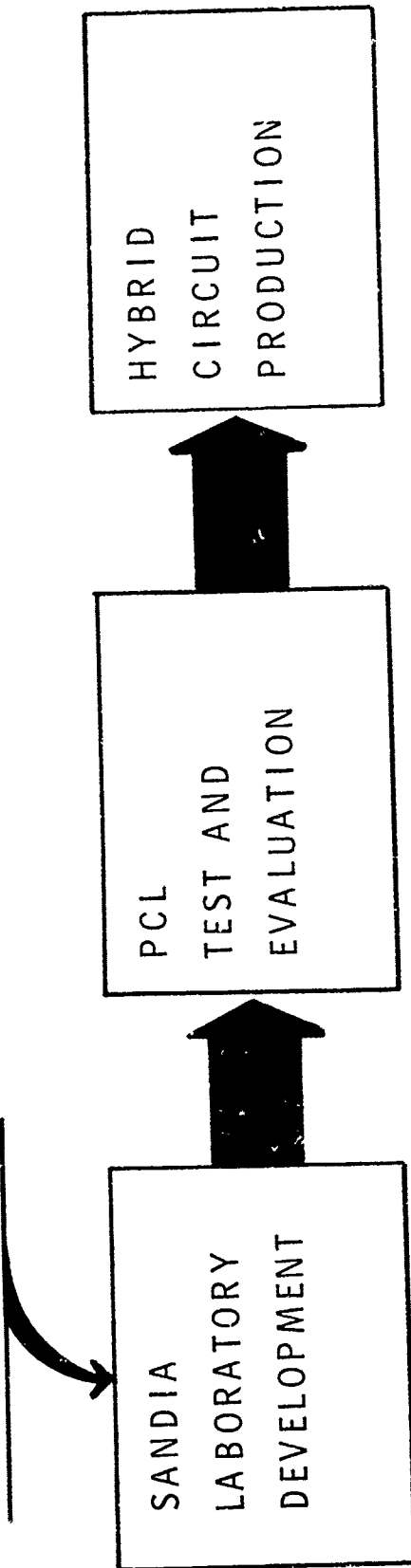


Figure 2

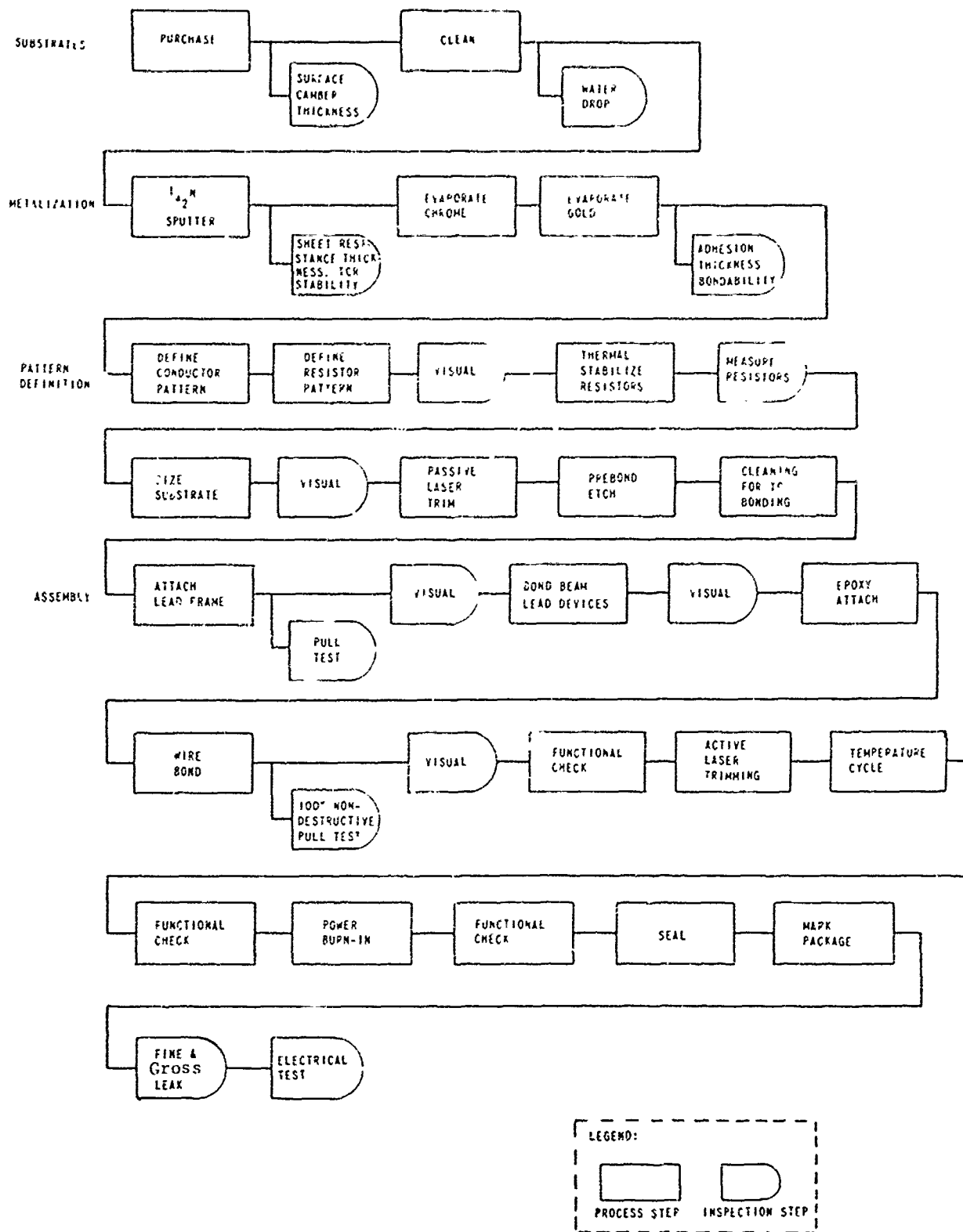
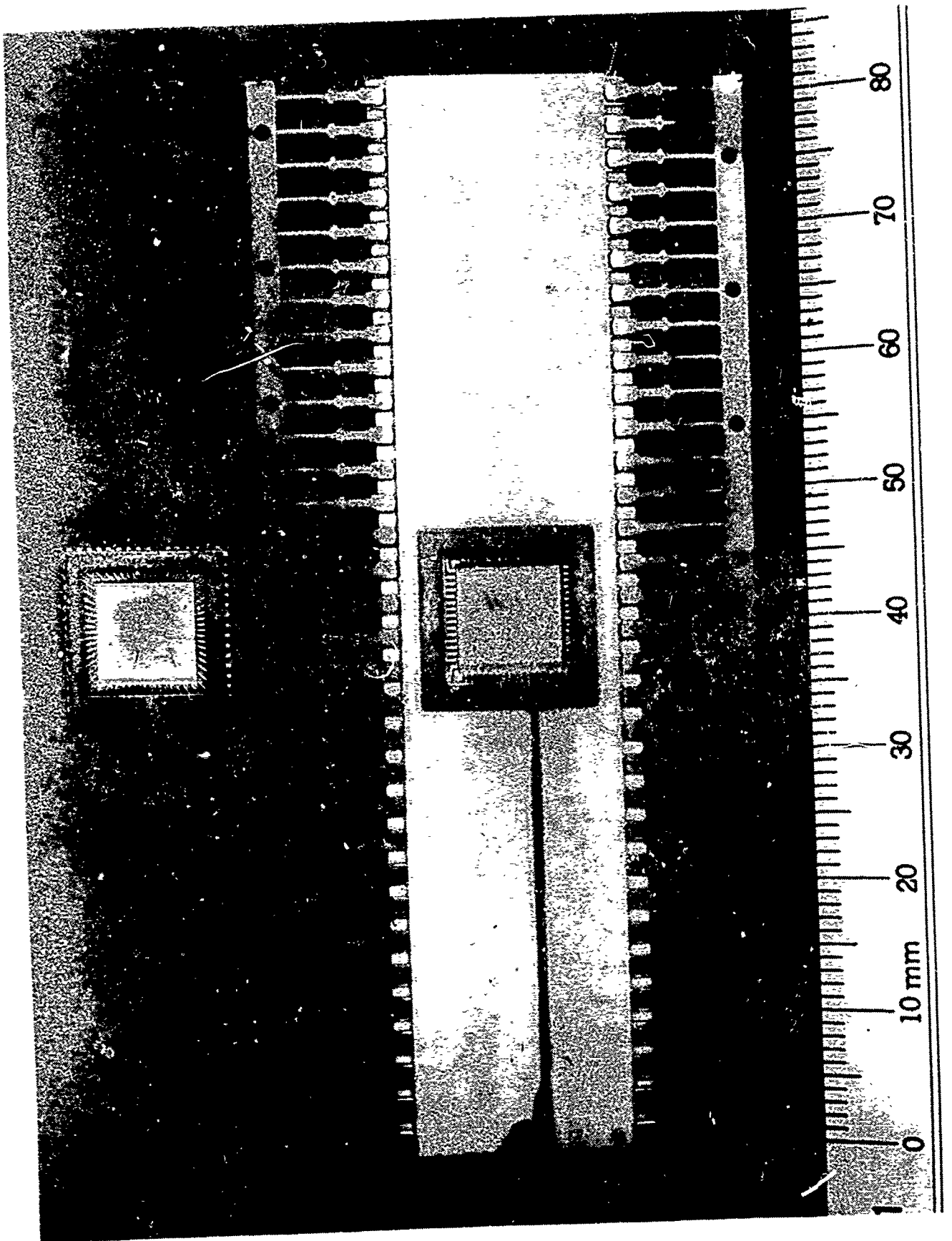


Figure 3



NAVY HYBRID MICROCIRCUIT APPLICATIONS

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ABSTRACT

The Navy has made significant application of custom hybrid microcircuits since early in the last decade. These range from a single hybrid microcircuit module developed to facilitate retrofitting a function into an in-service equipment, to use of hundreds of mini-chip microcircuits which appear in several subsystems of a sophisticated modern aircraft.

An experimental retrofit example is the calibrated noise source microcircuit for the SSQ-578 sonobuoy. A much more sophisticated retrofit is that of the Mark 46 torpedo electronics.

An early airborne equipment use of hybrid microcircuits was the Integrated Helicopter Attack System (IHAS). Although difficult and complex to make at the time, these early multi-chip microcircuits are dwarfed, from the functional electronic standpoint, by those of several systems using hybrid microcircuits in the Navy F-14 fighter airplane.

Attack missiles provide examples of hybrid microcircuits which appear both in conventional package geometries and as special shapes, dictated by missile geometry and requirements for maximum saving of weight and space.

The examples given are only a representative sample of the Navy's large, diverse, and growing applications of hybrid microelectronics.

*Invited Speaker.

TRADE-OFF CONSIDERATIONS IN CONTRASTING HYBRID APPLICATIONS

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ABSTRACT

This paper examines the application of hybrids to the electronic hardware associated with two quite different ECOM programs. One program involves hand-held field equipment; the other, rack-mounted test equipment. The initial motivating factors for using hybrids will be reviewed against some of the resulting experience. Cost considerations are emphasized over technical considerations in the review of the rack-mounted equipment. Between the two programs, a total of six different types of thick-film hybrids have been designed on a custom basis over a period of about two years. Technical highlights are given relative to the various assembly and packaging methods used in the design of these circuits.

INTRODUCTION

As the manufacturing technology for economically producing hybrid microcircuits continues to mature, more and more applications are being found where they can be profitably put to use. This paper examines two very different applications of hybrids in Army electronic equipment, reviewing technical and cost trade-off considerations for each of the applications.

The design of the AN/GVS-5 Hand-Held Laser Range Finder, motivated by demanding requirements on size, weight and performance as well as for low unit production cost, produced three unusual custom hybrids tailored to the application. Technical highlights on the hybrids are presented in support of their use.

The AN/USM-410 Automatic Test System features a Programmable Interface Unit that greatly reduces the cost of test design and test programming and the proliferation of test adapters. The size and cost of the more sophisticated test system interface is held to manageable levels by the use of three different types of hybrids, each of which is used hundreds of times per deliverable system. The paper summarizes a cost study that establishes the cost-effective use of hybrids instead of discrete parts. Although a superficial look at the application might indicate that hybrids should not be used, the cost analysis, comparing costs at a total system-hardware level, clearly reveals the appropriateness of the hybrid microcircuit approach.

HAND-HELD LASER RANGE FINDER

The AN/GVS-5 Hand-Held Laser Range Finder (Figures 1 and 2) is typical of that class of equipment where miniaturization through the use of hybrid microcircuits is the logical way to meet demanding size and weight requirements without compromising equally demanding performance requirements. Also, this hardware, with a production potential of over 7,500 units, can take advantage of the potential lower cost of hybrids produced in volume. The AN/GVS-5 has a complement of three hybrid microcircuits:

- 1) Detector-Preamplifier
- 2) Video Amplifier
- 3) Range Counter and Display Hybrid

Detector-Preamplifier Hybrid

A close-up view of the Detector-Preamplifier (Figure 3) reveals a rather conventional TO-8 type package except for the window in the cover. It is through this window that the reflected energy from a laser-illuminated target ultimately gets focused on the surface of a silicon avalanche photo diode inside the package. In addition to the photo diode and its load resistor, this hybrid package includes a wide-band, unity-gain transistor amplifier whose performance has been enhanced by the fact that stray capacitance can be kept smaller here than in a conventional discrete-circuit arrangement by at least a factor of two.

Video Amplifier Hybrid

The output of the Detector-Preamplifier drives the Video Amplifier Hybrid shown in Figure 4. The ceramic substrate used here is 2 1/4 inches long by 1 1/4 inches wide. The bare semiconductor chips and their wire-bonded connections to the substrate are all contained inside the hermetically-sealed, rectangular cover that is visible in the center of the photograph. Larger parts, like the tantalum chip capacitors and most of the thick-film resistors are located outside of the custom-sealed area. This hybrid contains a high-gain, wide-band amplifier used to process the narrow (about 5 nanosecond) input pulse. There are special circuit features worth highlighting. One feature is a time-programmed gain which maintains low gain for close targets and haze conditions. Another feature is a circuit that is part of an AGC loop involving the power supply (not hybridized) and the voltage bias to the avalanche diode in the Detector-Preamplifier Hybrid. In order to optimize certain critical performance characteristics, functional trimming of some of the thick-film resistors is performed after sealing. Both voltage gain and offset conditions are adjusted dynamically for significant performance improvement.

Range Counter and Display Hybrid

The operation of the Hand-Held Laser Range Finder depends basically upon determining the time interval between a START pulse associated with the laser

action and a STOP pulse developed from the reflection of the laser light off a distant object. The digital processing of the START and STOP signals, as well as other operator-controlled functions, is handled by the Range Counter and Display Hybrid shown in detail by Figure 5. This large, 2.25 inches x 1.725 inch substrate contains two round kovar covers in the center of the substrate which hermetically protect semiconductor chips and wire bonds. Under the far cover are two bi-polar integrated circuits, a diode, a transistor and a custom LSI chip. Under the nearer cover is another custom LSI chip. Most of the digital-circuit action is associated with the LSI devices, each of which uses COS/MOS silicon-on-sapphire technology.

After the active chip devices are sealed, functional trimming of six different resistors permits precise timing adjustments to be made on the ranging functions. Note that large parts such as chip capacitors and the crystal visible in Figure 5 are located outside of the custom-sealed region. At the rear of the photograph is another thick-film hybrid, in this case, a simple display subassembly that is populated by two light-emitting diodes and a numeric indicator. Aided by the precise location of the thick-film patterns on the parent substrate, the display subassembly is accurately aligned in the optical path of the range-finder system.

Motivation for Use of Hybrids in the AN/GVS-5

The AN/GVS-5 hybrids were selected after extensive trade-offs with other circuit types. The basic considerations were production cost, size and weight. Although it certainly would have been possible to pack discrete parts and module boards into an operable electronic configuration, the hybrid approach resulted in performance improvements and much easier integration of the end-item subassemblies. The hybrid realization of the product made it possible to achieve a weight less than the specified 5-pound limit for the Hand-Held Laser Range Finder by almost 10%. In this case, although the primary reason for selecting hybrids was because of smaller size and lower weight, the choice of hybrids also resulted in a lower production cost.

AN/USM-410 AUTOMATIC TEST SYSTEM

The AN/USM-410, shown in Figure 6, is a third-generation, computer-controlled automatic test system. Typical of such equipment is the packaging arrangement of consoles and rack-mounted chassis suitable for depot, van and shelter installations. Size and weight are not generally driving forces to the design. Hybrid microcircuits found a very important place in this rack-mounted equipment, providing performance improvements. The use of hybrids was found to be cost effective, a result primarily from the size reductions in the attendant equipment. There were fewer circuit boards, less chassis, a smaller rack, less labor in putting things together and getting them working - all acting to offset the higher initial cost of completed hybrids compared with the piece parts they replace. The reasons for using hybrids in the test system in the first place are presented in the remaining part of this paper along with the results of some cost comparisons of the discrete-part circuits and the substituted hybrid microcircuits.

Programmable Interface Unit

One of the major problems that has plagued automatic test systems for years has been the interface between the tester and the units-under-test (UUT). Whenever a test system serves a variety of different UUT's, there has been, in the past, a proliferation of special adapter cables and test-adapter boxes. Such interface hardware makes the unique interconnections to the UUT and augments the test system with special loads and interface circuits. The procurement, logistics support and change control of such adapters for fielded UUT's becomes very cumbersome and a major expense to the user. RCA has introduced a Programmable Interface Unit in the AN/USM-410 Automatic Test System as a viable solution to the interface problem. The Programmable Interface Unit shown in Figure 7 provides a complement of 128 identical Universal Test Point circuits, each of which can, under program control, be connected to a UUT interface line for measurement purposes or for excitation from a selected DC, AC or pulse stimulus. The number of Universal Test Points that can be provided in a given system is flexible because of the modular construction of the unit. Figure 8 shows one of the sixty-four Dual Universal Test Point boards of the Programmable Interface Unit. The individual hybrid microcircuits used on this board are separately highlighted in the photograph around the periphery of the board.

Even though the Programmable Interface Unit simplifies interface adapters and eases the test programming and test program maintenance, the unit itself is clearly complex and represents an increase in the cost to the test system hardware. Thus the designers have been motivated to drive these costs down. Furthermore, the unit presented potential technical problems because of possible large physical size. Conventional discrete-circuit packaging methods would lead to a physically large unit that would be subject to system noise problems and performance degradation from line capacitance and resistance. The designers were motivated, therefore, to use hybrids to reduce the physical size of the unit to manageable levels. Cost/performance trade-off studies revealed the desirability of converting three circuits of the universal test point to hybrid package configurations. They are:

- 1) 8-Channel, Latching Relay Driver
- 2) Digital Stimulus Buffer
- 3) Measurements Buffer

The studies showed that the desired miniaturization of the hardware by using hybrid microcircuits could be realized without cost penalties, even in relatively low production quantities.

8-Channel, Latching Relay Driver Hybrid

The Relay Driver circuit was the first circuit to be partitioned for hybridizing because it could be used not only on a universal test point board, but also on other boards of the main test system. A close-up view of the 8-Channel, Latching Relay Driver Hybrid is shown in Figure 9. A relatively uncomplicated hybrid, the circuit involves a dual, quad-latch integrated circuit, eight chip transistors and eight identical resistors. The thick-film substrate is solder mounted with gold-germanium in a 22-lead flat pack. The

package is hermetically sealed with gold-tin solder. Substrates are printed on a multiple-image plate, sixteen circuits at a time. The circuit itself provides eight latched outputs, each of which can sink up to 100 milliamperes of load current to ground.

Digital Stimulus Buffer Hybrid

The Digital Stimulus Buffer, shown in detail in Figure 10, is made up of 10-beam-lead diodes, 12 beam-lead transistors, 2 chip capacitors and 18 thick-film resistors. The package has leads for edge-type connection to a P.C. board. The conformally-coated circuit is provided with a heat sink to permit power dissipation of 2 watts under maximum specified load conditions. In the test system, the Digital Stimulus Buffer is used to drive a Unit-Under-Test with signals whose HIGH and LOW voltage levels are programmable over a range of ± 20 volts. The pulse width and pulse repetition rate are also controllable from programmable switching signals.

Measurements Buffer Hybrid

The Measurements Buffer, shown in Figure 11, is a high-performance, unity-gain Video Amplifier used from D.C. to 10 MHz as a buffer between input signals from a Unit-Under-Test and the measurements electronics of the test system. The hybrid packaging uses chip-and-wire construction. Chips are protected by encapsulation from the relatively benign environment seen by this class of equipment. In the manufacture of this hybrid, advantage is taken of functional trimming techniques to optimize the gain and frequency response of the circuit.

COST COMPARISONS - HYBRIDS vs DISCRETES

The AN/USM-410 Automatic Test System has provided an interesting opportunity to make cost comparisons between hardware produced using conventional discrete parts and hardware produced using equivalent hybrid microcircuit packages. Actual equipment has been built both ways so that historical data and factory cost estimates were available to make such comparisons on a total-build basis.

The case for using hybrids has often been lost in the past by a superficial comparison of so-called parts costs. Figure 12 dramatizes how such comparisons of "parts" costs can be misleading. Here the cost of each AN/USM-410 hybrid microcircuit, treated as a purchased part, is compared with the cost of the discrete piece-parts it replaces. The costs shown here, and all other places in this paper, have been adjusted to reflect a factory sell level appropriate to deliverable equipment. Note that in the simple comparison of parts costs, these particular hybrids run from 2 times to 3 times more expensive than the piece-part equivalents.

Baselines for Cost Comparisons

Clearly, the cost study must penetrate beyond the basic costs of parts. The hybrid, indeed, is more expensive than the piece parts it replaces simply because of labor content wherein a significant amount of value has been added already to produce a completely functioning circuit. Permitting objective cost comparisons, the AN/USM-410 provides two good baseline configurations of printed circuit boards, one associated exclusively with the Relay Driver circuit function and the other associated primarily with the Digital Stimulus Buffer and Measurements Buffer circuits. Figure 13 is a photograph showing the evolution of a combination of four 8-channel, latching relay driver circuits first configured with discrete parts (integrated monolithic circuits) spread out on four identical Relay Driver Boards and one Storage Board. The hybrid packaging allowed these five boards to be replaced functionally by one board with obvious cost savings in board fabrication, assembly and test. Similarly, the Automatic Test System has provided an opportunity to get a thorough comparison of costs for the two versions of the Digital Stimulus Buffer and the Measurements Buffer. Figure 14 shows an earlier circuit board configuration of a single universal test point for the Programmable Interface Unit. Unlike the Dual Universal Test Point Board shown in Figure 8, this board used discrete parts to implement the functions of the two buffer circuits. But again, the two different arrangements provide good sources for cost comparisons.

Cost Factors

The basic elements of recurring costs that must be reviewed in order to compare objectively the cost of each circuit function in discrete form and in hybrid form are:

- Electrical Material (Parts)
- Printed Circuit Board Fabrication
- Assembly Labor of P.C. Board
- Test Labor of P.C. Board
- Labor and Material associated with Next Level of Assembly
- Manufacturing Engineering and Support Labor

The above elements of cost must be divided and allocated in a rational way to each of the specific circuit functions being compared. The costs to be addressed here are recurring costs. There are, of course, non-recurring costs that can be considered but will not be included in any detail in this paper. It can be broadly stated that most of the differences in non-recurring costs for the subject hybrids and their discrete-part equivalents were associated with the design layouts. The hybrid microcircuit layouts were indeed more difficult to perform and ranged in cost between \$1500 and \$4000 a piece.

Results of Comparison

Table 1 summarizes each element of cost allocated to the hybrid version and to the discrete-part version of each of the three circuits. The cost numbers (at factory sell) are rounded off to the nearest dollar. Any cost

less than 50 cents has been dropped. The table is broken up into three groups of two columns, one group for each of the circuit functions that have been converted from discrete-parts packaging to hybrid packaging. Starting with the cost of the basic parts and treating the hybrid itself as a finished part, costs are compared for each major element of cost.

After parts costs, the next element of cost examined is that for fabricating a printed circuit board. Here actual (unpopulated) board costs for the finished products in both discrete and hybrid form were compared. Thus in the case of the relay driver, the total cost for the five boards using discrete parts (see Figure 13) was divided by four to allocate \$36 to the P.C. board cost for a single 8-Channel Relay Driver Function in discrete form; and the cost of the single board using hybrids was divided by four to allocate \$7 to that same function in the hybrid version. Similarly, costs for P.C. board fabrication were allocated to the discrete and hybrid circuit functions for the Digital Stimulus Buffer and the Measurements Buffer making use of cost records associated with boards shown in Figures 8 and 14 and taking into account the relative area utilization of the circuits on the boards.

The cost figures shown for P.C. board assembly are derived simply. The large differences here are a fundamental result of the substantially different number of parts being handled for the discrete versions compared with the hybrid versions. Although the dollars associated with P.C. board test are small compared with other cost elements, a parenthetical note is worth making, however. The discrete part versions of the circuit functions in general are still very much subject to failure at board test and costly diagnostic testing and rework must follow with potential degradation of an entire board. The cost for comparable testing, malfunction finding, and rework in the hybrid microcircuit is already built into the so-called piece part cost of the completed hybrid.

The next cost element in the table is concerned with carrying the circuit function costs to the next level of assembly. Thus, if the number of boards in a system is cut down, so too are the number of connectors that have to be assembled and wired in a chassis and the number (or size) of chassis and racks to handle the boards for a given system-level complement of circuit functions. For the 128 Universal-Test-Point configuration of the AN/USM-410 Test System, a half-rack of hardware with hybrids does the same job that two half-racks of hardware do with discrete parts. Thus, costs for the two versions, apportioned to single circuit functions, are shown for the three circuits on the line "CHASSIS MATERIAL ASSEMBLY".

The last cost element compares the support costs per circuit function for manufacturing methods engineers, test methods engineers and material control people.

The last line provides the total factory costs in the manufactured equipment for each of the three circuit functions. Each hybrid microcircuit comes out looking better than the discrete parts it replaced.

TABLE 1. COST COMPARISONS OF CIRCUITS - DISCRETE vs HYBRIDS

COST ELEMENT	COSTS PER CIRCUIT FUNCTION ^a					
	Relay Driver		Digital Stimulus Buffer		Measurements Buffer	
	DIS ^b	HYB ^b	DIS	HYB	DIS	HYB
BASIC PARTS (MAT'L)	\$15	\$45	\$17	\$55	\$40	\$82
PC BOARD FABRICATION	36	7	16	1	19	2
ASSEMBLY TO PC BOARD	15	2	17	1	16	1
CCT F'N - BOARD TEST	1	-	2	-	2	-
CHASSIS MAT'L/ASS'Y	12	7	12	7	12	7
MFG. ENG'G & SUPPORT	6	1	9	1	10	1
TOTAL COSTS	\$85	\$62	\$73	\$65	\$99	\$93
RELATIVE COSTS	100%	73%	100%	89%	100%	94%

^aCosts based upon circuit functions in quantities of 500-1000

^bDIS = Circuit using discrete parts; HYB = Circuit using hybrid

CONCLUSIONS

Hybrid microcircuit packaging has long answered a need where size, weight and performance have been driving requirements. Hybrids may now seriously be considered as cost effective even in relatively low production quantities if the total costs of manufacture in the end-item equipment are accounted for and in particular, if the beneficial effects of miniaturization are recognized.

ACKNOWLEDGMENTS

I want to give special recognition to the engineers who designed the electrical circuits for the hybrids so successfully used in the two ECOM systems: in the AN/GVS-5, to M. Teare for the Detector-Preamplifier, to L. B. Blundell for the Video Amplifier and to J. M. Quinn and N. L. Roberts for the Range Counter and Display; and in the AN/USM-410, to B. A. Bendel for the 8-Channel, Latching Relay Driver, to R. P. Percoski for the Digital Stimulus Buffer, and to D. F. Dion for the Measurements Buffer. Both Mr. Bendel and Mr. Percoski designed the Programmable Interface Unit with its universal test point approach and performed the initial cost analyses supporting use of hybrids in the AN/USM-410.

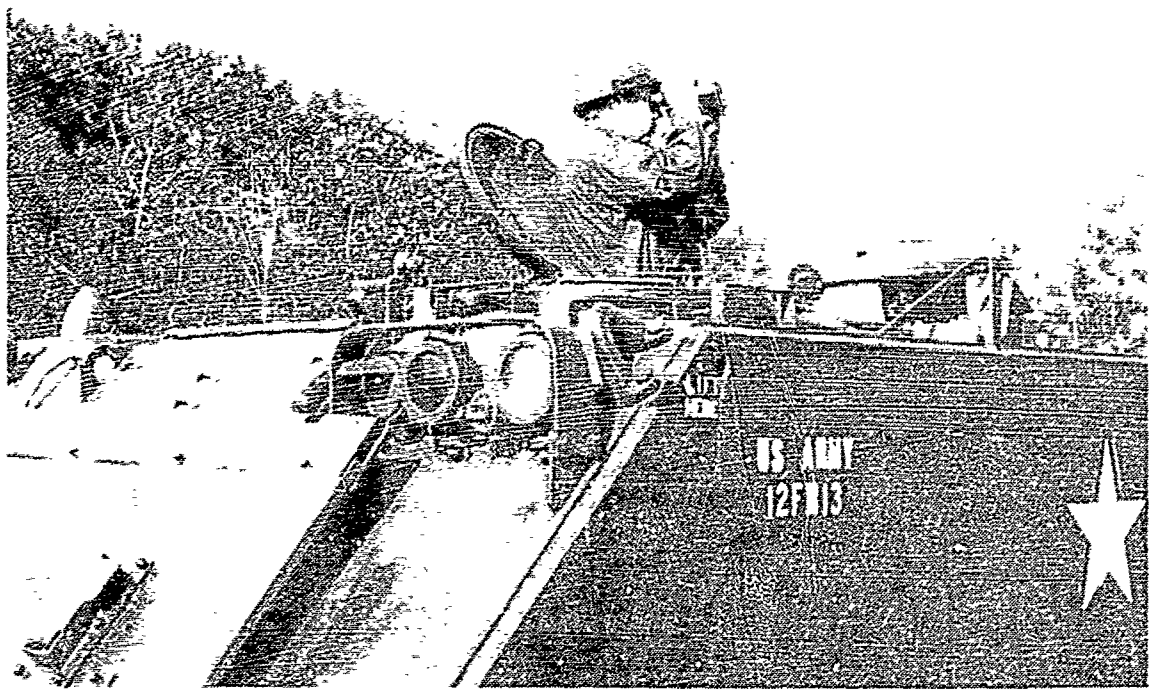


FIGURE 1 AN/GVS-5 HAND-HELD LASER RANGE FINDER

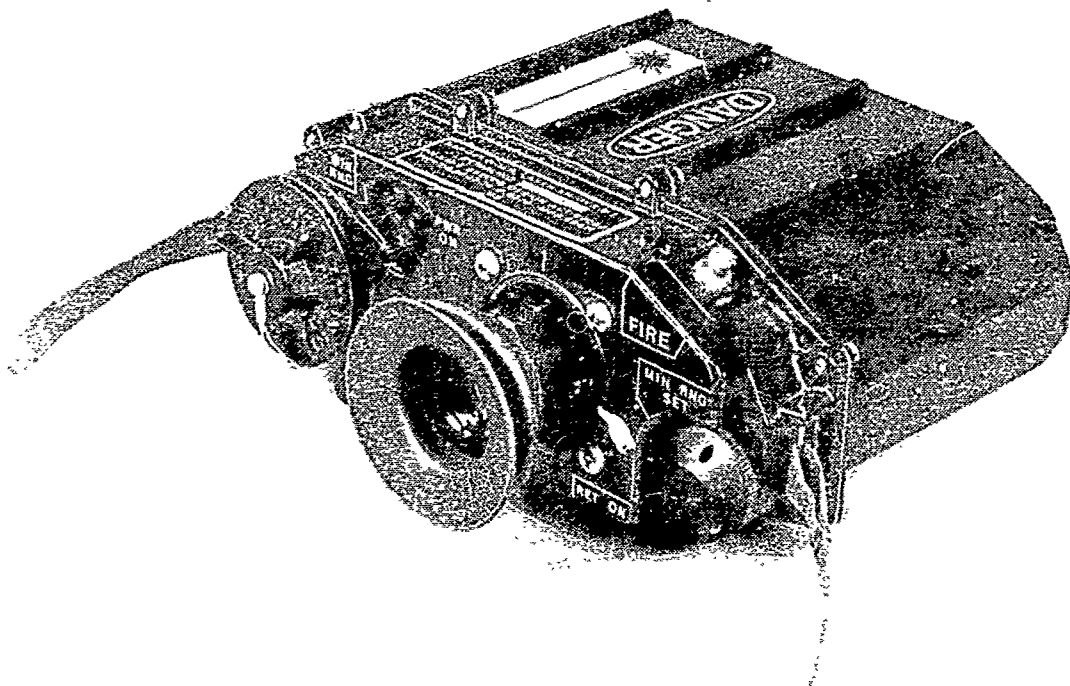


FIGURE 2. CLOSE-UP VIEW OF HAND-HELD LASER RANGE FINDER

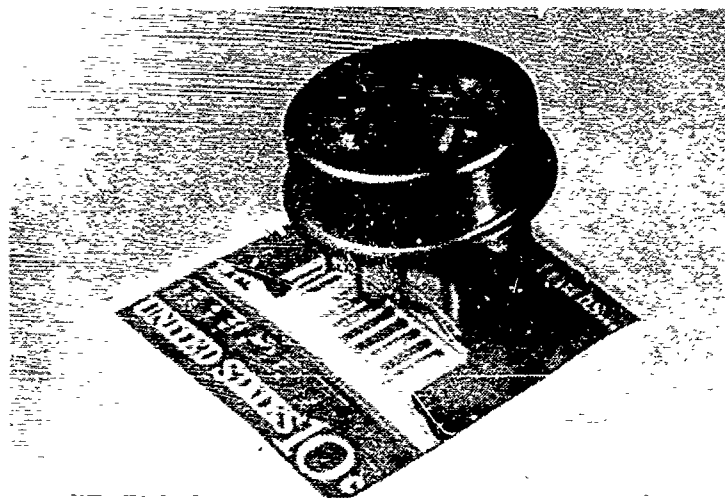


FIGURE 3. DETECTOR-PREAMPLIFIER HYBRID

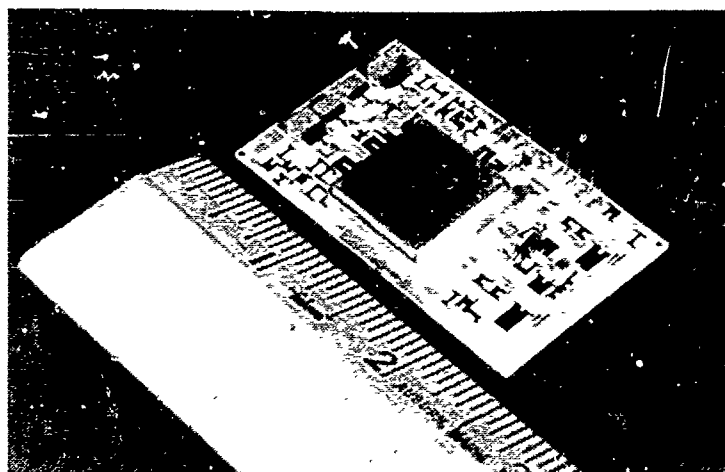


FIGURE 4. VIDEO AMPLIFIER HYBRID

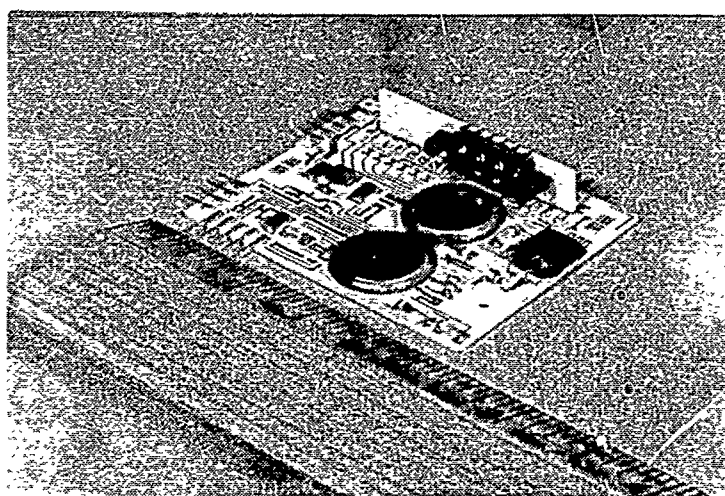


FIGURE 5. RANGE COUNTER AND DISPLAY HYBRID



FIGURE 6. AN/USM-410 AUTOMATIC TEST SYSTEM

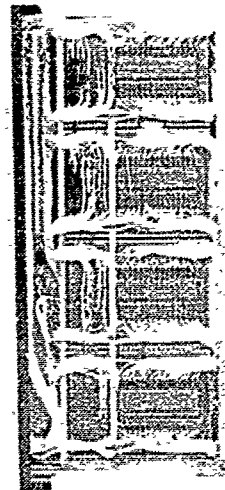


FIGURE 7. PROGRAMMABLE INTERFACE UNIT

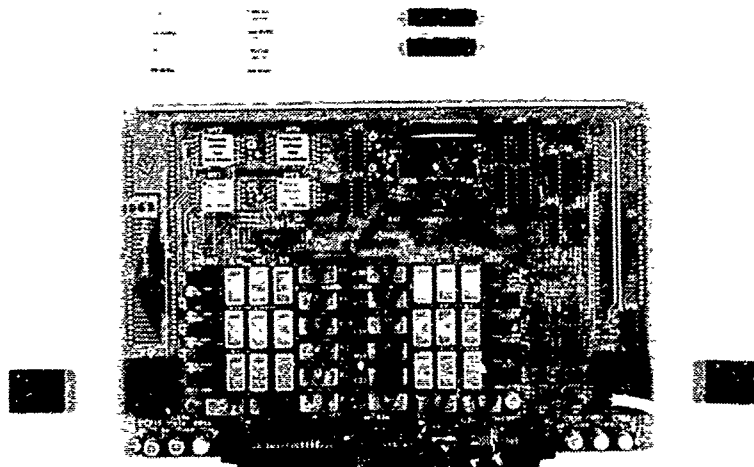


FIGURE 8. DUAL UNIVERSAL TEST POINT BOARD AND HYBRIDS

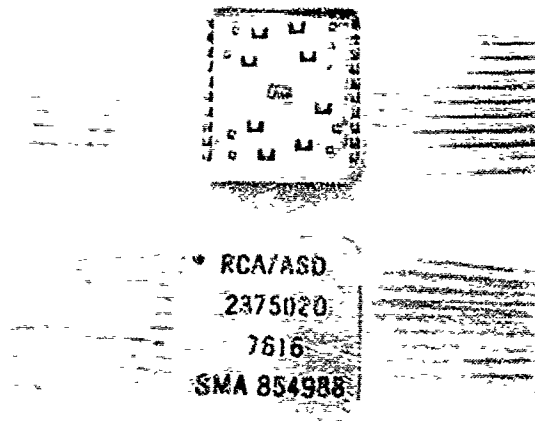


FIGURE 9. 8-CHANNEL, LATCHING RELAY DRIVER HYBRID

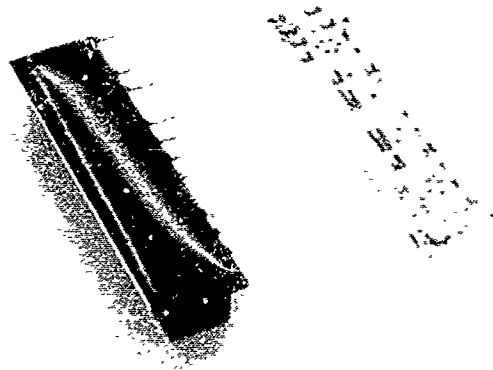


FIGURE 10. DIGITAL STIMULUS BUFFER HYBRID

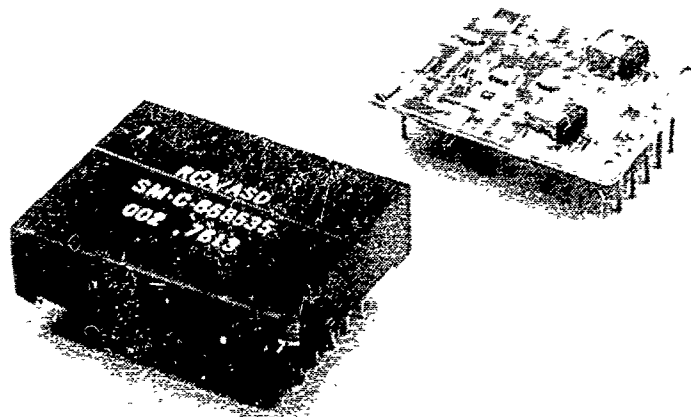


FIGURE 11. MEASUREMENTS BUFFER HYBRID

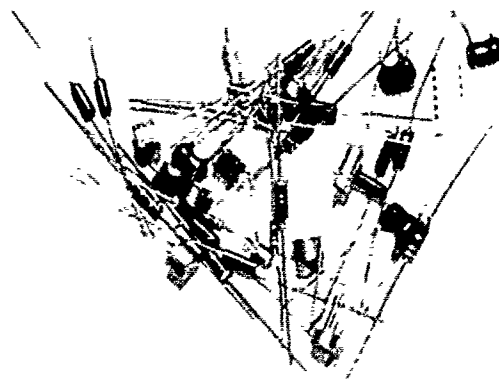


FIGURE 12. COMPARISON OF PARTS COSTS

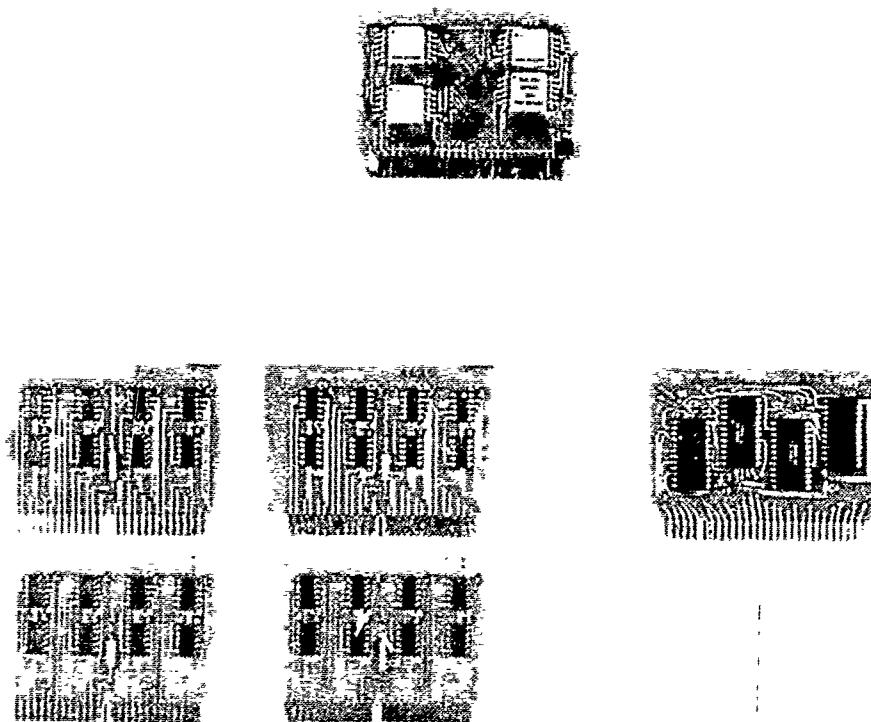


FIGURE 13. HARDWARE REDUCTION FROM USE OF HYBRID RELAY DRIVER

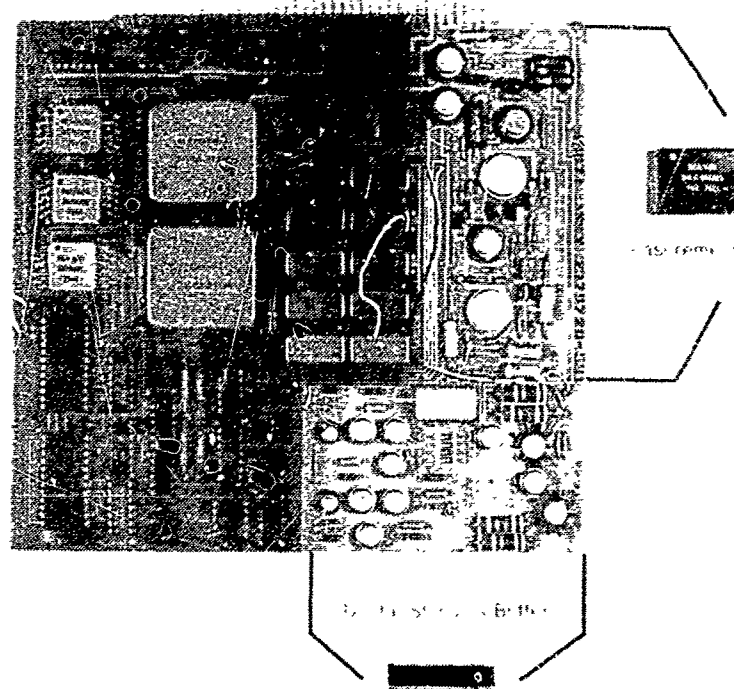


FIGURE 14. UNIVERSAL TEST POINT BOARD (EARLY VERSION)

APPLICATIONS OF HYBRID MICROCIRCUITS IN MANPACK RADIO EQUIPMENT

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ABSTRACT

Microelectronic technology has certainly impacted the modern soldier this past decade. He is required to operate many sophisticated weapon systems, to carry greater loads and more complex radio equipments, and to communicate effectively with supporting armaments and other personnel. In order to maximize his effectiveness, his communications equipment must be easy to carry and reliable. The application of large scale integration (LSI) and multi-chip hybrid microcircuit techniques has proven to be an effective tool to achieve the size, weight, cost reduction, reliability and performance goals required in military manpack radio equipment.

INTRODUCTION

Tactical man-portable military radio equipment poses many problems in the packaging phase due to the emphasis placed on both the various design factors and the need for strict adherence to military specifications and standards. Size is severely limited and weight is critical since the equipment must be transported by men in the field. The equipment must meet environmental as well as electrical and reliability performance standards and must also be designed to satisfy military maintenance and logistics requirements.

This paper describes Cincinnati Electronics' experience in developing the multi-chip hybrid microcircuits for three specific manpack radio equipments that cover the HF, VHF and UHF military frequency ranges: AN/URC-78, AN/PRC-70 and AN/PSC-1. It will discuss why and how hybrids were used in a wide variety of circuit applications which include the use of hybrids as a LSI development tool. After illustrating several types and complexities of hybrids, the parts, materials and processes used in these applications will be briefly discussed. In addition, environmental test results of the final equipments and some resultant failures will be reviewed. The concluding remarks will describe the final equipments successfully developed as a result of using hybrid microcircuit packaging technology.

WHY HYBRIDS?

Small Size And Weight

Hybrids can significantly reduce the size and weight of the end equipment. Printed circuit board area reductions of more than thirty times were realized using hybrid packaging techniques.

Low Power Consumption, Lower Operating Cost

Batteries are by far the highest cost item in the operating life of any manpack radio. The cost of battery power alone has been estimated as approximately one thousand dollars per watt over the life cycle of the equipment.¹ To maximize battery life and minimize battery weight it is necessary to design for the lowest power consumption possible. Hybrids permit lower power requirements than equivalent circuits in discrete form due to the low interconnection capacitance between circuit elements. Hybrids can also be used in many low power analog circuits where no equivalent monolithic IC devices are available and, if monolithic IC devices do exist, their power consumption is usually excessive.

Improved Reliability

Hybrids offer improved reliability because the number of electrical interconnections can be reduced through the use of thick film resistors and printed conductor patterns. This reduction of interconnections also reduces the number and complexity of PC module boards. Smaller package seal areas also improve reliability.

Short Development Cycle, Ease Of Repairability

Frequently, the development schedule for military equipment is very short. The thick film hybrid microcircuit not only lends itself to quick turn-around time, but is also completely adaptable to design changes and repair. Prototype quantities were typically delivered four to eight weeks after design release, depending upon circuit complexity.

Provides Hermetic Environment, Improves EMI Performance

Metal packages with metal cover seals provide a hermetic environment for all circuit elements and electrical interconnections contained within the package. The hybrid also provides improved EMI and isolation characteristics with its metal package and short lead lengths when compared to larger conventional component assembly techniques.

CIRCUIT APPLICATIONS

The thick film hybrid microcircuit is readily adaptable to almost every circuit function in a radio design. The following list shows several circuit applications successfully implemented in the three manpack radios. These applications covered the frequency range from DC to 200 MHz, and power levels from microwatts up to 10 W at 80 MHz.

- Audio Amplifiers And Squelch
- Active Filters
- Frequency Control And Memory
- Antenna Coupler Tuning
- Regulated Power Supplies
- Digital Synthesizers
- RF Switches
- High Gain IF Amplifiers (120 dB at 12.5 MHz)
- RF Power Amplifiers (10 Watts at 30 - 80 MHz)

Performance Improvement

Variable divider circuits are only one of the numerous applications which illustrate the improvement of several parameters by using hybrids. In hybrid form, the circuit had higher frequency performance at lower power levels than their equivalent circuit design in discrete form.

The AN/URC-78 variable divider breadboard operated at frequencies up to 5.2 MHz. The hybrid operated to frequencies over 8 MHz. A CMOS variable divider in the UHF manpack radio breadboard had an operating power requirement of 260 mW; the hybrid only required 160 mW.

HYBRID USAGE

Considerable emphasis was placed on the use of hybrids as shown by the total quantities and types used. These hybrids varied in complexity from simple RF switches in TO5 headers to multi-chip LSI hybrids packaged in 60 pin one-inch square packages. The quantity of hybrids used in each equipment is summarized in Table I.

TABLE I. HYBRID USAGE-MANPACK RADIOS

	AN/URC-78 VHF	AN/PRC-70 HF/VHF	AN/PSC-1 UHF
HYBRID MICROCIRCUIT TYPES	39	13	34
TOTAL HYBRID MICROCIRCUITS PER RADIO SET	42	13	44

THICK FILM HYBRID MICROCIRCUIT AS LSI DEVELOPMENT TOOL

One of the best techniques to achieve low cost in the design of radio equipments is the use of digital circuitry that can be readily converted to LSI for final development models and subsequent volume production. Several problems were confronted in directly implementing LSI devices into the exploratory development radio equipments. First,

there were many possibilities for error, especially in layout. Also, it was necessary to package the final equipment size as early as possible in the development to realize the effects of circuit strays and EMI problems that usually arise in densely packaged radio equipments. Because LSI design and development is generally costly and time-consuming, it is desirable to produce a circuit that can work in the same environment as the final LSI package. The hybrid microcircuit provides the means of attacking these problems both in the development phase and in final production.

LSI Packaging Evolution

The preset and frequency displays utilized in the AN/URC-78 equipment are excellent examples of how the hybrid was applied to solve these various problems. Figure 1 shows the natural evolutionary process toward the final microminiaturized package configuration. In the upper portion is shown the breadboard which utilized several cards containing standard 4000 Series CMOS logic. This breadboard was divided into three basic functions: (1) a MHz counter type circuit, (2) kHz counter type circuit, and (3) a control circuit that interfaced with both the MHz and kHz counters. Both the information from the kHz and MHz counters are displayed on the front panel of the radio.

Since an exploratory model of the final packaged radio was required in fourteen months, it was impractical to attempt to convert from the breadboard directly to the final multi-chip LSI hybrid. This hybrid is shown mounted to the pin light display PC card at the bottom of Figure 1. Because of the short development cycle and form factor requirements, a decision was made to convert the breadboard to three hybrid microcircuit packages shown below the breadboard circuit cards.

Early Development Typical Hybrid

The hybrid shown in Figure 2 is typical of the three hybrids constructed for the AN/URC-78 Exploratory Development Model. Each hybrid contained approximately forty individual 4000 Series CMOS integrated circuit chips positioned exactly as the final three LSI chips were to be designed. Thus, each hybrid provided an environment that closely simulated the anticipated LSI packaging configuration.

These hybrids enabled the Exploratory Model to be produced very nearly to the form factor of the final equipment. This enabled the equipment to be thoroughly checked out and provided a high degree of confidence that the final development models would perform in a similar manner. Although these complex hybrids usually do not lend themselves to production usage, they did perform well as development tools.

AN/URC-78 Frequency Control LSI Hybrid

During the Advanced Development phase, the three forty-chip thick film hybrid microcircuits were successfully converted into three individual custom LSI circuit chips. These three LSI chips along with their associated circuitry were subsequently packaged in the $3/4 \times 1$ inch package shown in Figure 3. This hybrid is the final frequency control circuit for the entire AN/URC-78 Manpack Radio equipment. The completely packaged assembly is shown in Figure 4.

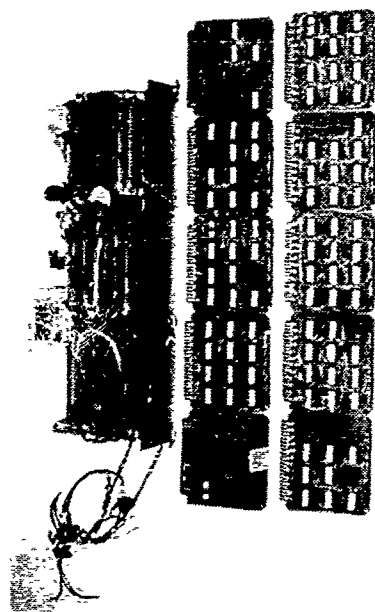


Figure 1.1 Early Development Hybrid VLSI Package (AN VRC-75)

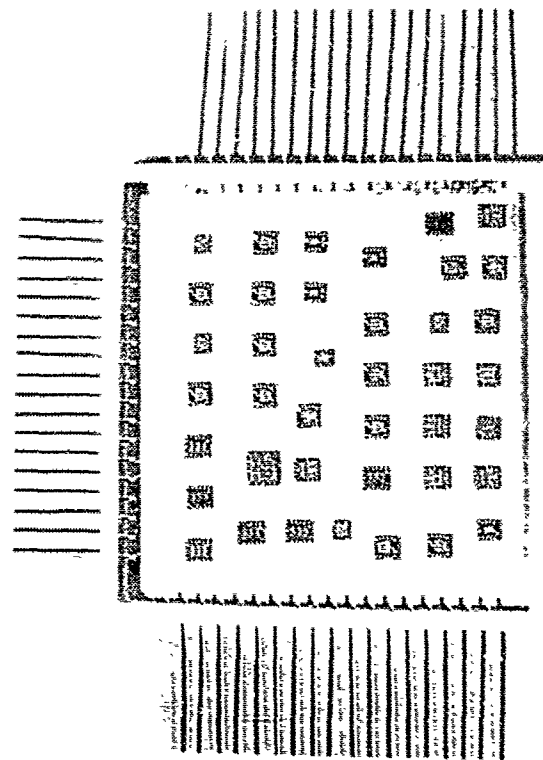


Figure 1.2 Early Development Hybrid VLSI Package (AN VRC-75)

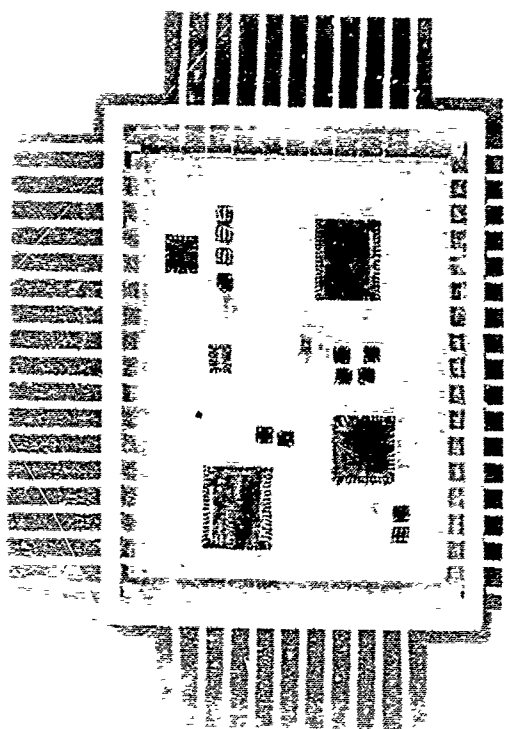


Figure 1.3 Frequency Control VLSI Hybrid (AN VRC-75)

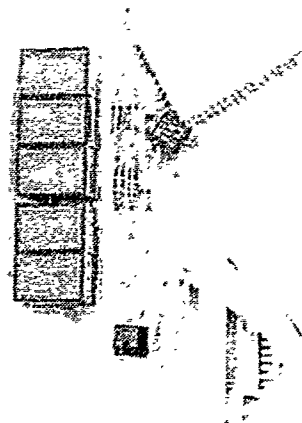


Figure 1.4 Frequency Control Module Card (AN VRC-75)

All three LSI chips performed on the first design and are still performing today after two years of rough handling in the course of development and evaluation.

Several other custom LSI hybrids were developed for other radio equipments and an order of magnitude increase in density and reliability was also achieved. This whole concept proved to be technically and economically feasible through the use of extensive automation in LSI layout design, mask-making and test generation. The thick film hybrid clearly functions both as an interim development tool for design verification in a short time frame and, in its final LSI form, provides a package that is readily adaptable to volume production.

THICK FILM HYBRID MICROCIRCUIT APPLICATIONS

Typical Module Card (AN/URC-78)

The module shown in Figure 5 typifies the packaging used in all manpack radio equipments. It clearly shows the extensive use of multi-lead hybrid microcircuits in a final equipment packaging design. This module performs the receive and transmit audio and squelch functions for the AN/URC-78 manpack radio. The board size is approximately 4.5×2.75 inches.

10W PA Hybrid (AN/URC-78)

This hybrid (Figure 6) exemplifies how the thick film technology can be successfully applied to broadband RF power amplifiers in the 10W region. This amplifier provides 10 dB of gain, flat within 1 dB over a 30-80 MHz range. A size reduction greater than 10:1 in volume was realized, compared to the discrete component breadboard. The power transistor chips are mounted on beryllia carriers and electrically interconnected using 3-mil gold wire. The electrical design incorporates circuitry for temperature, power dissipation and peak current limiting.

IF Amplifier Hybrid (AN/PRC-70)

Three hybrids of this complexity (See Figure 7) provide greater than 100 dB of IF amplification in the AN/PRC-70 manpack radios. An AGC range of 90 dB was precisely sequenced within a linearity of ± 2 dB using functional laser trimming techniques. Demodulation is also provided for AM, FM, USB, LSB, CW and FSK operation. The component density of these hybrids is approximately 120 parts per square inch.

Data Mod Control Hybrid (AN/PSC-1)

This hybrid (Figure 8) is representative of a high density digital circuit. Twenty-one IC chips were mounted on a four metallization multilayer substrate and packaged in a $1/2$ by 1 inch flat package. The circuit function encodes input data for either BPSK or QPSK modes of operation. This circuit, like the FREQUENCY CONTROL hybrid in the AN/URC-78, could be readily converted into LSI design in production quantities.

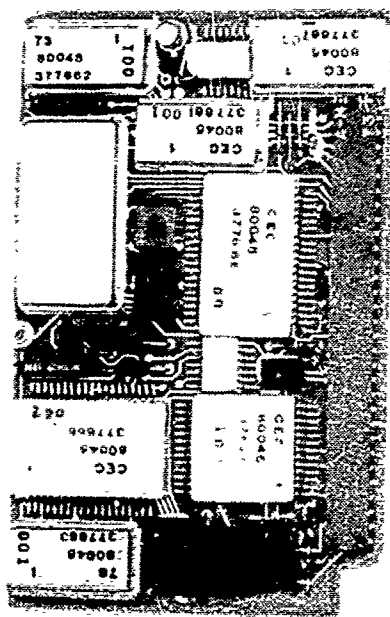


Figure 5. Typical Module Card (AN/URC-78).

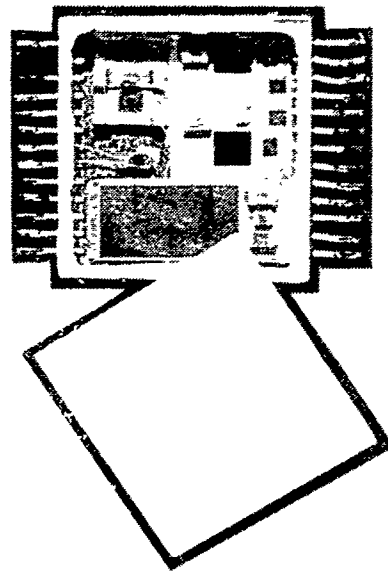


Figure 6. 10W PA Hybrid (AN/URC-78).

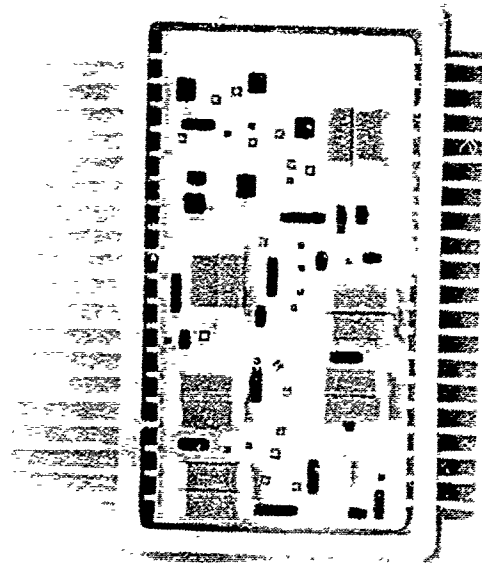


Figure 7. IF Amplifier Hybrid (AN/PRC-70).

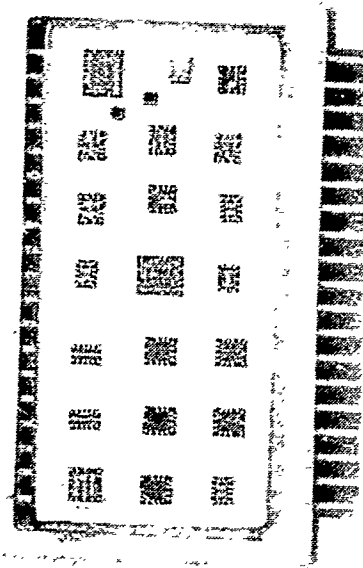


Figure 8. Data Mod Control Hybrid (AN/PSC-1).

Band Pass Filter Hybrid (AN/PSC-1)

The BPF hybrid (Figure 9) is also typical of a high component density circuit. This hybrid consists of 71 chip devices mounted on a $1/2 \times 1$ inch multilayer substrate. The circuit is used as a signal detector for BIT SYNC acquisition.

ACQ SWEEP Hybrid (AN/PSC-1)

The ACQ SWEEP hybrid (Figure 10) typifies the largest substrate and package size used in current manpack hybrid development. Again, it is an example of all CMOS circuitry and short leads which provide lower operating power than conventional discrete component designs.

The ACQ SWEEP hybrid performs three circuit functions. It first generates a pretune function for the VCXO. When the lock detector detects low pretune beat frequencies, the threshold detector determines if the signal is within the lock range of the carrier tracking phase-locked loop. This circuitry, in turn, corrects the VCXO pretune voltage to permit tracking of any frequency change in the received signal.

CPU Hybrid (AN/PSC-1)

The CPU hybrid (Figure 11) is another example of a multi-chip LSI hybrid. This hybrid includes a microprocessor, RAM memory, memory address and address decode for sixteen peripheral devices. This hybrid package allowed a 31:1 reduction in required PC board area compared to the breadboard discrete design. The microcomputer hybrid requires 1.4 square inches of PC board area and has 54 connections. It replaces 15 conventional LSI/MSI devices mounted to 43 square inches of multilayer PC board area with over 300 connections.

PARTS, MATERIALS AND PROCESSES

In order to minimize the cost of hybrid development to the government, no effort was made to independently evaluate the numerous microelectronic packaging methods and technologies available. This condition forced us to economize and choose the best approach based on current technology information and good engineering judgement consistent with end equipment requirements.

Thick-Film Substrate And Resistor Metallurgy

The substrate conductor networks were predominantly provided by using a thick-film gold paste system. Platinum-gold was used where reflow-solder attachment was required. Screen-printable dielectric pastes were used for multilayer substrates where high component densities were required. Up to five metalization layers were used. A ruthenium-based resistor paste system was chosen to provide:

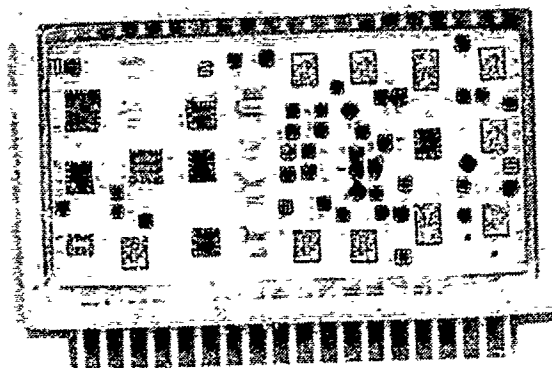


Figure 9. Band Pass Filter Hybrid (AN/PSC-1).

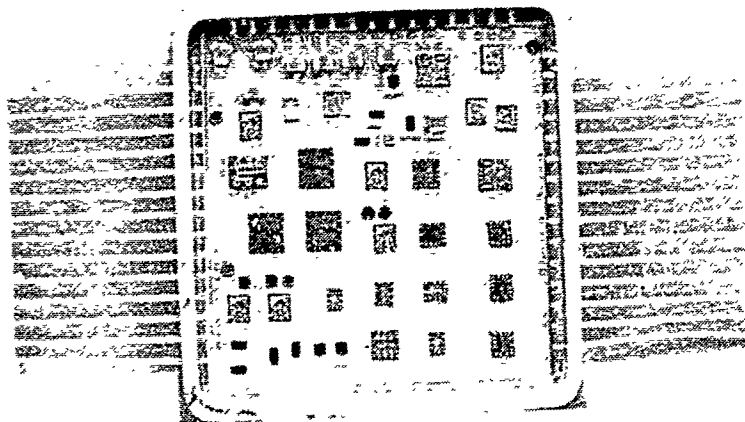


Figure 10. ACQ Sweep Hybrid (AN/PSC-1).

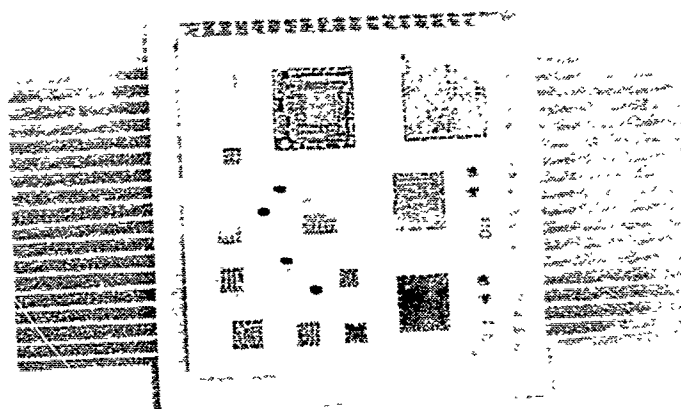


Figure 11. CPU Hybrid (AN/PSC-1).

- (a) a wide range of resistivities ($10 \Omega/\text{sq.}$ to $1 \text{ M}\Omega/\text{sq.}$);
- (b) low TCR characteristics (25 ppm-200 ppm);
- (c) good stability characteristics after laser trimming.

Resistor tolerances ranged from 0.25% to 10% and were used in a power range of 20mW to 5W.

Thick-Film Parts And Attachment Techniques

Unglazed 96% alumina substrates were used in sizes up to one inch square. They were attached to the metal packages with non-conductive epoxy. This combination of package size and attachment method enabled us to meet 10,000 G constant acceleration test environments with no failures. Integrated circuit chips were attached to the substrate using non-conductive epoxy. Other semiconductor devices were attached with conductive epoxy. Both monolithic ceramic and MOS capacitor chips were attached to the substrate with conductive epoxy. Inductor chips were attached using solder-reflow techniques, and thin-film resistor chips were attached with non-conductive epoxy.

Electrical Interconnection

All integrated circuit devices were electrically interconnected to the substrate metalization network with ultrasonically bonded, one-mil gold wire. Power transistors were interconnected to the substrate with three-mil gold wire. Electrical interconnection of all other semiconductors was made using both conductive epoxy and one-mil gold wire. Solder-reflow was used for electromechanical attachment of all inductor chips.

Hermetic Packaging And Sealing

All-metal packages with glass-sealed leads were used to achieve the best hermeticity and EMI protection as well as good repairability. Flat packages with up to sixty leads per package were sealed using a parallel-gap welded cover. Dual-in-line packages were either welded or reflow-soldered in a parallel gap welder. TO5 and TO8 headers were sealed with a resistance welded cover.

It should be noted that none of the process techniques used exposed the active circuit devices in the hybrid to temperatures exceeding 150°C . As a result, we realized a high yield during manufacturing operations. The use of epoxy and parallel-seam welded covers enabled us to easily repair or modify circuits throughout the development of these radios. The use of these process techniques has been evaluated by other hybrid manufacturers and was found to produce improved yields during manufacturing operations.²

Thick-Film Hybrid Flow Chart

The chart in Figure 12 shows the manufacturing sequence typical of the hybrid microcircuit product line used for manpack equipments. The manufacturing steps are shown in squares and the in-process control and inspection steps are shown in circles. All hybrids developed on these programs were subjected to the Class B level screening requirements of MIL-STD-883. Constant acceleration was reduced to 10,000 G in the Y1 plane due to the large package sizes and end equipment requirements.

END EQUIPMENT ENVIRONMENTAL TEST RESULTS

AN/URC-78

Six AN/URC-78 radios were subjected to the developmental tests shown in Table II. The equipments successfully passed all tests except airborne vibration; a hybrid microcircuit in a dihedral-type design failed to withstand this environment. As a result of this test, the use of this particular package type has been discontinued.

TABLE II. END EQUIPMENT-ENVIRONMENTAL TESTS (AN/URC-78)

- AN/URC-78 Developmental Tests Per MIL-STD-810
 - High & Low Temp., Ground Equipment
 - Temp. - Alt. Test
 - Elevation Test
 - Ground Vehicular Vibration
 - Air Vehicular Vibration
 - Ballistic Shock
 - Drop Test
 - Vehicular Bounce
 - Bounce, Loose Cargo
- AN/URC-78 Ground Nuclear Environment
 - Radiation
 - EMP
 - Overpressure
 - Thermal Blast

AN/PRC-70

AN/PRC-70 Service Test Radios were successfully subjected to both Qualification and Reliability tests (see Table III). No hybrid failures occurred in qualification testing and two failures occurred in reliability testing; both failures were traced to CMOS chip devices. These failures were not associated with the processing of the hybrid microcircuits.

TABLE III. END EQUIPMENT-ENVIRONMENTAL TESTS (AN/PRC-70)

- AN/PRC-70 Qualification Tests Per MIL-STD-810
 - Drop Test
 - Vehicular Bounce
 - Bounce, Loose Cargo
 - Vibration, Resonant Search
 - High Temperature
 - Low Temperature
 - Reliability Testing
- AN/PRC-70 Reliability Tests (7000 Hrs. at +15°C with Vibration 1/4 of Time.

One of the processing problems that occurred during screen testing of these hybrids resulted from the use of conductive epoxy as an electrical connection to TO5 and TO8 header pins. This connection failed during temperature cycling because the non-conductive epoxy attachment of the substrate had a greater coefficient of expansion than the conductive epoxy. This problem was resolved by replacing the conductive epoxy attachment with an ultrasonic gold wire bond. Other problems involved cleaning and handling techniques, and were quickly identified and corrected.

FINAL EQUIPMENTS

AN/URC-78

The AN/URC-78 manpack radio (Figure 13) was developed for the U.S. Army Electronics Command and is an FM equipment operating in the frequency range from 30-80 MHz. This radio is a 10W transceiver, contains 2000 channels of operation, and is packaged in a ninety cubic inch volume.

AN/PRC-70

The AN/PRC-70 manpack radio (Figure 14) was also developed for the U.S. Army Electronics Command and is a multi-mode equipment operating in the frequency range of 2-76 MHz. This radio operates in the AM, FM, CW, SSB, and FSK modes. It is a thirty-watt transceiver with 100 Hz channel spacing.

AN/PSC-1

The AN/PSC-1 manpack radio (Figure 15) is currently being developed for the Communication Satellite Agency at Ft. Monmouth. It operates over the UHF frequency range of 225-400 MHz and provides either satellite relay or direct line-of-sight communication. This radio is a 35W transceiver and contains an internal modem for either BPSK or QPSK operation. The complete system, including transceiver, battery, handset, whip antenna, and carrying harness weighs 11.34 kilograms (25 pounds).

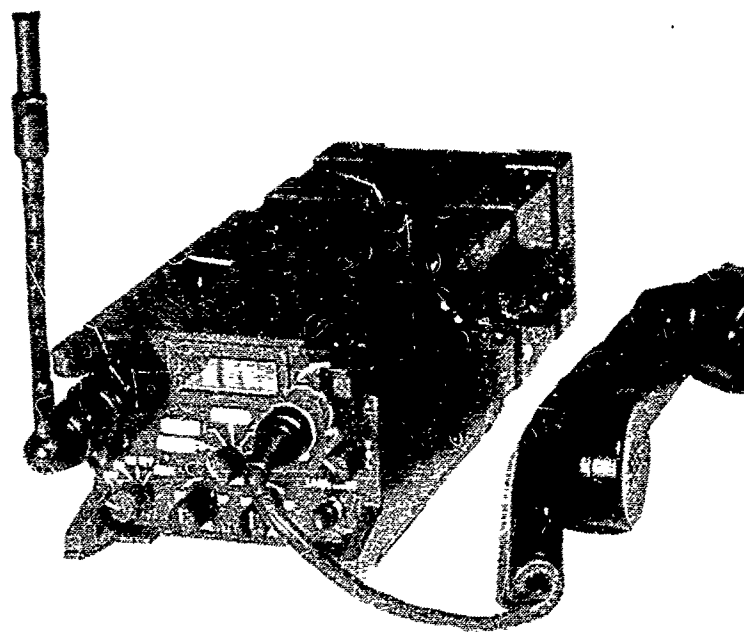


Figure 13. AN/URC-78 Manpack Radio.

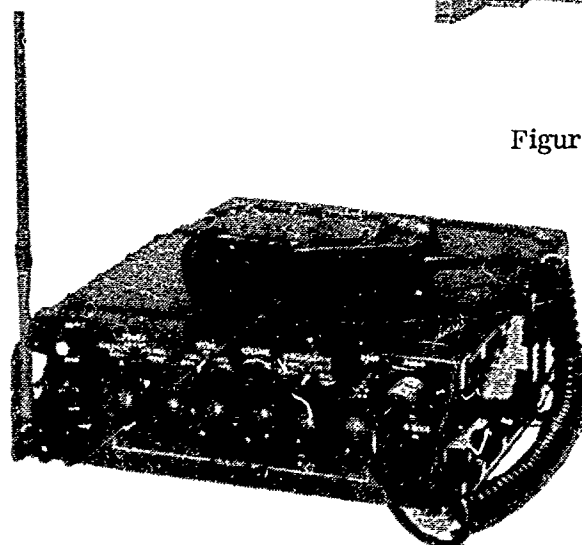


Figure 14. AN/PRC-70 Manpack Radio.

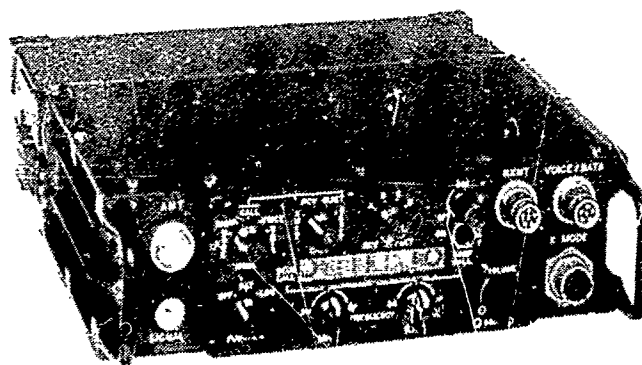


Figure 15. AN/PSC-1 Manpack Radio.

CONCLUSION

Thick-film technology is readily adaptable to the needs and requirements of manpack radio equipment. A variety of packaging designs has been presented to illustrate the wide scope of feasible circuit applications that were successfully implemented in three radio equipments. The capabilities of hybrid technology were exploited in the areas of improved performance, high power, dense packaging, lower cost, higher reliability and custom LSI development. The feasibility of designing and fabricating custom LSI multi-chip hybrid microcircuits was demonstrated on several manpack equipment programs.

Parts, materials and processes were selected to meet the stringent manpack radio environmental requirements and to produce the complex, high density hybrid microcircuits as economically as possible. Use of low temperature processing methods permitted ease of repairability and rework as required, and assured the highest manufacturing yields possible. The use of hybrid microcircuits has proven to be a very effective tool in achieving manpack radio equipment design and performance goals.

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APPLICATION OF HYBRID MICROWAVE INTEGRATED CIRCUITS IN A TACTICAL RADIO RELAY SET

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ABSTRACT

Design of the 1350-1850 MHz tuning heads for Radio Set AN/GRC-103 posed problems in the fields of reliability, reproducibility, maintainability and size which were solved by use of hybrid microwave integrated circuits in four different applications. These were a broadband low noise amplifier, a 1 watt high power amplifier, a frequency converter and a monitor and alarm unit, all operating in the 1350-1850 MHz range. A standard hermetic package was adopted. Factors considered in selecting circuits for integration are reviewed, a brief review of the circuit designs is given, and problems encountered in construction and test are discussed.

INTRODUCTION

Radio Set AN/GRC-103(V) is a transportable radio relay set operating in various frequency bands by exchange of plug-in r-f assemblies. In June 1973 Canadian Marconi Company was awarded a contract for the development of the Band IV tuning heads of this radio set, for operation in the frequency range 1350 MHz to 1850 MHz. Previous versions for frequency bands from 220 MHz to 1000 MHz had been developed using conventional discrete component technology. The Band IV version presented special problems not only because of the increased frequency but also because of an upgrading of specification requirements in areas of reliability and maintainability.

A functional block diagram of the tuning heads is shown in Figure 1.

Modulated r-f from the Transmitter Radio is multiplied to final frequency in a frequency multiplier. Unwanted frequency multiples and noise are removed by a tunable band pass filter. The r-f is amplified to final power level in a tube-type power amplifier, chosen for compatibility with the designs of the other tuning heads. Transmitter and receiver share a common antenna and are combined by a duplexing network consisting of two tunable filters and a circulator. The received signal is down-converted to i-f in a mixer stage and the i-f is sent to the Receiver Radio via an i-f pre-amplifier. The mixer stage receives its local oscillator signal from a

frequency multiplier driven from the Receiver Radio. The local oscillator signal is purified of unwanted multiples and noise by a tunable band pass filter.

The major active circuits in the tuning heads are the frequency multipliers in both transmitter and receiver, the transmitter power amplifiers, the mixer which contains a low noise amplifier, and an i-f pre-amplifier. The power amplifiers are of tube type both for ruggedness and compatibility with the power supply arrangements of the basic radio set. The i-f pre-amplifier is a module common to other frequency tuning heads. Thus the items for which microwave integrated circuits might be used are the transmitter and receiver frequency multipliers, and the mixer stage.

Compared to conventional discrete circuit design, microwave integrated circuits were considered to have the following advantages:

- a) Improved circuit realizability due to the generally smaller interconnecting lengths possible.
- b) Improved producibility due to the more precise location of interconnections and hence improved control of parasitic impedances.
- c) Improved reliability due to the construction technology.
- d) Improved maintainability due to the module nature of the microwave integrated circuits.
- e) Easier packaging into the tuning heads due to generally reduced size.

The disadvantages anticipated were increased design costs and increased manufacturing costs.

The circuits selected for realization as microwave integrated circuits were:

- (i) the low noise amplifier used in the Mixer Stage.
- (ii) the frequency converter used in the Mixer Stage.
- (iii) the output power amplifier of the transmitter frequency multiplier.
- (iv) the power monitor and alarm unit used in the receiver frequency multiplier.

The receiver frequency multiplier was realized as a direct step-diode multiplier and required no UHF power amplification.

CIRCUIT DESCRIPTION

i) Broadband Low Noise Amplifier

The broadband low noise radio frequency amplifier, shown in Figure 2, in block diagram form, consists of a balanced amplifier stage, followed by

a single-ended stage. The balanced configuration is chosen to achieve the required low noise figure over the 1350 MHz to 1850 MHz operating frequency range, while maintaining an adequate input match. A low VSWR at the input is required to provide a matched termination for a bandpass filter which precedes the converter.

The 3 dB couplers are realized as dual 8 dB parallel line couplers. The input transistors Q1 and Q2 are matched for best noise performance. Their outputs are matched for optimum VSWR at the upper band limit. The output transistor is matched for optimum power gain. Its output circuit contains an equalizer which corrects for the gain variations due both to the inherent gain roll-off of the transistors and the deliberate mis-matching introduced in the input stages.

Hybrid microcircuit technology is especially advantageous from the point of view of compactness and for good grounding requirements at these higher frequencies. This amplifier was developed by use of extensive computer-aided design techniques covering broadband matching, noise figure optimization, and realization and evaluation of microwave integrated circuit components. State-of-the-art semiconductors were employed in the design to achieve the required gain and noise figure.

ii) Frequency Converter

The frequency converter, shown in Figure 3, used in this design is of the image rejection type. The use of the broadband low noise amplifier in the previous stage makes this a requirement, since the image frequency of the amplified signal will always be present at the input of the mixer. This type of image rejection mixer takes advantage of the image amplitude cancellation which occurs when two balanced mixers are driven through a 3-port network that divides the amplitude equally, but in phase quadrature, at its two output ports, then recombines the two i-f outputs through a similar type of network, but operating at the intermediate frequency. This concept is identical to that used in the Bands II and III AN/GRC-103(V) mixer stage designs.

The couplers are realized in parallel line form. The local oscillator coupler which must provide in-phase rather than quadrature outputs, is of the Wilkinson type. The i-f hybrid combiner is external to the microwave integrated circuit.

Hybrid integrated circuit technology is especially advantageous in this application, since amplitude and phase unbalance of the two mixer branches are extremely critical in achieving good image rejection. The two balanced mixers employ Schottky barrier diodes since these offer excellent conversion properties at low local oscillator power level.

iii) High Power Amplifier

The amplifier, shown in Figure 4, is a wideband, variable gain, three-stage transistor amplifier with a PIN diode level control (electronic attenuator) between the first stage and second stage. The signal from the second stage is split by a Wilkinson in-phase splitter to feed the third stage which consists of two transistors. The amplified signal then is com-

bined by a Wilkinson in-phase combiner to achieve the final output power. The output level of the amplifier is monitored via a 16 dB coupler, using a Schottky barrier diode.

Hybrid technology is important because of high component density and also the difficulty of realizing the Wilkinson splitter and coupler as discrete circuits.

iv) Power Monitor and Alarm

The power monitor and alarm circuit, see Figure 5, consists of a coupler-detector section, a fixed attenuator and a low pass filter. The signal from the frequency multiplier coaxial resonator is fed through the coupler-detector section which has an r-f detector on the coupled line, is then attenuated to the proper operating level, and filtered by the low pass filter to reduce high order harmonics before reaching the output connector.

The advantage of constructing this module as a microwave integrated circuit was simplification of the overall packaging of the assembly containing it, which contained several other similar packages.

CONSTRUCTION

The package chosen was a shallow pressed-steel box which could house a 2" x 1" x .025" substrate. This size is a compromise between the conflicting requirements of rigidity, flatness, and size adequate to provide the physical circuits required in the 1350 MHz to 1850 MHz range. 2" x 1" is a relatively common substrate size. The package had previously been used on other programs of the Company.

The four hybrid microwave integrated circuits are constructed on 2" x 1" x .025" thick alumina substrates. The substrates are then mounted in the metal box which is approximately .35" deep. The box has glass sealed feedthrough conductors through its sides which have been carefully designed to provide the required r-f matching. This construction allows the box to be mounted on its side on a printed circuit "mother" board which not only reduces the area which is taken up by the box on the printed circuit board, but also permits direct, short connections which are desirable for the r-f signals. The box has a lip on the open face which allows the cover to be securely soldered all around to provide hermetic seal.

The substrate is alumina and all conductor patterns are gold plated. Most resistors are thin film, many of them adjustable by trimming, and some 1/8 watt discrete resistors are also used. Most capacitors are chip type, some variable, but where the value was low, and the packaging permitted, the capacitance of the substrate was utilized. There are some discrete inductors but again where possible the circuit inductance was utilized. Packaged transistors are used in the broadband low noise amplifier in order to allow proper characterization of the devices before assembly while chip transistors are used in the high power amplifier to ensure good heat transfer and because individual characterization is not critical in that application. Diodes are chip or beamlead devices.

PROBLEM AREAS

There were several problems encountered during design and small scale production. Most of these have been successfully solved.

An equalizer circuit is located at the r-f output connection of the low noise amplifier unit. Part of this equalizer is an interdigital capacitor, integral to the substrate, see Figure 6.

While the engineering prototype worked well, the production model had poor VSWR. Initially it was suspected that there was a short circuit between the fingers of the capacitor which are only .002 ins. apart, but a thorough investigation did not confirm this. Several more microcircuits were then made, using different processes which proved that if there is insufficient amount of gold over the nichrome, the capacitor will not perform as designed due to higher losses.

Soldering some of the chip components to the substrate was met with mixed success only due to leaching of the thin gold layer. This was overcome by using solders with high gold content, or tab mounting sensitive components, or using components, such as capacitors, with solder coated termination instead of gold.

The biggest problem encountered, however was the high temperature storage and burn-in requirements (Test Methods 1015 and 1008 of MIL-STD-883). The four types microwave integrated circuit were to be subjected to the high temperature storage tests, 1000 hours at 150°C or maximum process temperature, but not below 125°C. The tests were started on one type of circuit at 133°C chamber temperature. This was chosen because the lowest melting point solder had a solidus point of 145°C and it was felt that 12°C safety margin would be sufficient.

The chamber was a small one, without any windows, therefore the units were just left in there without regular visual inspection. About halfway through the test an inspector opened the door and found that solder was covering most of the module surfaces, in fact, it looked like the solder had reflowed, which was quite surprising knowing that the melting point of the solder was supposed to be a whole 12°C above the chamber temperature. After opening the unit it was found that another solder, having a melting point of 151°C had also flowed. Initial reaction was that the chamber must have overheated. However, investigation proved the chamber temperature to be rock stable. An investigation was then started to find the cause for the reflow. This investigation lasted over three months until it was finally established that tin or lead based Eutectic solders form a tertiary eutectic alloy with gold which has a lower melting point than the parent alloy. This solder then starts to creep even though the temperature is below the melting point of the solder, up to 40°C below the solidus point. Therefore different solder compositions were used on the new assemblies which successfully withstood the temperatures at high temperature storage, which is now limited at 125°C.

The high temperature burn-in (240 hours at 125°C or maximum safe junction temperature) presented a similar set of problems, on the two

amplifier units only, as these are the only ones which generate heat while operating. The maximum allowable junction temperature was known, as well as power dissipation, derating etc. so the maximum allowable burn-in temperature was established such as not to reduce the reliability of the units. However some units quit before the 240 hours limit was reached. Investigation discovered creep again, this time inside the circuit, the solder having come through some of the plated through holes, shorting out some components, and causing the failure. Semiconductor devices generated local hot spots which can reach particularly high temperatures if there are voids in the solder joint between the substrate and can. In order to eliminate voids, the process was modified and each unit was X-rayed. The solder composition was changed to ensure that creep will not occur.

CONCLUSION

Hybrid microwave integrated circuits have proven to be difficult to design, costly to produce and lengthy to test. However, there are good and valid reasons why they are required in a complex electronic equipment, therefore they are here to stay.

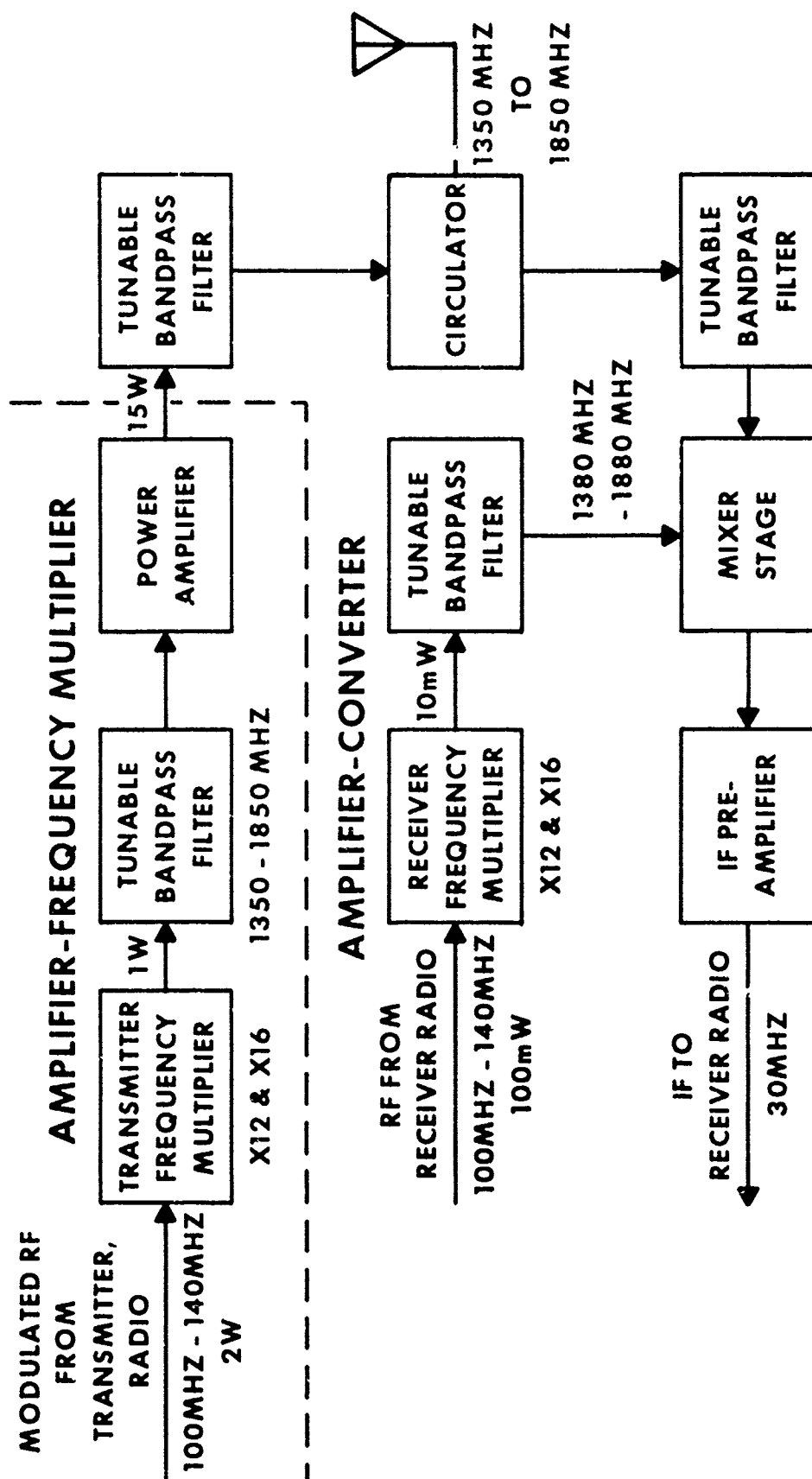


FIGURE 1
BAND IV TUNING HEADS, FUNCTIONAL BLOCK DIAGRAM

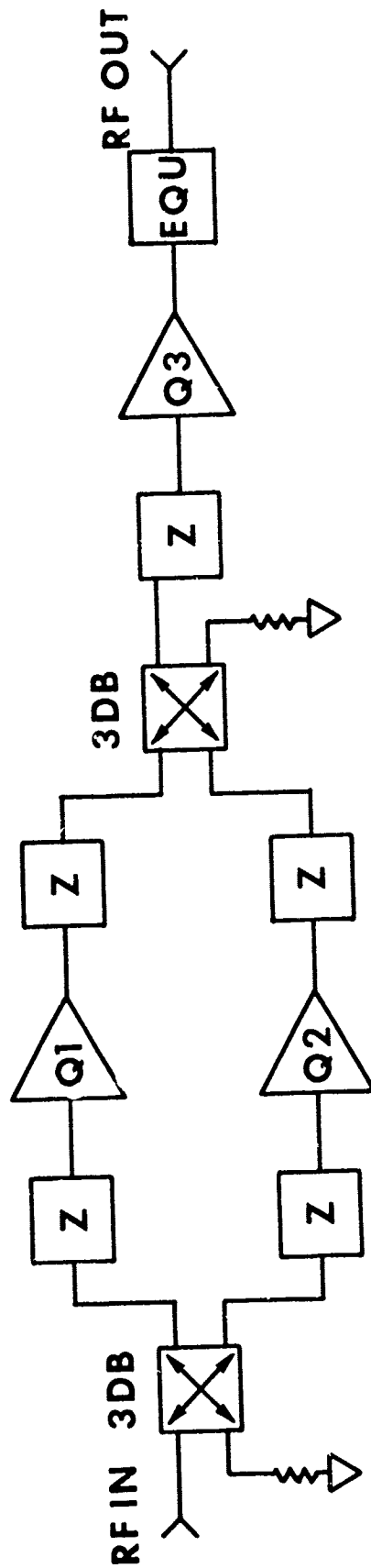


FIGURE 2
BROADBAND LOW NOISE AMPLIFIER
BLOCK SCHEMATIC DIAGRAM

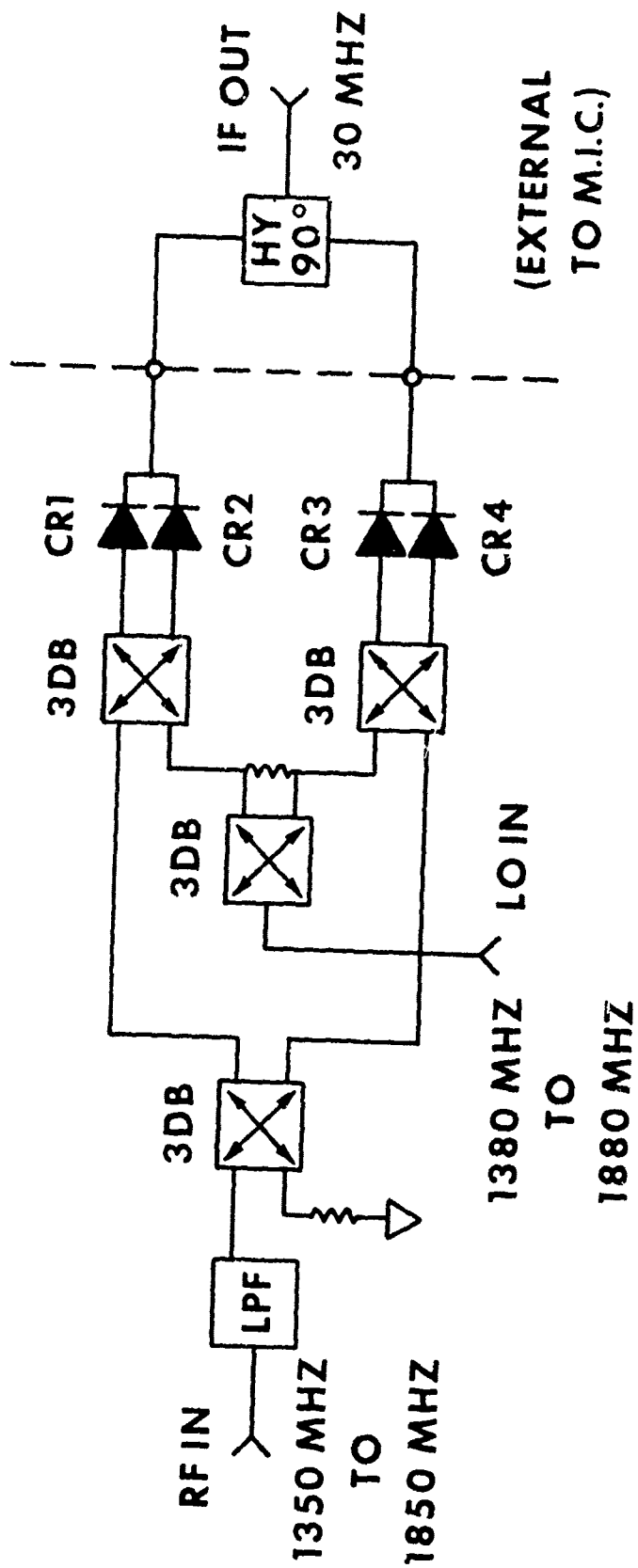


FIGURE 3
FREQUENCY CONVERTER BLOCK SCHEMATIC DIAGRAM

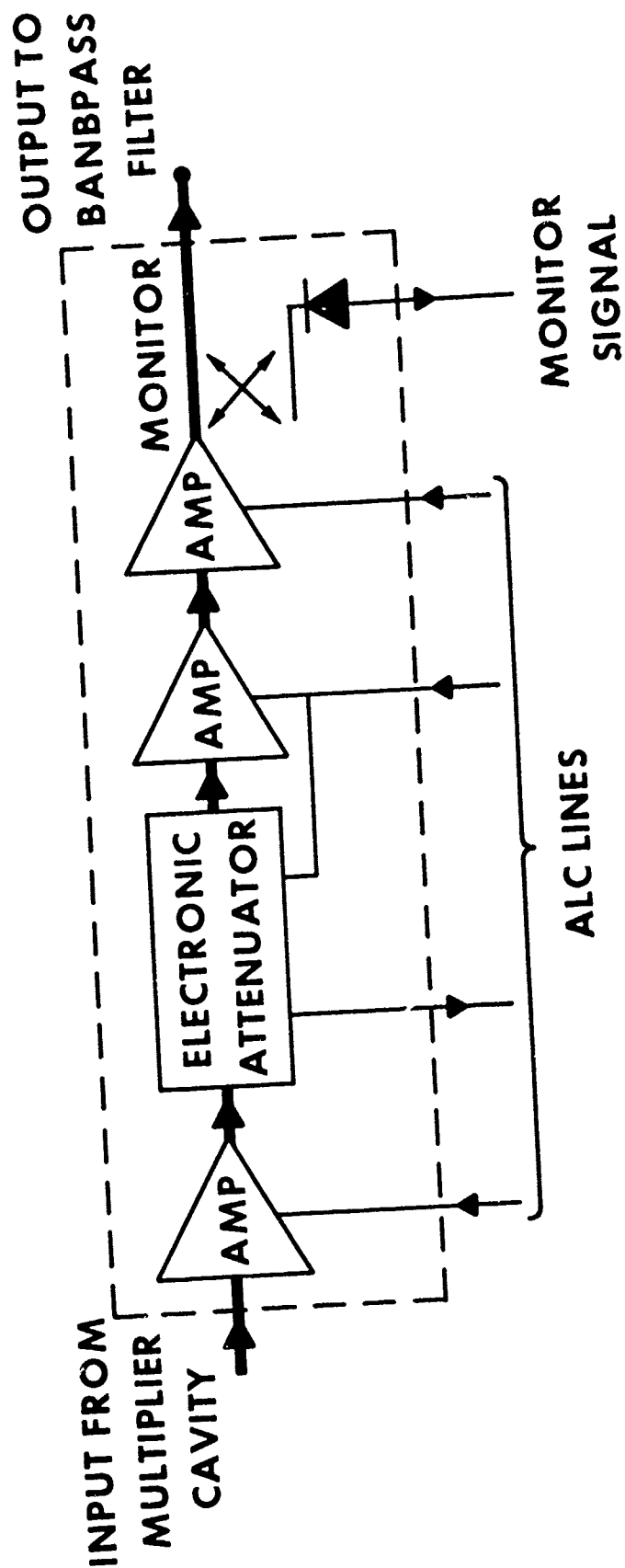


FIGURE 4
BLOCK DIAGRAM HIGH POWER AMPLIFIER

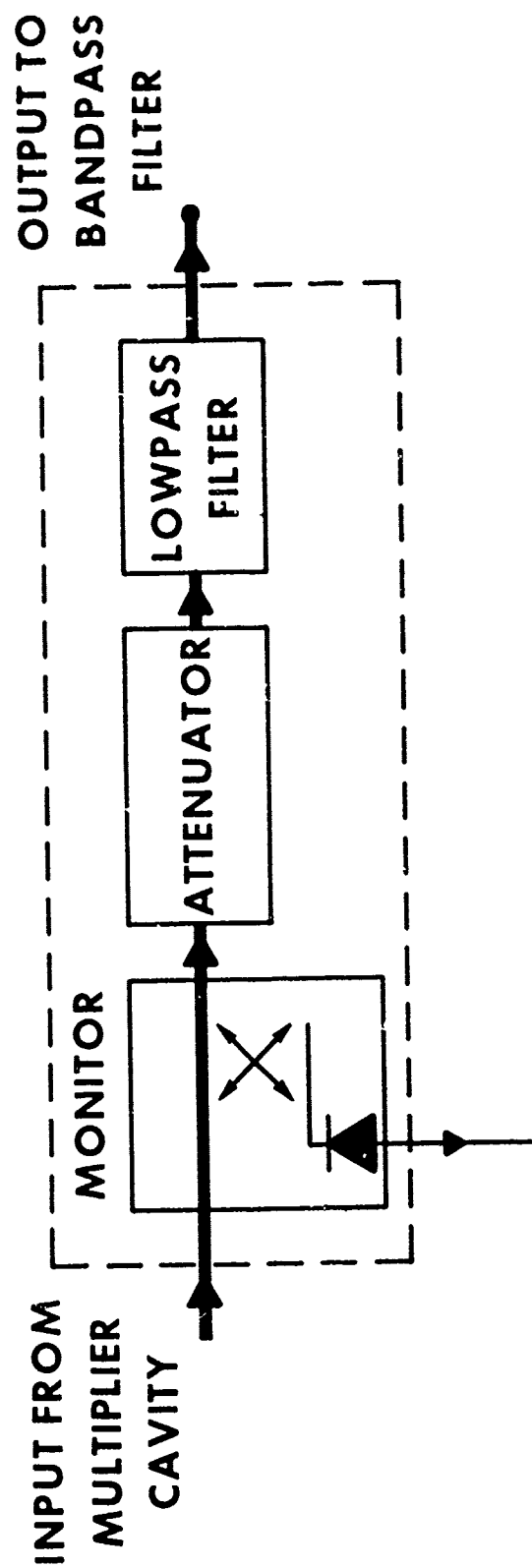


FIGURE 5
BLOCK DIAGRAM MONITOR AND ALARM CIRCUIT

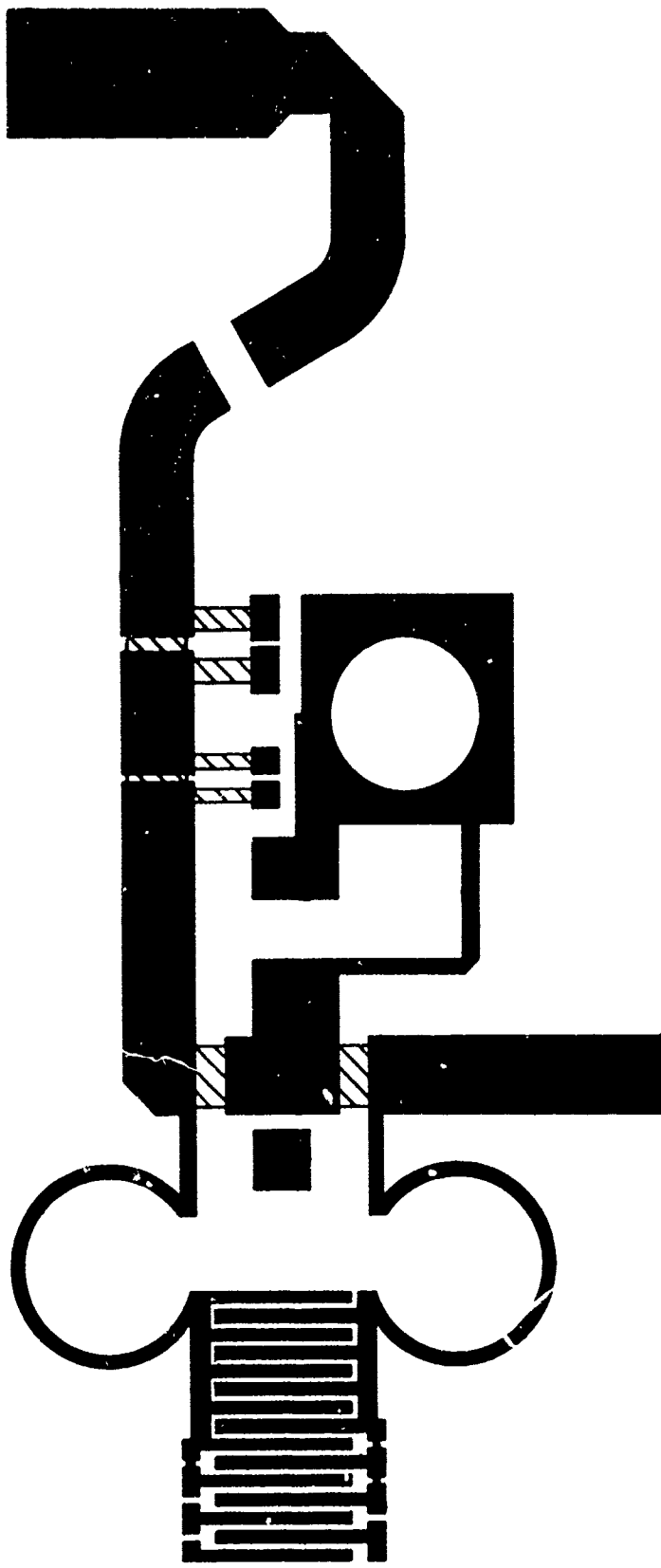


FIGURE 6
BROADBAND LOW NOISE RADIO FREQUENCY AMPLIFIER
SHOWING EQUALIZER PATTERN

HYBRID AND MIC PACKAGING DESIGN
FOR SHF SATELLITE COMMUNICATIONS TERMINALS

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Camden, New Jersey 08102

ABSTRACT

In a family of four SHF satellite terminals extensive use was made of advanced microelectronic packaging techniques. Thick film hybrid modules were utilized for circuits in the 10 kHz to 280 MHz frequency range. MIC modules using thin film techniques were utilized for the 700 MHz to 8.4 GHz frequency range. The thick film hybrid modules utilized component complexities ranging from several transistors to designs using a multiplicity of integrated circuits. These latter types could be classified as medium scale integrated (MSI) designs in their own right and required up to four levels of metallization to accomplish the required signal interconnection patterns.

INTRODUCTION

A family of engineering development models of SHF Satellite Communication Ground Terminals was developed by RCA under the sponsorship of the U.S. Army Satellite Communication Agency on Contract DAAB07-73-C-6084.

These terminals are highly mobile, lightweight ground terminals containing communication capabilities compatible with the DCCS II Satellite. Three of the terminals - AN/MSQ-59(), AN/TSC-85() and AN/TCS-86() - differ primarily in transmitting power output level, channel capacity, and equipment redundancy. The fourth terminal, AN/TSQ-118(), differs considerably from the three other configurations because of other functions that are required.

The design of all four terminals used common subsystems and or subunits to the maximum extent possible, providing a high degree of commonality between the

equipments and resulting in lower manufacturing and maintenance costs. Figure 1 shows one of the terminals in various positions; i.e., stowed for transport (left) and erected ready for operation (right). The drawers containing the electronics can be seen in the two views shown on the left.

The packaging of the electronics in all of the equipment was dictated by three primary factors:

- Field operational fault isolation from the equipment front panel without the use of external test equipment.
- Minimum cost, size and weight of replaceable assemblies.
- Minimum number of interconnections and manual wiring operations for high reliability.

A blend of construction techniques were employed to achieve the overall required equipment package size, weight, maintenance features, and manufacturing costs.

This paper will discuss two of the replaceable module designs used in the construction of the equipment. Both module designs and all circuit designs were developed by RCA for use in the SHF Satellite Terminals prior to the award of the Government contract.

The first is the thick film hybrid modules which were used in selected circuits in the UHF and lower frequency analog and digital circuits. Fifteen different circuit designs using this construction were packaged in this equipment. A typical example of one of the applications is shown in Figure 2. This plug-in subassembly contains five hybrid modules mounted on a printed circuit board with the other components. It can be seen that the hybrids were implemented only to the extent required to realize an economical packaging density. The hybrid module can be identified as the five largest packages on the subassembly.

The second module design was for selected circuits in the frequencies between 0.60 and 8.4 GHz. These microwave integrated circuits (MIC) modules used thin film microstrip construction techniques.

In the selection of the circuits for MIC designs, consideration was given to the modulization of desirable field maintenance features as well as reducing the RF connector and cable interfaces which impact reliability and cost. Four MIC designs were used in the various equipment. An example of the SHF Up-Converter MIC is shown in Figure 3. This MIC module contains four MIC components.

THICK FILM HYBRID MODULES

A. Module Dissipation

The four configurations of the engineering development model terminals used fifteen basic hybrid module types. The modules description and frequency of operation is shown in Table I. Quantities of up to 80 modules of one type were fabricated.

TABLE I

THICK FILM HYBRID MODULE TYPES

<u>CIRCUIT TYPE</u>	<u>FREQUENCY</u>
Wide Band Amplifier with AGC	50-200 MHz
Analog Phase Comparator	1 MHz
Lock Detector	1 MHz
Frequency Multiplier	20 to 180 MHz
Frequency Multiplier	5 to 20 MHz
A/D Converter	9.8 Mbps
20/1 Frequency Divider	20 MHz
20/1 Frequency Divider & Sweep Generator	30 MHz
40/1 Frequency Divider	5 MHz
200/1 Frequency Divider	250 MHz
500/1 Frequency Divider	5 MHz
Programmable Divider	35 MHz
Programmable Divider	60 MHz
Programmable Divider	200 MHz
Programmable Divider	300 MHz

B. General Packaging Philosophy

1. Partitioning

The partitioning of the circuits for packaging using thick film screening technology involved circuit designs of both analog and digital circuit types. The packaging of this circuitry for the SHF equipment in the UHF frequency range and below involved the partitioning of drawers and sub-assemblies for maintenance and reliability consideration and the subdividing of the subassemblies for hybrid module packaging.

As mentioned previously, circuitry was included in the hybrids only to the extent necessary to achieve the individual subassembly packaging density. This was compromised in some instances to standardize circuit functions used in multiple applications.

All hybrid types used the custom seal design to make optimum use of the "real estate" allocated for packaging. In this way compromises could be made on the subassemblies between the conventional component parts mounted on the printed circuit board and the hybrid size without being limited by the availability of conventional packages. A discussion of the custom sealing technology is being presented in another paper entitled "Packaging Design for Army Tactical Radio Set AN/URC-78" and the details are not repeated here.

2. Electrical Design

Referring to Table I, it can be seen that most of the circuits operate at fairly high frequencies which required some additional features to be incorporated into the custom seal design which may not be necessary for lower frequency operation. The higher frequency of operation makes the circuits more sensitive to capacity loading. Also the designs can be more susceptible to variations from unit to unit because of variations in this capacity.

For instance in the digital design, the sharp rise of the pulses can couple into other parts of the circuitry giving faulty signal indication. Careful layout with the proper decoupling is required to prevent this from happening. In addition several of the designs required back plane metallization to provide shielding of the circuitry from outside interfering signals and to stabilize the circuit capacity.

As an additional capacity consideration the seal ring metallization and the hermetic cover in all the designs were connected to circuit ground. This minimized the coupling capacity on adjacent I/O lines under the seal ring metallization. Figure 4 shows this effect with and without grounding of this seal ring.

3. Mechanical Design

The hybrids were designed with I/O terminals made of copper, .025 inches in diameter that were thermc-swaged into holes provided in the substrate. Figure 5 shows the method of attachment of the terminal to the substrate. The module terminals were soldered to plated-through holes on the equipment printed circuit boards.

As can be seen in Figure 5 the back plane metallization was connected to the circuit ground either by a conductive metal wrap around the edge of the substrate or by using a termination pin to interconnect the grounds on two sides of the substrate. Both techniques were used in the designs.

Ten of the designs used a kovar metal cover over the complete substrate in which case the terminals were brought out as shown in Figure 5A. The leads of the terminals were soldered to the circuit metallization to provide for hermetic sealing of the terminals. Figure 6 shows the Wide Band Amplifier module which used seven I/O terminals constructed in this manner.

Five of the designs used a cover over only parts of the substrate. In this case metallization patterns for the input and output connections were brought out under the seal metallization to the substrate edge where the I/O terminal was located. This design is shown in Figure 5B.

This latter design is preferred since higher yield for hermeticity is realized with the I/O leads brought out under the seal metallization.

4. Components

The variation in the electrical performance requirements of the various designs dictated a wide variation in the parts used in the designs. The semiconductor types varied from simple diodes to complex integrated circuits. Capacitors were from a few picofarads to 30 microfarads for decoupling purposes. Resistor values had the same large variation from low ohm values to megohms.

The most complex designs used four layers of metallization and up to 11 total screens were required for these designs.

Figure 7 shows a typical hybrid of the more complex type. Also shown is a list of the components used in the hybrid.

MIC MODULE DEVELOPMENT

A. Module Description

There were four MIC module types employed in the engineering development model terminals. These four MIC modules are:

1. SHF Mixer Coupler Module

The SHF mixer coupler module integrated seven (7) individual circuit elements into one module. These elements are shown in Figure 8 with photograph of the unit with the cover removed. The module was divided into two chassis such that the two halves could be pretested separately before final assembly. Provisions were incorporated to install SMA connectors at the interface of the two chassis for testing as shown in Figure 9. This concept was applied to the SHF up-converter module as well. In the manufacture of complex MIC modules, this assembly technique allows for the optimization of the component parameters of each circuit for maximum yield prior to the overall module integration. Subsequent production units could be manufactured as a one piece chassis to reduce cost.

A total of 50 of these modules were produced for the EDM equipments.

2. Spectrum Generator Power Divider

The power divider module integrated three individual circuit elements as shown in the block diagram and photograph of Figure 10. Again, 50 modules were produced with minimum problems.

3. SHF Up-converter

As mentioned previously, this module was also separated into two halves and had six individual circuit elements as shown in Figure 11. Due to the extremely tight specifications on the flatness of the passband response, the LO input VSWR, and the output VSWR at the output port, it was found that the testing of the up-converter portion of the module by itself to be extremely valuable during the manufacturing of the EDM modules. A total of 25 of these were manufactured for the EDM equipments.

4. 630 MHz Amplifier

This module, since it was in the lower end of the MIC band, was relatively trouble free and was the simplest module from the circuit design and contained two circuit elements. 50 of these units were produced for the equipment. This design is shown in Figure 12.

B. General Packaging Philosophy

1. Chassis

All of the chassis were milled out of brass stock and gold plated. It was found that at X-Band and higher frequencies, the continuity of ground current was extremely important to reduce circuit losses and to ensure proper electrical performance of the circuits. The internal part of the chassis has rather complex configurations because:

- a. The thicknesses of the substrates were different (e.g. 50 mils for ferrite and 25 units for ceramic).
- b. Ground pads were brought up to be planar with the substrates for the 50 ohm chip resistors used for terminations.
- c. Wells were milled out at the bottom side of the chassis for the magnets used for the isolators.
- d. Holes on the interface sides of the modules with two chassis for installing SMA connectors for testing.

2. Electrical Design

No tight tolerance specifications were imposed on the purchased microwave semiconductor devices in order to minimize the cost of the devices. To take into account the normal variations of the parameters of the devices, worst case parameters were used throughout the design. This proved to be extremely worthwhile to minimize testing time and circuit optimization required during the manufacturing phase.

3. Substrates

Chrome-copper-gold metallizations were used for the substrates. This eliminated detrimental scavenging of the gold by the tin/lead solder. In subsequent repairs, no damage was experienced when the modules had to be disassembled for repair.

4. Components

All of the semiconductor components used were commercially available hermetically sealed devices which precluded the requirements for the complete modules to be hermetically sealed. Microwave chip resistors were used for terminations of the isolators and couplers. This represented a sizable cost saving as compared to the using of external terminations through connectors. Carbon resistors were used in the bias circuits of two of the modules to provide a design tolerance variable (DTV) for adjusting the transistor bias current.

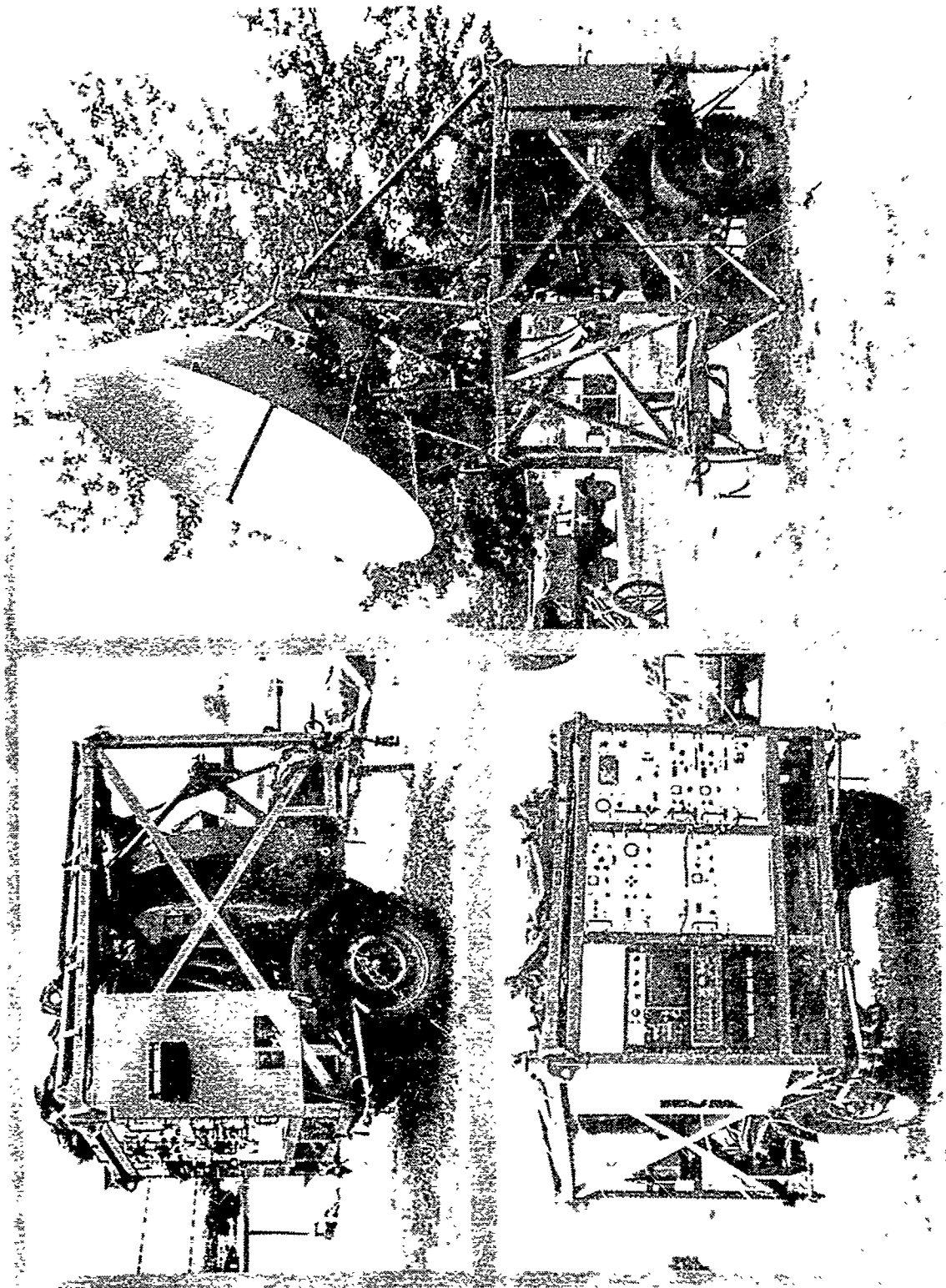


Figure 1. Terminal in Transport (Left) and Operating (Right) Configuration

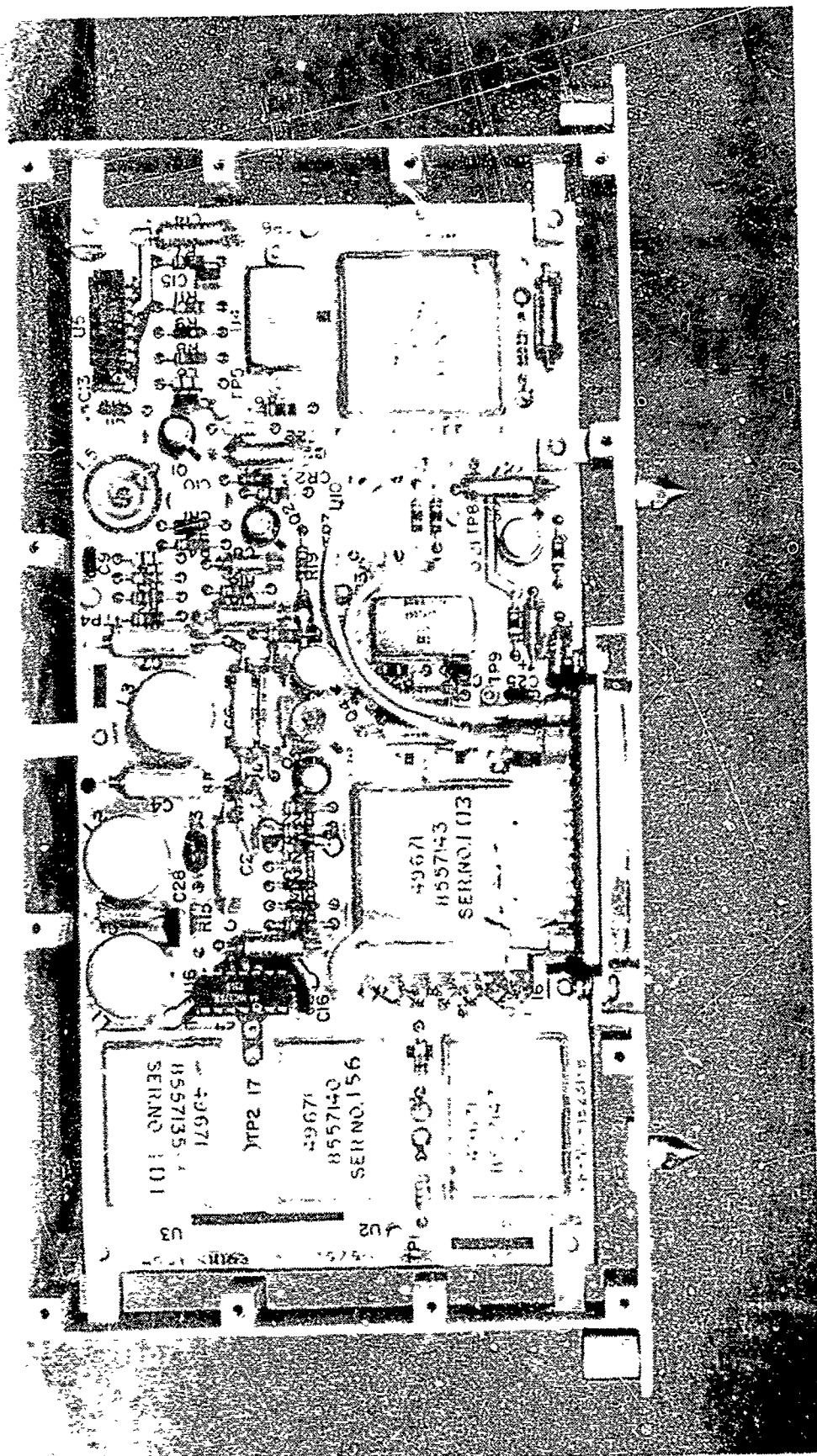


Figure 2. Typical Subassembly Containing Thick Film Hybrid Modules

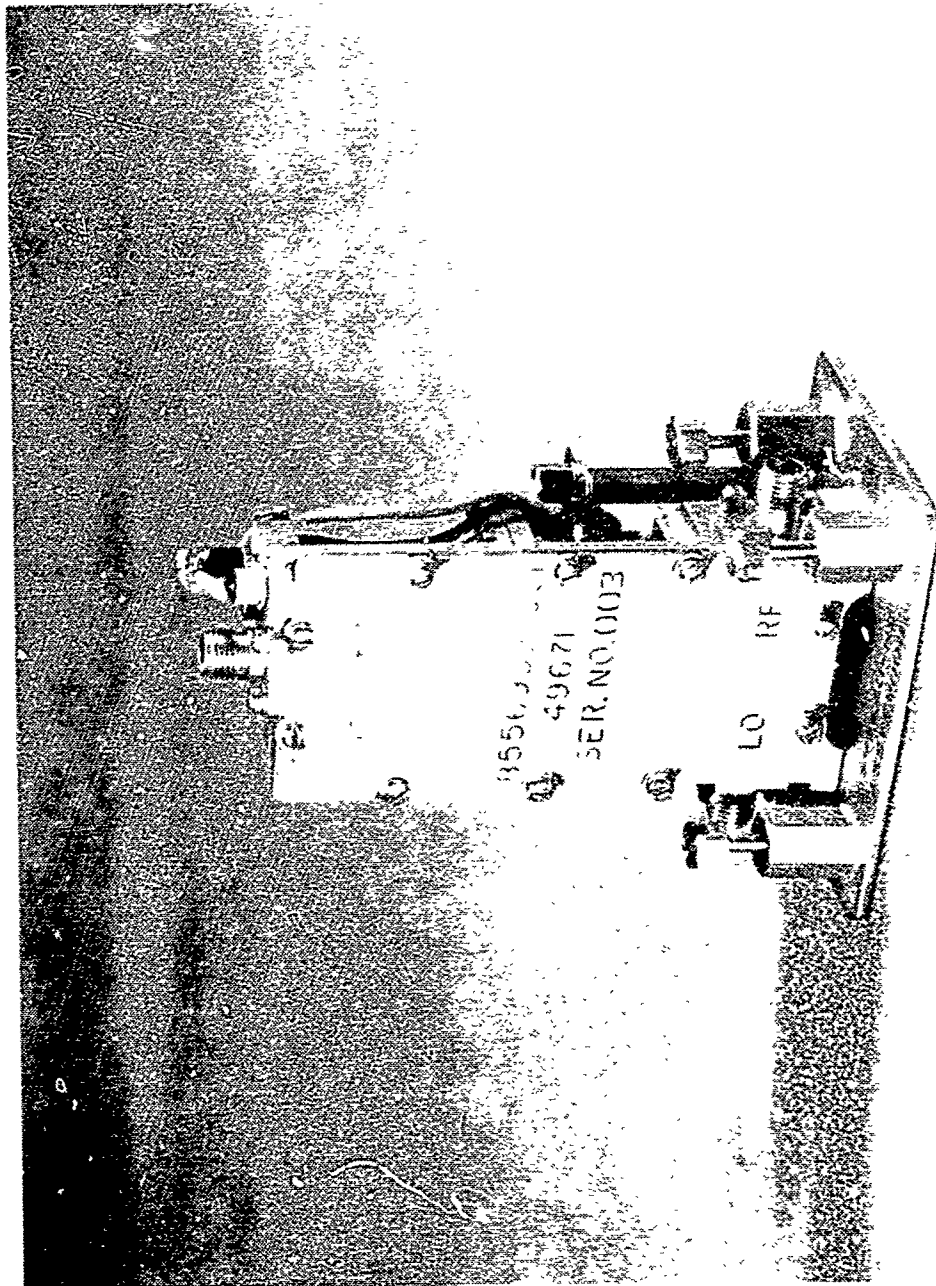


Figure 3. SHF Up-Converter MIC

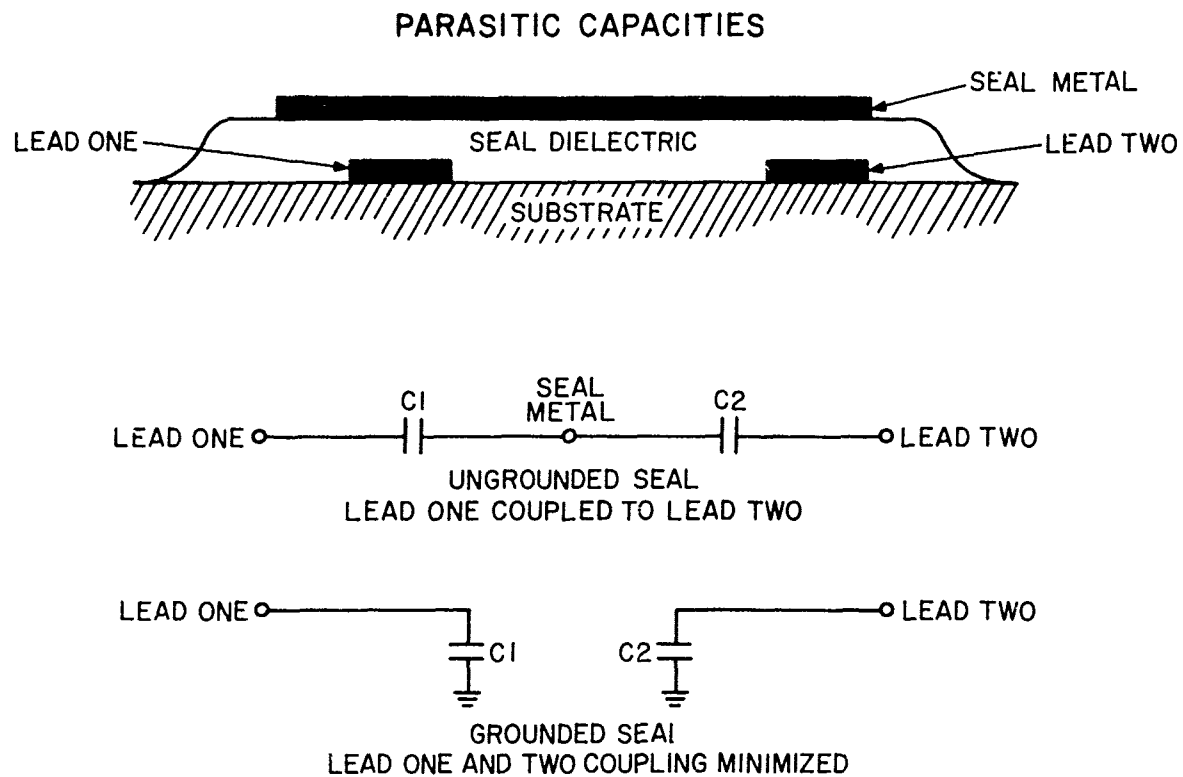
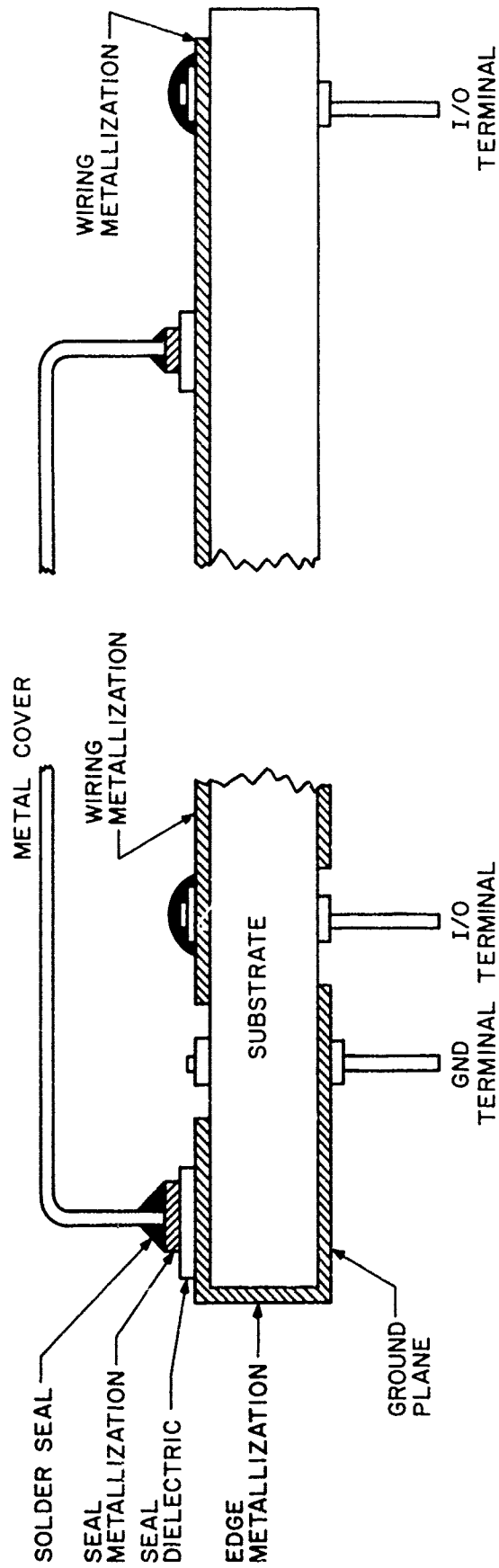
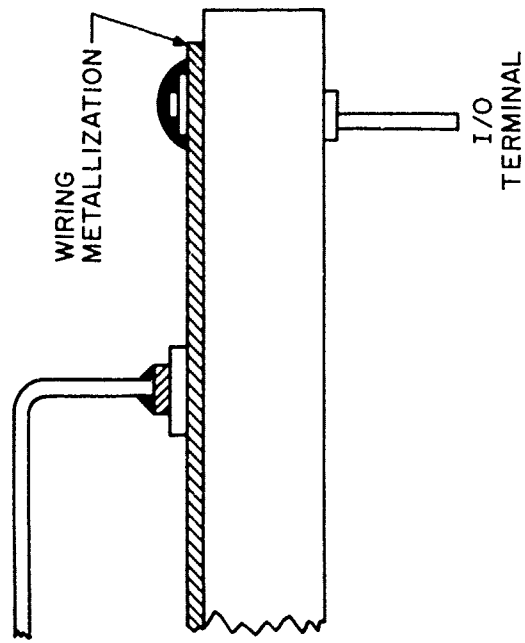


Figure 4. Parasitic Coupling Capacities



A



B

Figure 5. Standard Custom Seal Hybrid Module

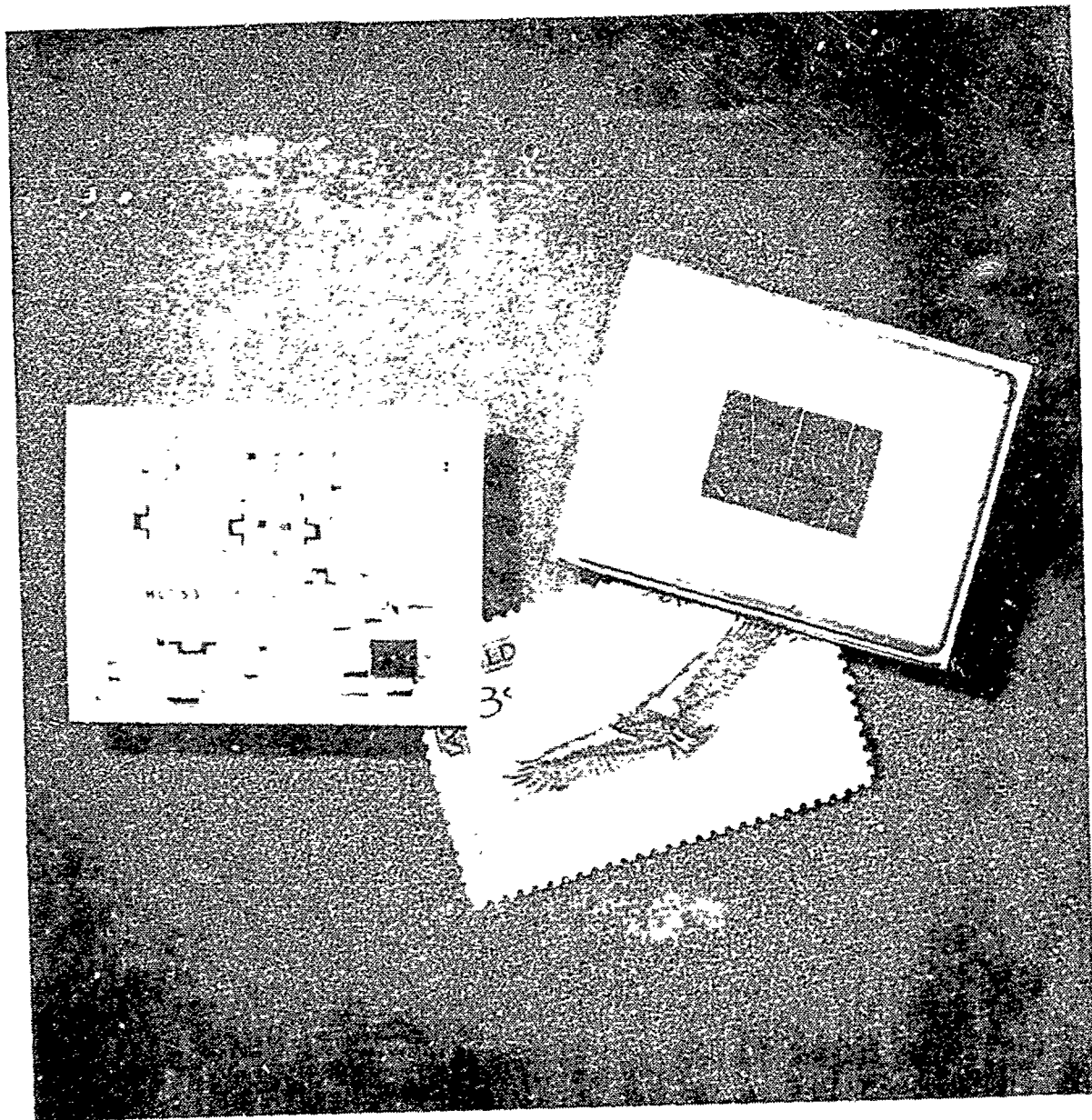


Figure 6. Wide Band Amplifier with AGC

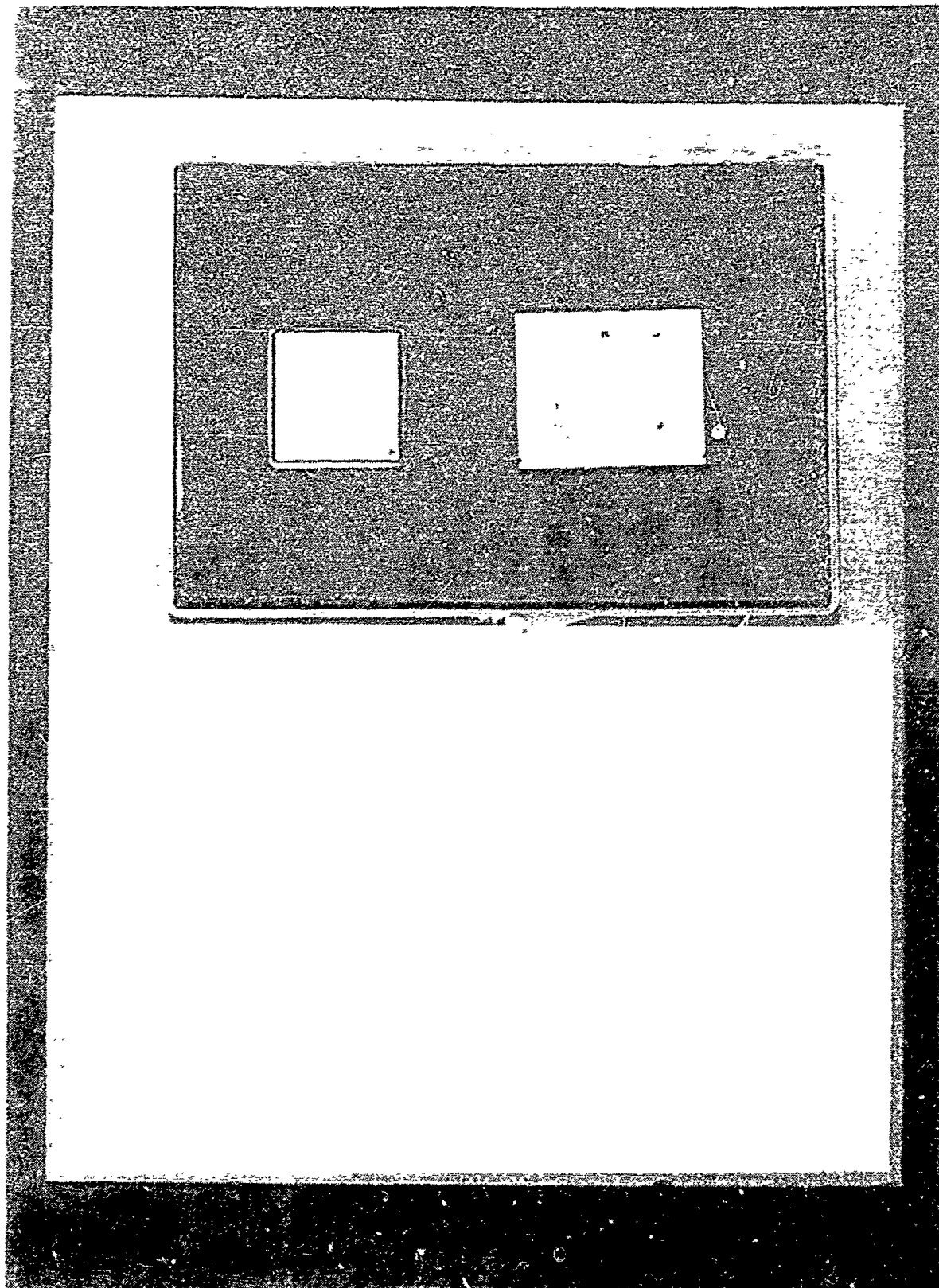
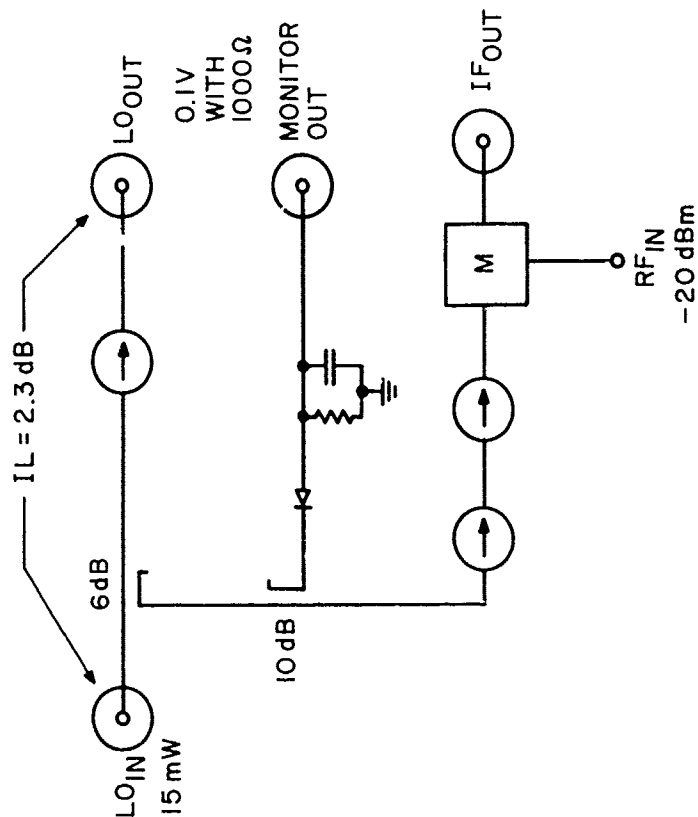


Figure 7. 200 MHz Programmable Divider



ISOL. (RF_{IN} TO LO_{OUT}) ≥ 50dB

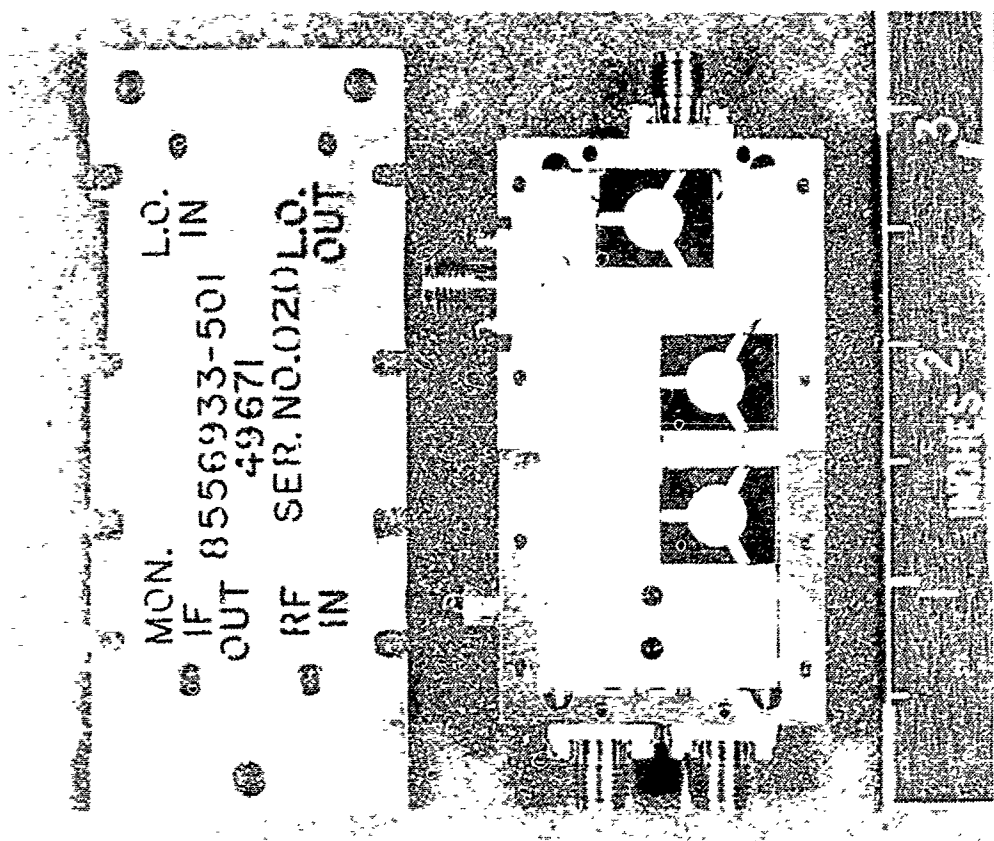


Figure 8. Mixer Coupler 6.4-7.6 GHz/100-200 MHz

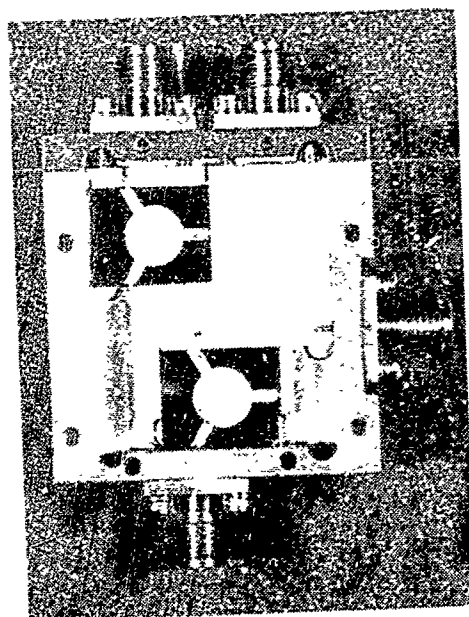
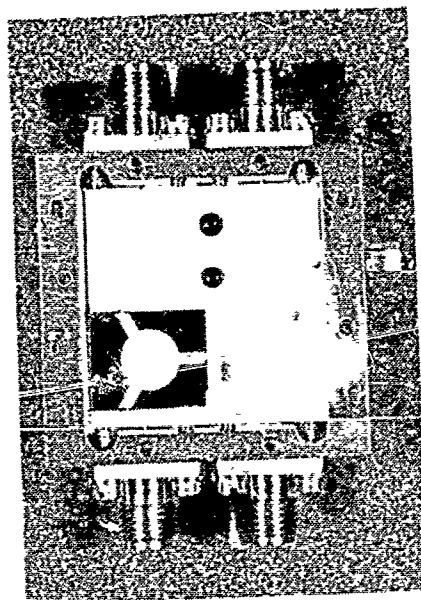


Figure 9. Subassembly Test Fixture

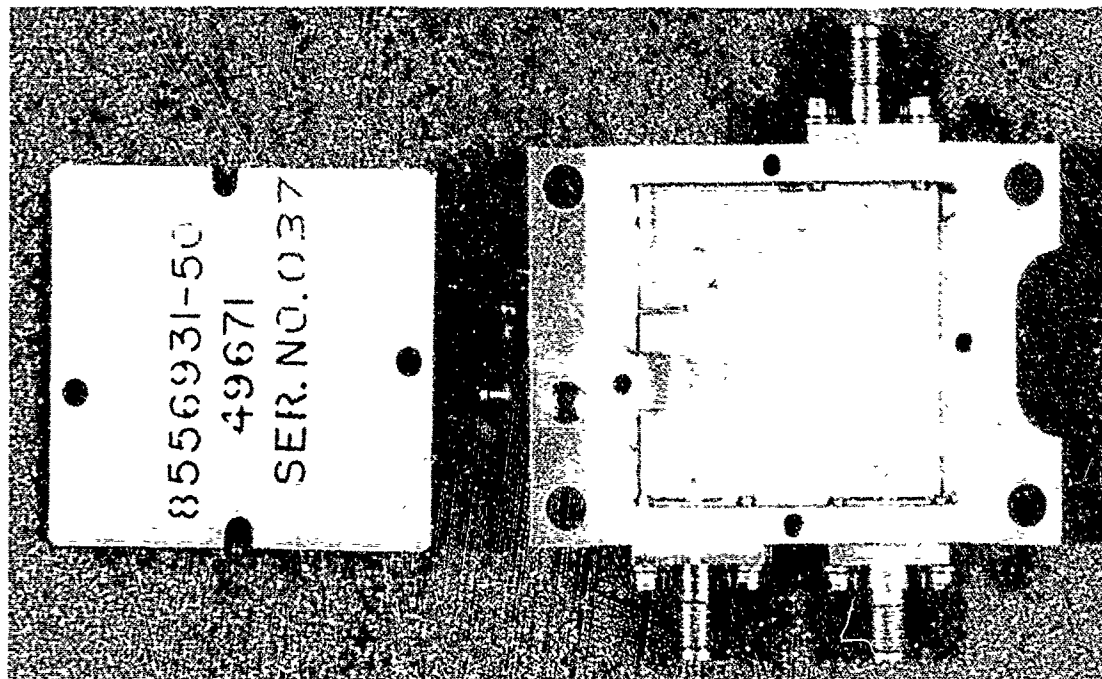
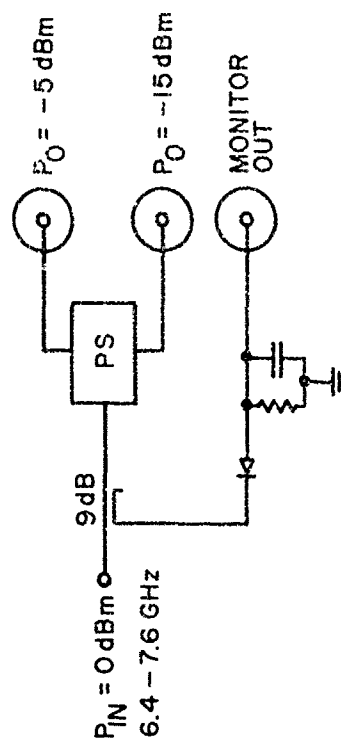


Figure 10. Spectrum Generator Power Divider - 6.4-7.6 GHz

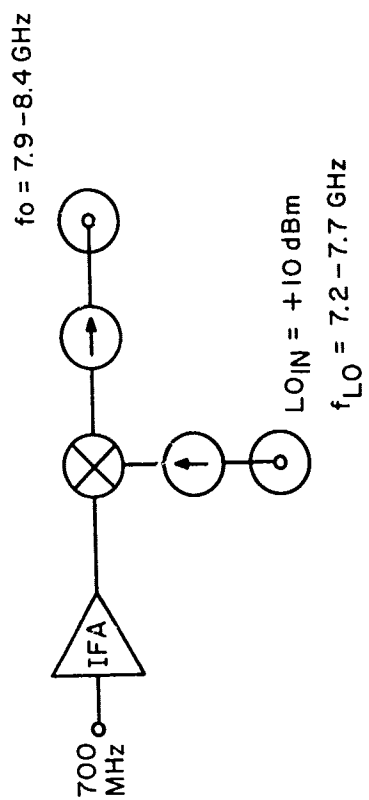
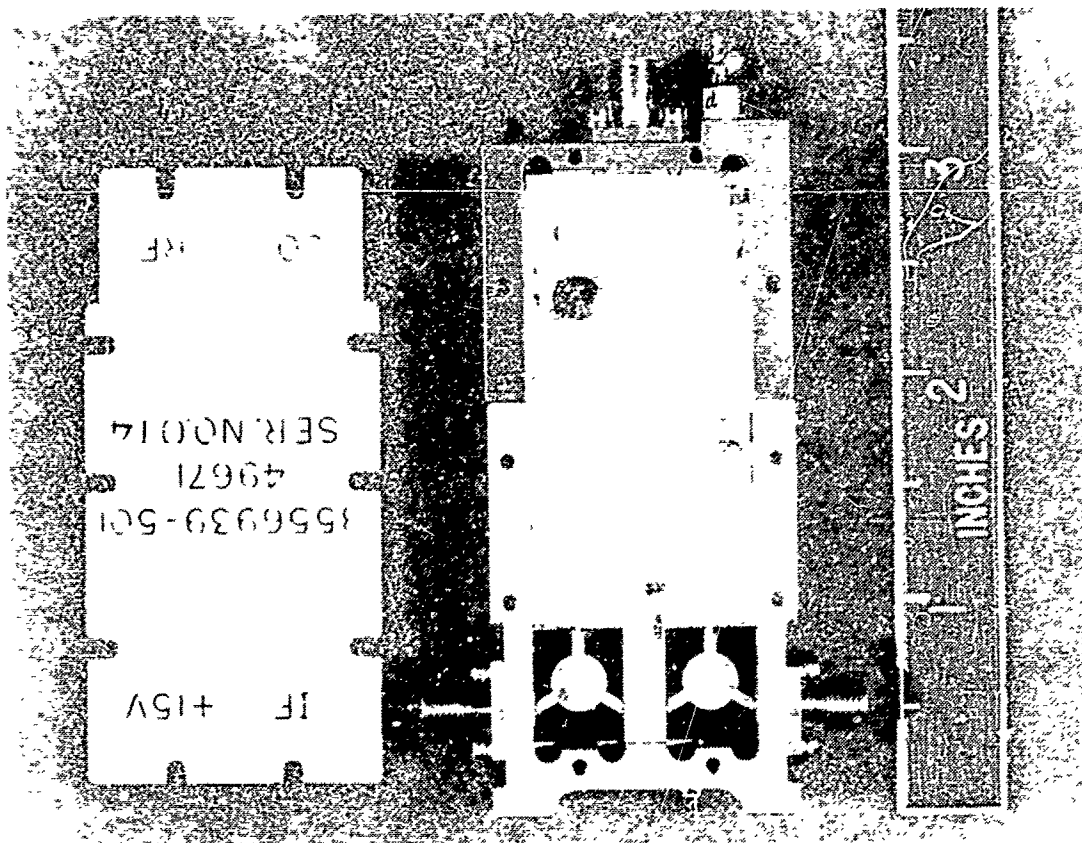


Figure 11. SHF Up-Converter 700 MHz/7.9-8.4 GHz

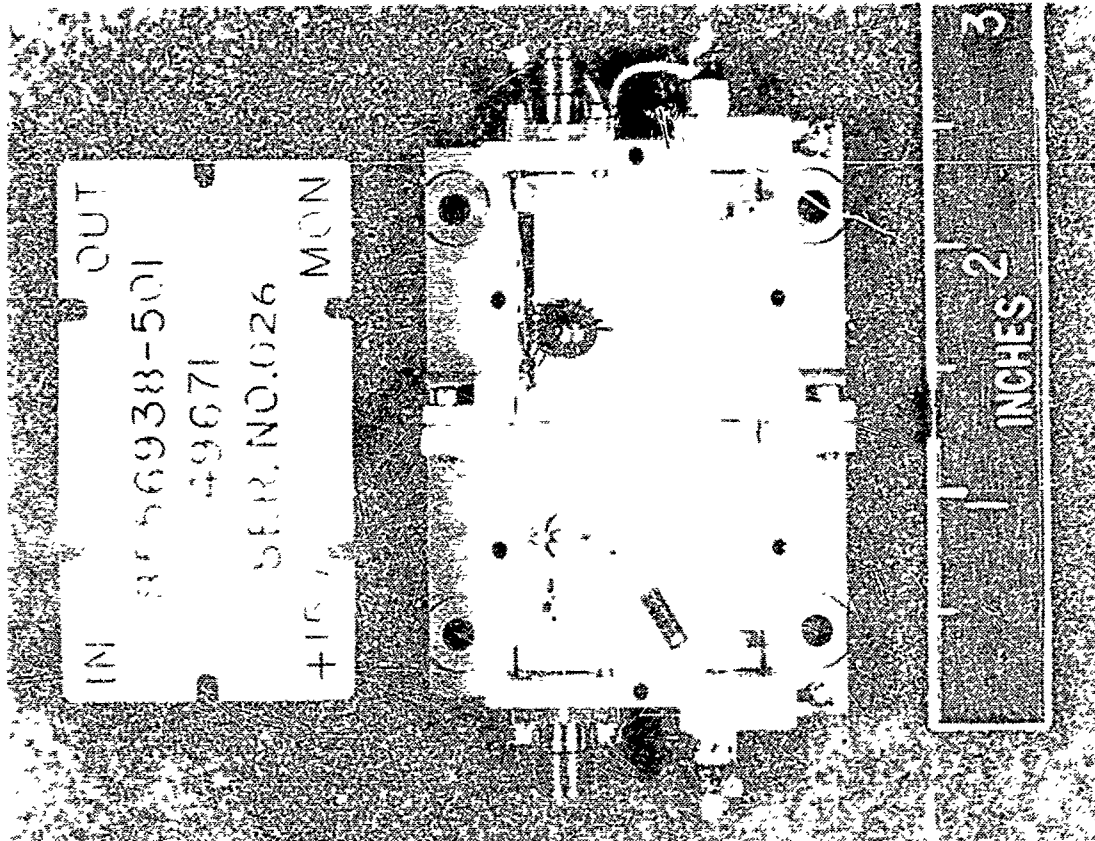
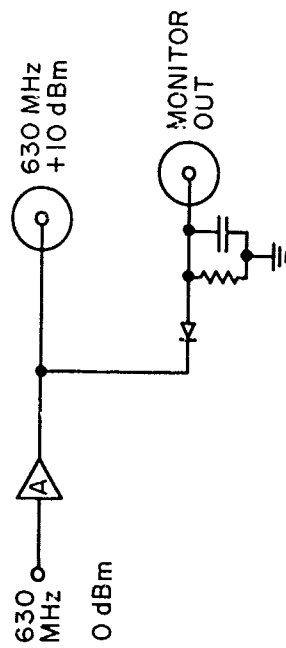


Figure 12. 630 MHz Amplifier

THE APPLICATION OF HYBRID MICROELECTRONICS TO THE IMPROVED TD-206 PULSE
FORM RESTORER

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ABSTRACT

Hybrid microelectronics technology has been successfully applied in the development of an improved TD-206 Pulse Form Restorer so as to enhance reliability and performance. Improved reliability was achieved through the use of beam-lead devices, multilayer thick film conductors and integral resistors, while the high density packaging permitted added circuitry for electrical design improvements.

Essentially all of the active circuitry of the new TD-206 B/G is contained in a hermetically-sealed hybrid microcircuit module. The module consists of a two layer thick film metallized substrate on which are deposited 60 integral thick film resistors and 63 attached chip components. The chip components consist of beam-leaded transistors and diodes, chip-and-wire diodes, ceramic and tantalum chip capacitors and chip inductors. Epoxy adhesives are used to attach all non-beam leaded components to the thick film substrate and the substrate to the base of a 32-pin metal platform package. The package is hermetically sealed by soldering.

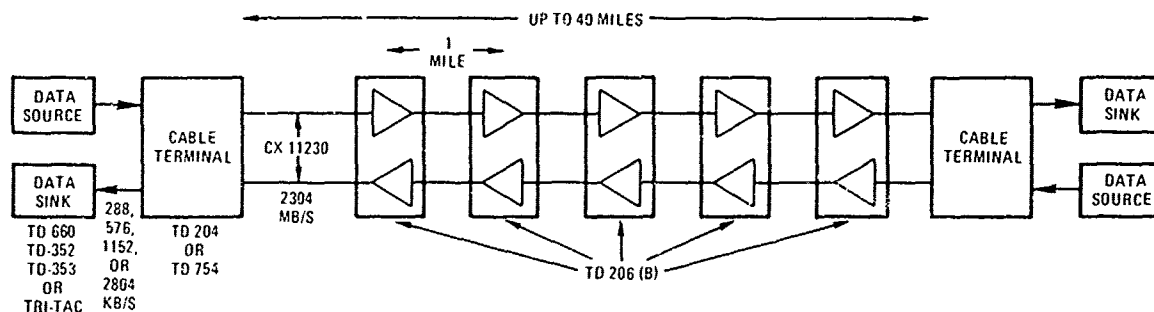
Several assembly and packaging processing problems had to be resolved during the development of the hybrid microcircuit. Some of the chip capacitors and inductors were only available pretinned with solder. These components could not be reliably attached to the substrate with epoxy, and a new attachment technique was developed. The requirement for a hermetically-sealed package coupled with a requirement that no flux could be sealed in the hybrid created a serious challenge. A technique was developed that insured no flux entrapment and did not expose the package contents to temperatures exceeding 150°C.

The completed hybrid microcircuit module was subjected to MIL-STD-883, Class B screens consisting of pre-cap visual inspection, temperature cycling, mechanical shock (drop test), burn-in, hermeticity and functional electrical testing.

The improved reliability, ruggedness, and overall performance has been demonstrated by laboratory and field tests. An order of magnitude improvement in MTBF has been exhibited.

INTRODUCTION

The TD-206 B/G Pulse Form Restorer, developed and produced by Raytheon Company, Equipment Division, is a result of an Army product improvement program on its predecessor, the TD-206/G, to improve the latter's reliability and ruggedness. The TD-206 is used as an unattended repeater, at one-mile intervals in a two-way pulse code modulation cable transmission system. The TD-206 restores the original amplitude, wave shape and timing of a PCM signal, transmitted in either direction. A maximum of 39 TD-206's may be used in a cable link between repeaters/terminals to provide up to a 40 mile system. This system is shown schematically in Figure 1.



TD-206B/G in Typical System Configuration

Figure 1

The function block diagram for the repeater (1-way) is shown in Figure 2.

The improved TD-206 had a 50,000 hour MTBF objective and a 20,000 hour MTBF specification, as compared to the MTBF of approximately 6000 hours for the presently fielded TD-206/G. Raytheon's approach to meeting the reliability and ruggedness objectives focused on the maximum utilization of hybrid microelectronics technology to achieve these objectives. As additional benefits the use of hybrid technology results in minimum size, weight, and cost and permits added circuitry for electrical design improvements. Consequently, essentially all of the active circuitry for the new TD-206 is contained in hermetically-sealed hybrid microcircuit modules. Two identical hybrid modules are used per TD-206 unit, one for each of the two ways of transmission. The block diagram for the electronics contained in each hybrid is shown in Figure 3. The microcircuitry includes the following circuit functions: preamplifier, threshold circuit, phase splitter, clock driver, phase shifter, sampling flip-flop, output amplifier, and solid state switch.

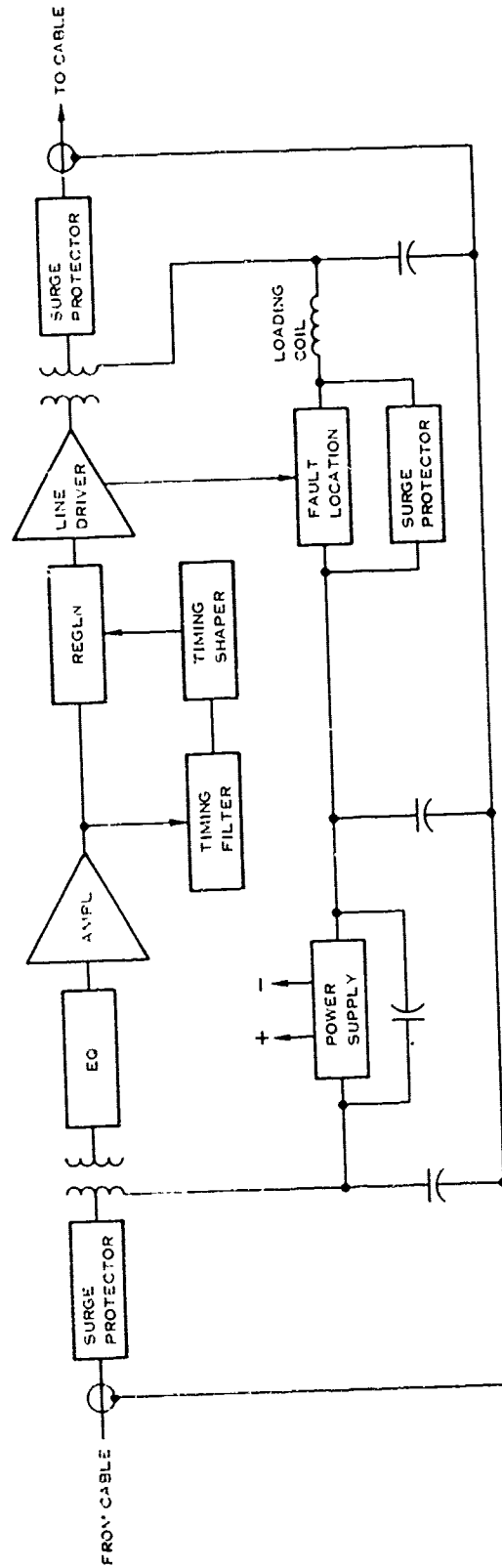


Figure 2. Repeater Block Diagram (One Way Shown)

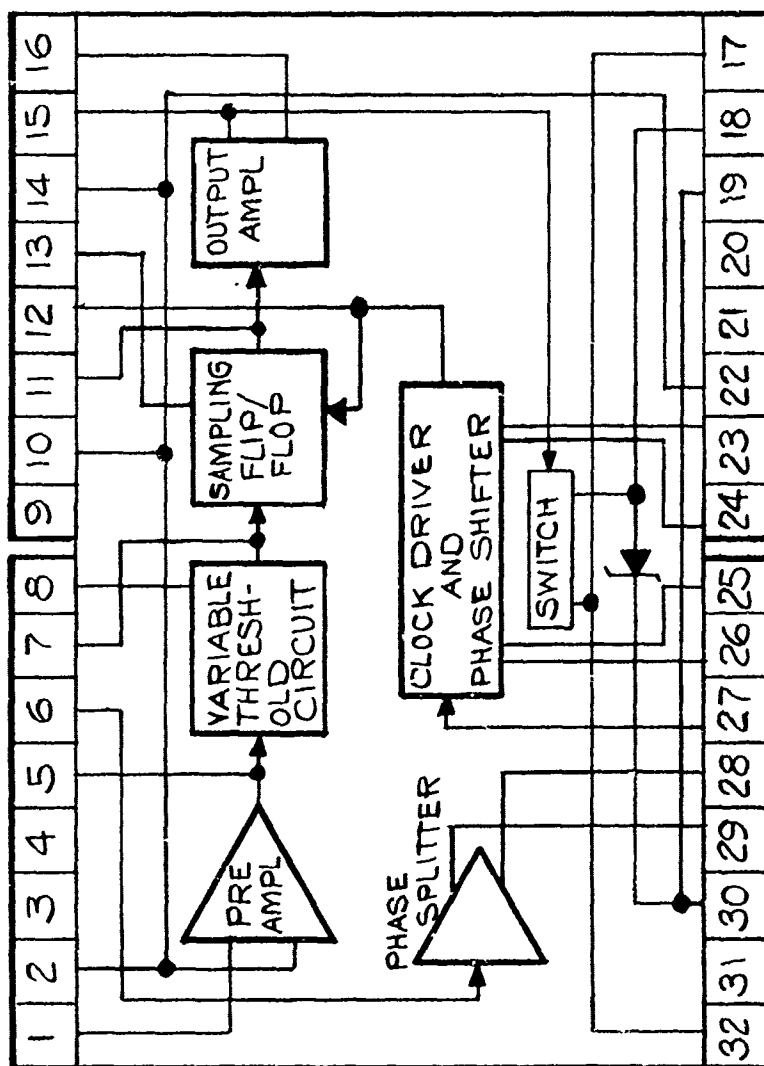


Figure 3. Block Diagram of Electronics

PHYSICAL DESCRIPTION

Physically, the hybrid module consists of a two layer thick film gold metallized substrate on which are deposited 60 thick film resistors and 63 attached components. The substrate is 95% Alumina, with dimensions 2.16" x 1.07" x .025". The chip components consist of 19 beam-leaded transistors, 3 beam-leaded junction diodes, 4 beam-leaded hot carrier diodes, 23 ceramic chip capacitors, 8 tantalum chip capacitors, 2 chip-and-wire bonded diodes, 1 axial-leaded diode, and 3 chip inductors. The package is a gold plated Kovar, 32 pin platform-style package with outside dimensions of 2.3" x 1.4" x .5". Figure 4 is a picture of the assembled hybrid.

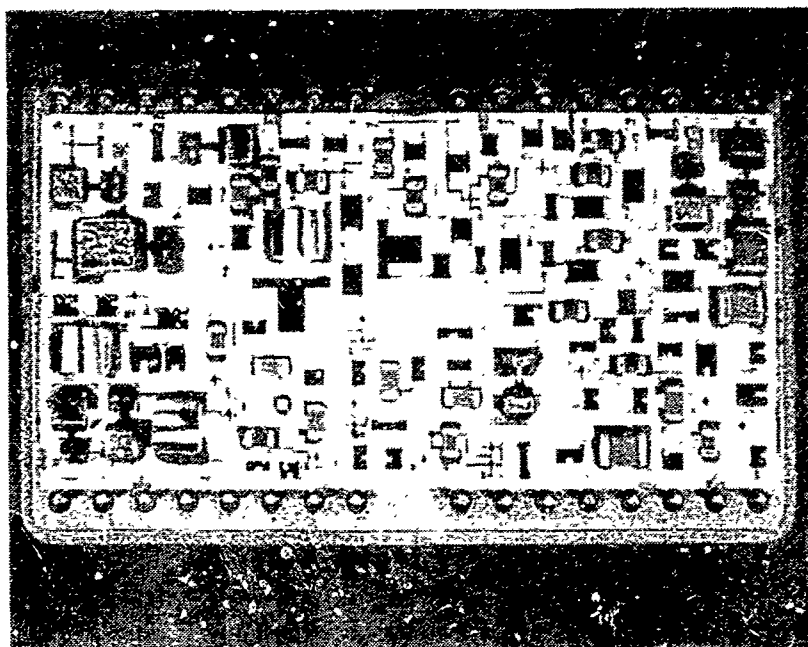


Figure 4. TD-206 Hybrid Assembly

DESIGN CONSIDERATIONS AND PROCESSING

One of the fundamental design considerations was the type of hybrid that was best suited to meet the program objectives. In large production a monolithic approach perhaps would have been more cost effective, but this type of approach was not compatible with the electrical design and was not pursued. A thick film approach was chosen because it was the most cost effective in large production of all the hybrid technologies.

The manner in which the components would be attached to the substrate was the next consideration. Use of integral thick film screened and fired resistors eliminated 120 interconnections which would have been required if discretes had been utilized. In addition, the weight and size were minimized by eliminating discrete resistors and production cost was lowered because of the batch processing of the resistor-conductor networks. The decision was made to use beam-leaded devices wherever possible. The reasons for this choice were as follows. Data available indicated that beam lead bonding was at least as reliable as the alternative chip-and-wire joining technique. The improved reliability resulted mainly from the elimination of the critical wire bonding of device interconnections, from the hermetically sealed junctions due to the silicon nitride surface passivation, from the bonding stress being placed only on the leads and not the chip, from the higher component packaging densities which could be achieved; and from the ability to assess the bond quality by visual inspection. In addition, Raytheon as a vendor of beam lead parts would have the ability to properly control the quality of the beam lead device supplied to the program. Beam leads were also judged to be more cost effective in large production quantities because of the following factors which influence assembly cost:

- . Elimination of separate die and wire bonding operations
- . Simultaneous bonding of all leads on a device
- . Applicability to automated chip handling and bonding operations
- . Increased circuit yield due to relative ease of device replacement when faulty.

Three active devices which had been specified in the electrical design were not available in beam lead form. Two of these devices were diodes which were available in chip form. It was decided that they would be die bonded and wire bonded with .001" 99% Al, 1% Si wire. In later production these devices would be available in beam lead form. The third device, also a diode, was selected in axial lead form because the chip was not conventionally wire bondable, and the other configuration in which it was available (i.e., LID) consumed too much substrate area.

The attachment of chip capacitors and inductors was a major concern. Raytheon internal reports¹ and the work reported by others² seriously questioned the reliability of ceramic capacitors attached by means of solder because of failures during thermal cycling. Raytheon's experience with capacitor mounting indicated that with the proper choice of epoxy and processing controls, epoxy attached capacitors would be at least as reliable as those attached by solder. In addition, the use of epoxy was more cost effective and greatly increased the repairability of the module. The decision was made to use conductive epoxy. The epoxy chosen was Epo-Tek H44, a solvent-free, single-component epoxy specifically designed for use in microelectronic applications. Past usage of this epoxy by Raytheon and by one of Raytheon's customers to bond similar components on a major military microelectronic program had excellent results. H44 has good physical and electrical properties and is relatively low outgassing.

The choice of a package was dictated by the following considerations: the size of the substrate which was approximately 2" x 1", the desirability of a plug-in style package for ease of attachment to a printed circuit interconnection board, the current availability of a suitable package as an off-the-shelf item, and the desirability of a hermetic package for reliability purposes because of the necessary use of some non-beam leaded devices. A Tekform Part #20117 32-pin platform-style package was chosen. The substrate was attached to the header using Ablefilm 535 adhesive preforms. An epoxy preform was used because it provided the most void free surface for such a large attachment area. Ablefilm 535 was chosen because of its excellent adhesion characteristics to gold, its low outgassing characteristics, and prior in-house usage of it for similar applications.

In/out connections were made using .001" x .010" gold ribbon which was pulsed thermo-compression bonded between the substrate and package pins. Figure 5 is a process flow diagram for the fabrication and electrical testing of the TD-206 hybrids.

PROBLEM AREAS

Several assembly and packaging processing problems had to be resolved during the development of the microcircuit. For reasons previously stated, epoxy was chosen to mount the chip capacitors and inductors. Drop testing of the hybrids during the development phase indicated the need to strengthen the mechanical bonding of some of the more massive components. It was decided that an additional non-conductive epoxy would be applied to the body of all chip capacitors and inductors to provide added mechanical strength. The package sealing process used required a substrate temperature of approximately 125°C. Subsequently, a high electrical failure rate was recorded during post-seal testing. The failure mode was determined to be open or high impedance connections on tantalum capacitor chips and chip inductors. The failure was at the epoxy chip interface. In both instances, the part was pretinned for solder attach. Consultations with the capacitor manufacturer and an epoxy manufacturer verified that they were both aware of this problem, that the capacitor manufacturer's literature was wrong and that they could not recommend an epoxy that would have good adherence to tin.

It was then necessary to find a new means to attach these parts and repair those modules which had already been fabricated. We could not solder the part because substrate metallization was pure gold which would be subject to excessive leaching. The following was eventually implemented. The terminations of the tantalum chip capacitors and chip inductors were first soldered to .004" thick gold-plated Kovar tabs; next the tabs were epoxied in place with the H44 epoxy. This eliminated the tin/epoxy interface and the associated bonding problem. In future production, these parts can be soldered directly to the substrate upon changing substrate metallization.

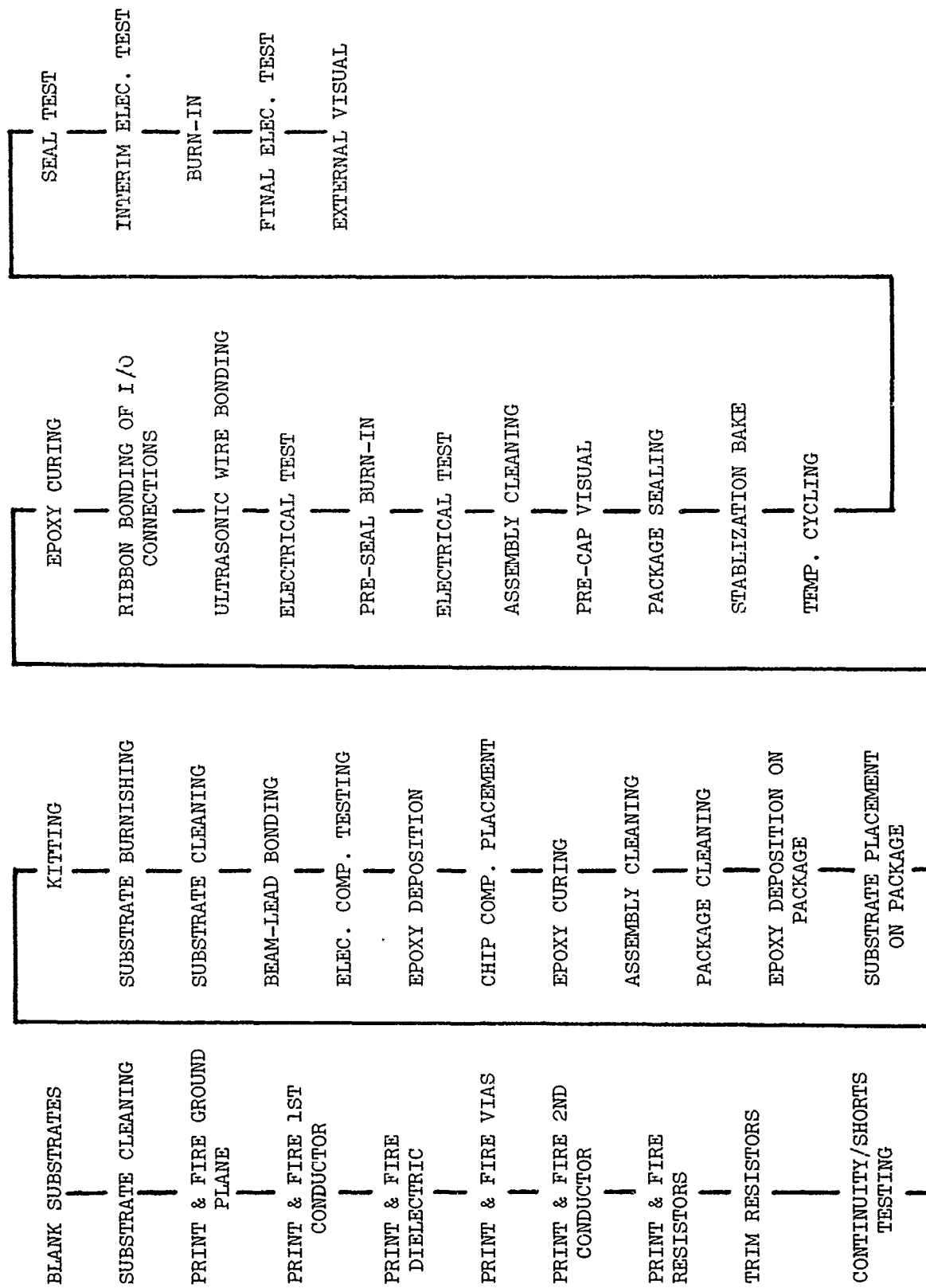


FIGURE 5. PROCESS FLOW DIAGRAM

In retrospect, it appears that the reason these parts fell off after the first drop test was not because they were so massive, but because there was never good adhesion to the tin in the first place. Probably all the non-conductive epoxy was doing was holding the part in contact with the substrate. When the substrate was put into burn-in, the non-conductive epoxy expanded and the contact was broken. In most of the burn-in failures, when the part was cooled down, it would function normally again.

The sealing of TD-206 packages went through a series of process variations in attempting to develop an optimum hermetic seal. Initial attempts to seal the package all used flux, and while successful seals were obtained (leak rates of less than 5.0×10^{-6} STD CC He/Sec.), ECOM requirements dictated sealing without the use of flux. Attempts were made to seal using solder preforms, solid wire solder, various soldering irons, a hot plate to preheat the package, hot air, a hydrogen flame, and inert and reducing atmosphere. While none of the seals appeared as good as those made using flux, seals meeting the leak criteria and good visual characteristics were obtained by using SN 62 preforms, preheating the package 100°C, and drawing a soldering iron around the perimeter.

Attempts were made at welding and brazing the package closed. A pulsed YAG laser was tried, but cross sections of the weld indicated the presence of microcracks. Raytheon's staff metallurgist indicated that these cracks might be caused by the rapid cooling rate of the Kovar when the weld solidifies or by the "hot short" tendency of this alloy which loses strength abruptly at high temperatures.

A laser was also used in an attempt to braze the cover to the case. About a half dozen alloys including copper-silver, gold-silicon, gold-tin and pure copper were tried. Whereas some success was noted, it was not possible to obtain repeatable results around the entire perimeter.

Tekform was contacted on the availability of a cover which could be single-shot projection welded. They did not have a design for this approach, and cost and delivery were prohibitive for the quantity needed.

When it became necessary to reseal the units after reprocessing to correct the component attach problem, it became apparent that the method previously described would not provide a sufficient yield. Best results were obtained on reprocessed units by preparing the seal area by wicking off solder left from the initial seal effort, cleaning off the flux residue on the surface that had come from the solder wick, and then pretinning both the cover and package without flux. At this point, the initial sealing method (preform, hot plate, iron) was used.

This method would yield at best only about 80 percent of the units sealed. In addition, and more importantly, although the seal met the leak rate criteria, mechanical strength did not appear sufficient.

A soldering technique was developed which would assure that soldering flux was not entrapped in the package. It involved pre-tinning both the header and the cover with S/N 63 solder and a rosin type, non-activated flux was used for this operation. Both header and cover were then carefully cleaned in a vapor degreaser to remove all residue. The perimeter of the assembled header and cover was then heated, not locally as in the previous procedure, but in its entirety to a temperature which melted the solder (about 230°C). It should be noted that the final joint to this point had been made without the use of flux. At this point, there was an effective seal formed between the cover and the header, but the seal was molten. Then a cotton-swab wetted with a non-activated rosin flux was carefully drawn around the outside of the seal. Since a molten metal seal already existed, there was no possibility for the flux to penetrate to the package interior. The purpose of the flux was to remove dross and promote good wetting of the solder which contained some of the package gold plating in solution. The part was then cooled and the joint was complete.

This soldering method is patterned after a method used for many years for sealing precision quartz crystals. The method was developed specifically to eliminate solder flux contamination which would be detrimental to the operation of these crystals.

To accomplish the sealing procedure, a hot plate was designed and built with a cold sink in the center. The cold sink runs at about 18°C while the hot plate is at 325°C. A fluorescent tracer was added to the flux, Alpha Microflux No. 5002, a type R flux. The technique was extremely successful with no trace of the flux inside the package. Qualification of the procedure was further investigated by placing temperature indicators in the package to assure that 150°C was not exceeded, which is the storage temperature of the hot carrier diodes.

The production testing program for the hybrids consisted of in-process electrical checks of substrate metallization and individual bonded devices, pre-cap functional electrical testing and burn-in of assembled hybrids, and post-cap temperature cycling, mechanical shock (drop) testing, burn-in, hermeticity testing and functional electrical testing of completed modules.

In-process testing of the two layer thick film substrates for continuity and shorts was performed in a routine manner prior to the assembly of components. Bonded beam-lead devices were DC checked individually prior to the assembly of other components so as to check on their as-received quality. Defective devices were immediately replaced.

Following the usual pre-cap electrical testing of the assembled hybrid, the units were burned-in at 100°C for 48 hours so as to weed out semiconductor device infant deaths and replace them prior to hermetic sealing. This burn-in was performed with DC supply power and excitation applied and was in addition to a full 168 hour burn-in performed after sealing.

Temperature cycling of the sealed hybrids was performed over the range -55°C to 125°C in accordance with MIL-STD-883, Method 1010, test condition B. Mechanical shock testing of the hybrids was accomplished by means of a drop test. Four samples from each production lot of 25 units were dropped 5 times so as to be subjected to a 1500g level in the Y_1 direction only.

All sealed hybrids were tested for hermeticity per MIL-STD-883, Method 1014. Units were sealed in a 50% He/50% N_2 atmosphere and therefore, the He could be used as a tracer gas for fine leak testing.

RELIABILITY DEMONSTRATION

Complete TD-206 B/G repeaters, consisting of two hybrid modules each, underwent reliability demonstration testing at Raytheon. The TD-206's were operated in series at one mile intervals in a cable system while being temperature and power cycled. 31,614 unit hours of operation was demonstrated with only one failure. That failure was associated with a hybrid. At the hybrid level, this translates to 63,228 unit hours of operation with only one failure. The single test failure was associated with the previously discussed problem with the epoxy bonding of tantalum chip capacitors, and appropriate corrective action had already been instituted for future units to preclude recurrence. The fact that no other type of failure occurred during this testing established at that time a high degree of confidence in the reliability of the new TD-206.

Development testing of the TD-206 B/G were subsequently performed at the U.S. Army Electronic Proving Ground, Ft. Huachuca, Arizona. The Development Test Program consisted of a series of tests, the objectives of which were the determination of performance characteristics, the evaluation of operational performance with emphasis on reliability and ruggedness, and the determination of safety, human factors and maintainability characteristics. 60 units were provided for test. So as to assess reliability, 39 TD-206 B/G repeaters (containing 78 hybrid modules) were operated in a 40 mile cable system test configuration for a total of 1400 hours, resulting in 54,600 TD-206 unit hours and 109,200 hybrid unit hours of operation. Test results from the entire Development Test Program showed that only two TD-206 B/G units failed due to hybrid malfunctioning. On one of the units, the previously discussed problem of the epoxy bonding problem was the fault. In the other unit, one lead of a beam-leaded device had been overly deformed during the bonding operation. This lead eventually cracked resulting in an open circuit. This fault should have been recognized during internal visual inspection and corrective action has been implemented by Raytheon's Quality Assurance Organization to preclude a similar fault from passing inspection during future production.

ACKNOWLEDGEMENT

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HYBRID THIN FILM TECHNOLOGY AS APPLIED TO THE
AIRBORNE LASER TRACKER (ALT) AN/AAS-32 DEVELOPMENT

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ABSTRACT

Engineering development of the Airborne Laser Tracker (ALT) AN/AAS-32 was conducted for the US Army Electronics Command by Rockwell International, Missile Systems Division, Anaheim, CA under contract DAAB07-73-C-0083. The ALT was designed to search, acquire, track and provide positioning information of properly coded laser designated targets to an aircraft operator. The ALT provides the pilot with the means to make positive target identification in a matter of seconds. Thereafter, the aircraft attitude may be manipulated to allow the aerial delivery of conventional munitions or may be used to interface with and direct a fire control system such as an aircraft mounted stabilized sighting platform.

An overview of the design features, which utilized an extensive amount of hybrid thin film circuits, is presented. Environmental, reliability, maintainability and acceptance test results are presented as evidence of the ability of hybrid thin film technology to meet the Army's requirements for equipment in the military environment. The reliability test results demonstrate a Mean-Time-Between-Failure (MTBF) in excess of 900 hours versus a design goal of 300 hours. Additionally, the maintainability test results demonstrate that modularization of circuit functions with thin film techniques reduces the Mean-Time-To-Repair (MTTR) significantly at all lower maintenance levels. The key advantage of hybridization as demonstrated by these results is lower equipment life cycle costs.

INTRODUCTION

The Airborne Laser Tracker (ALT) AN/AAS-32 is an aircraft installed system that automatically searches a target area, detects properly coded laser energy and tracks the source of reflection (target) of that energy. Figure 1 depicts a typical attack helicopter with the ALT installed in the aircraft nose. The ALT is comprised of three major assemblies (from left to right in Figure 2): an electronics unit, a receiver unit and a pilot's control panel. A simplified block diagram of the ALT is shown in Figure 3.



FIGURE 1. ALT INSTALLED ON AH-1G HELICOPTER

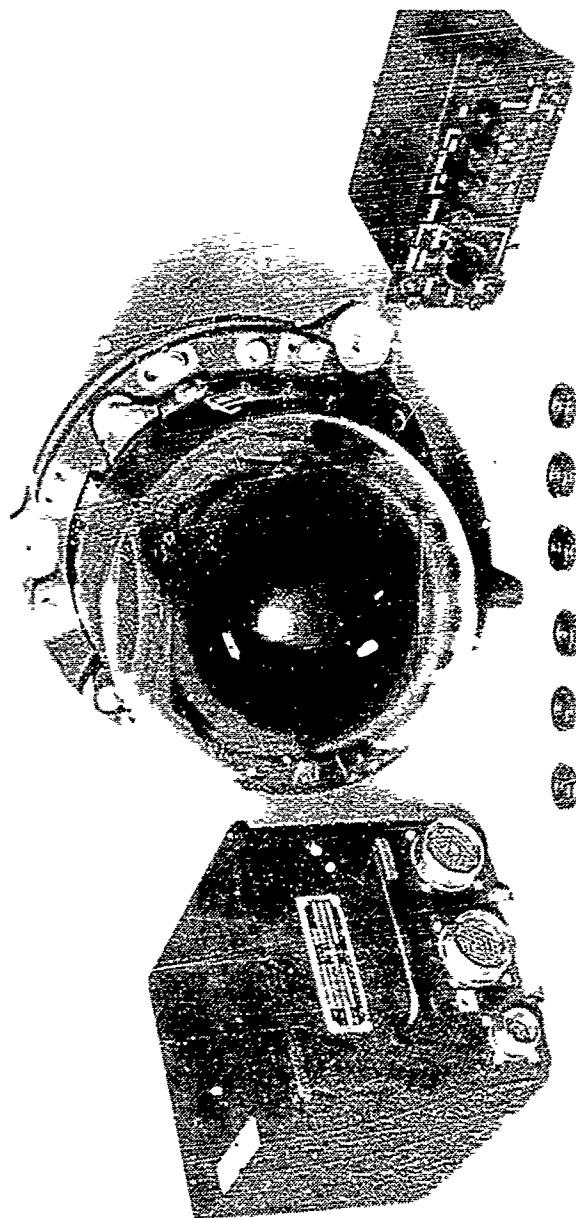


FIGURE 2. AIRBORNE LASER TRACKER AN/AAS-32

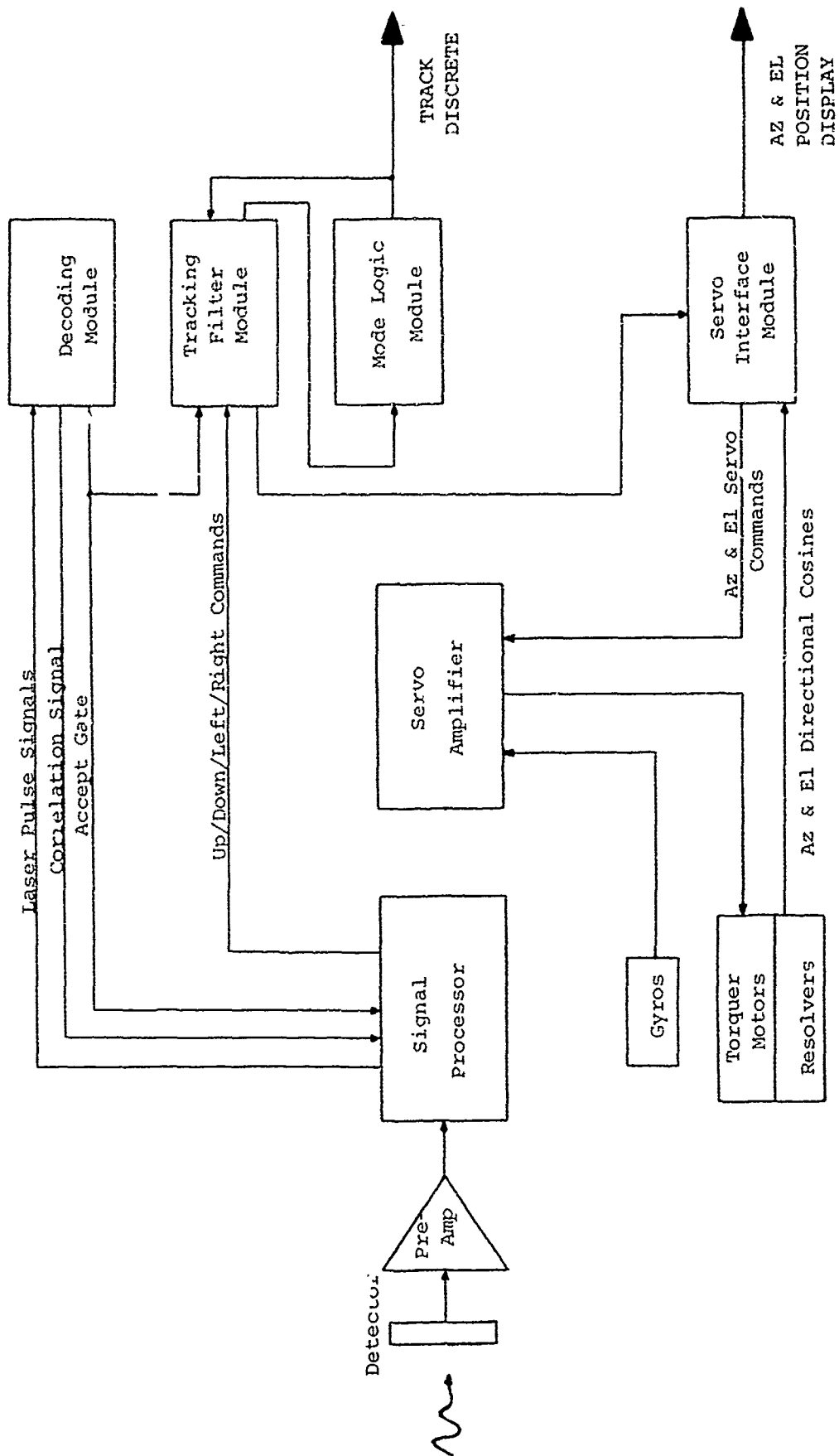


FIGURE 3. ALT SIMPLIFIED BLOCK DIAGRAM

The receiver unit is mounted in the nose of the helicopter to afford an unobstructed field of view. The receiver contains a four-quadrant silicon P-I-N photo-detector, preamplifiers, signal processor, rate gyros, torquer motors, gimbal resolvers and the servo control electronics (rate stabilization loop). The detector/preamplifier, optical assembly and signal processor are mounted on a two axis rate stabilized gimballed platform. Laser signals of the proper wavelength are converted to appropriate electrical signals by the quadrant detector and immediately amplified by the preamplifier. These signals are then routed to the signal processor for electronic processing to obtain direction (azimuth and elevation) commands. Interface of these commands to the servo control electronics via the tracking filter module (electronics unit) enables error generation to drive the gimballed platform such that the laser energy is centered within the four quadrants of the detector.

The electronics unit may be mounted anywhere in the helicopter as space and mission dictates. The electronics unit contains the system power supply, an interconnecting printed circuit board and four plug-in printed circuit board modules: system mode logic and tracking filter, servo interface, Built-In-Test-Equipment (BITE), and decoding. These modules were partitioned by electronic function for ease of maintenance, reduced complexity and reduced life cycle cost.

The control panel is mounted in the pilot's cockpit instrument rack enabling the pilot to set the desired mode (TEST, STBY or SCAN) for system operation and to set in the desired three digit code. Two fault lamps are provided to indicate fault location (receiver unit or electronics unit) during the TEST sequence. Successful completion of the TEST is indicated by illumination of a GO indicator. A TRACK indicator is provided to signal the pilot that the system is tracking laser energy (of the proper code) reflected from a target.

HYBRID THIN FILM CIRCUITS

The ALT system's size and weight were of great concern during development since the ALT was designed for helicopter installation where these parameters are critical. With this constraint, the majority of the ALT electronic circuitry was packaged into Hybrid Thin Film Circuits (HTFC) which provided maximum capability with minimum size and weight. In addition to the discrete components; metal oxide semiconductor (MOS), complementary MOS (CMOS), transistor transistor logic (TTL) and medium scale integration (MSI) were used throughout the ALT design. Twenty-one (21) different HTFC types were developed, with two of them used twice for a system total of twenty-three (23) HTFC's. One such HTFC is depicted in Figure 4.

The receiver unit utilizes eight (8) HTFC's (see Table 1): four (4) in the signal processor module and four (4) in the servo amplifier module (see Figure 5). These HTFC modules were designed by function to reduce complexity and cost. The function of the signal processor module is to process the detector outputs (amplified by the Quad Pre-Amplifier HTFC) to furnish the correct up/down and left/right commands to the servo system, which then aligns the receiver's gimballed platform to the target. The

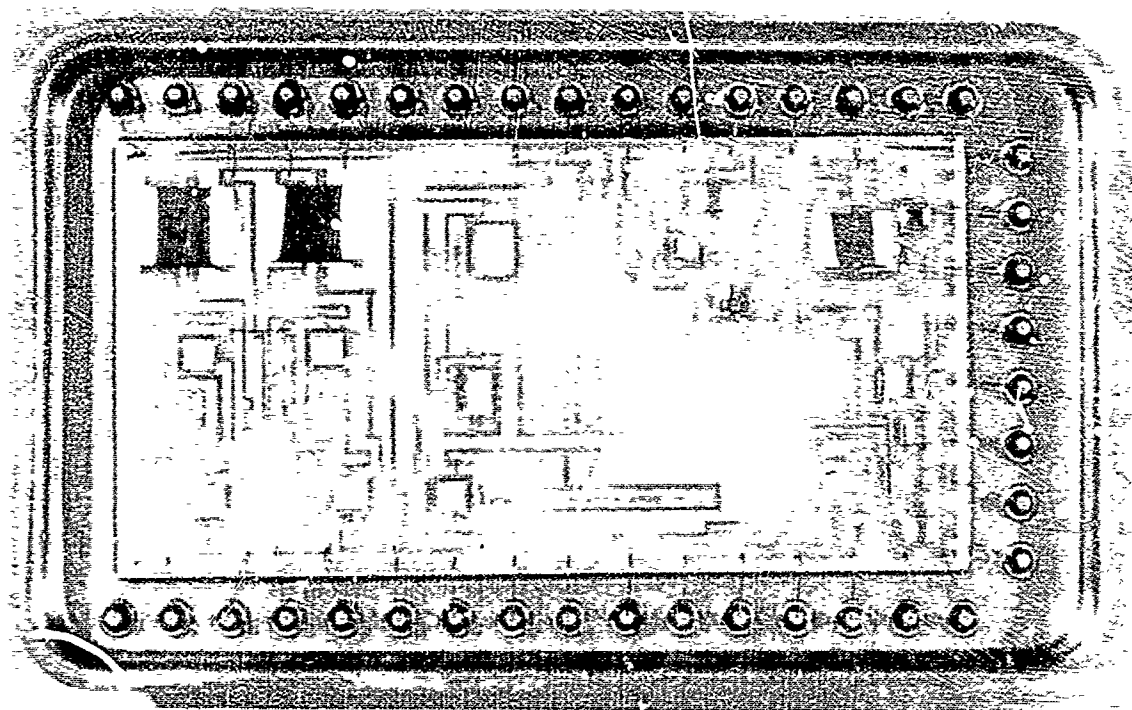


FIGURE 4. HYBRID THIN FILM CIRCUIT

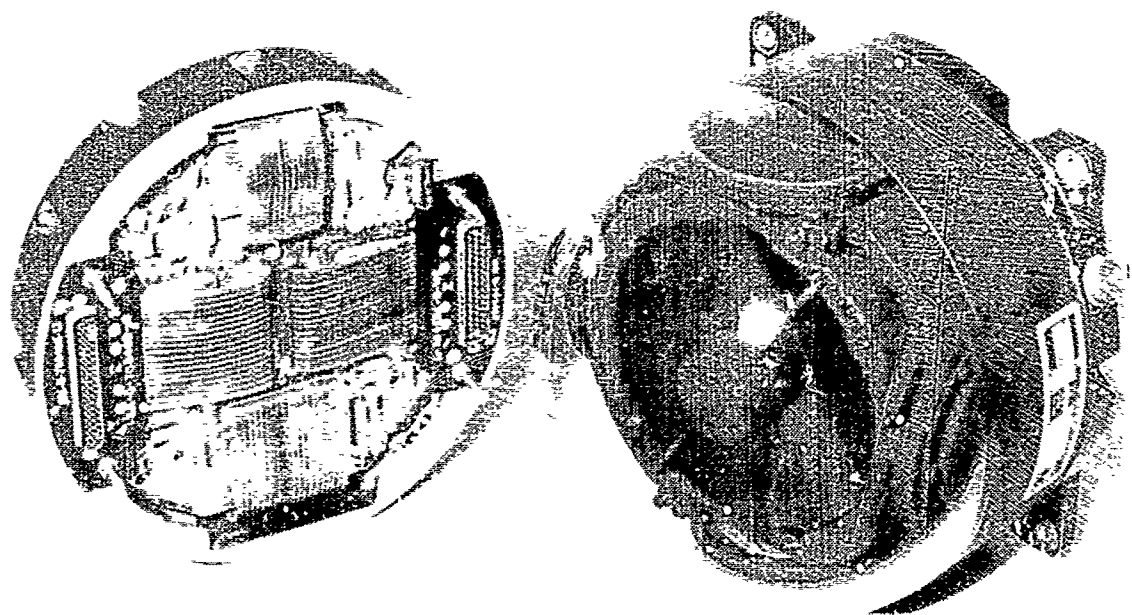


FIGURE 5. ALT RECEIVER UNIT - BROKEN OUT

<u>Circuit Function</u>	<u>Quantity Per System</u>	<u>Package No. Pins</u>	<u>Thin Film Resistors</u>	<u>Discrete Resistors</u>	<u>Capac- itors</u>	<u>Trans- istors</u>	<u>Diodes</u>	<u>Integrated Circuits</u>
Signal Processor								
* Pre-Amplifier (Quad)	1	16	12	16	5	12	11	--
* Sum Channel Amplifier	1	40	52	1	17	5	4	7
* Extended Range Amplifier	1	40	40	--	22	4	--	16
* Difference Channel Amplifier	1	40	44	12	22	4	12	14
Servo Amplifier Module								
* Resolver Amplifier	1	40	44	4	28	16	--	10
* Two Axis AC/DC Amplifier	1	40	30	1	14	7	2	10
* Servo Compensation Driver	2	32	42	13	9	9	10	7
TOTAL (8 hybrids)			306	60	120	66	49	64

TABLE 1. ALT RECEIVER UNIT HYBRID CIRCUITS

up/down and left/right commands (tracker error signals) are generated in the Sum Channel and Difference Channel HTFCs. Additional range capability is provided by the Extended Range HTFC for low signal amplitudes by separately amplifying and thresholding each of the quadrant outputs which halves the effective noise. Thus, the ALT has a greater sensitivity and greater operating range. The tracking accuracy is improved with greater energy density signals and the system will automatically switch out of the extended range mode.

The servo amplifier module provides for the rate stabilization of the gimballed platform. Azimuth and elevation servo error commands from the electronics unit are received by the azimuth and elevation Servo Compensation Driver HTFC's. Further, the Servo Compensation Driver HTFC circuit receives the demodulated azimuth and elevation gyro signals from the Two Axis AC/DC Amplifier HTFC. Servo error commands are processed/generated within the electronics unit and routed to the servo amplifier via the servo interface module (electronics unit). The Servo Compensation Driver HTFCs then drive the torquer motors to command the platform. Platform controls are derived from the rate gyros, signal processor and resolver position signals for the various operating modes.

The electronics unit (see Figure 6) utilizes fifteen (15) HTFCs (see Table 2) as follows: One (1) HTFC in the system power supply, three (3) HTFCs in the logic module, four (4) HTFCs in the servo interface module, four (4) HTFCs in the Built-In-Test Equipment (BITE) module and three (3) HTFCs in the decoding module.

The power supply accepts 28 Vdc and 115 Vac, 400 Hz input power (MIL-STD-704) and generates filtered 28 Vdc, ± 14 Vdc, ± 20 Vdc, ± 5 Vdc, -300 Vdc and 52/26 V RMS, 400 Hz power. The DC Regulator HTFC provides power regulation and rectification. Overvoltage, undervoltage and reverse polarity voltage protection are also provided.

The logic module provides control of the system based upon the position of the mode selection switch on the control panel. The Mode Control HTFC provides platform commands for cageing, scanning, tracking, self-testing, standby or external cueing. The two tracking filter HTFCs accept servo error commands, accept gate pulses and the track discrete signal to generate an adaptive tracking rate. The tracking rate is a function of the integral of previous error signals and the current command. Basically, this HTFC doubles or halves the tracking rate depending on the current direction signal, an integral of previous direction (error) signals and whether cross over (i.e. up to down, left to right) occurs.

The servo interface module provides the scan pattern generator, target position indicator meter driver and servo command generation functions. The Scan Generator HTFC generates the appropriate azimuth and elevation attitude commands for the appropriate scan pattern selected on the control panel. These commands are interfaced with the three servo interface HTFC's along with the resolver signals to generate the azimuth and elevation servo commands. Positive feedback through the servo loop ensures desired platform precession. The servo interface module also provides azimuth and elevation line-of-sight positioning information (directional cosines) for

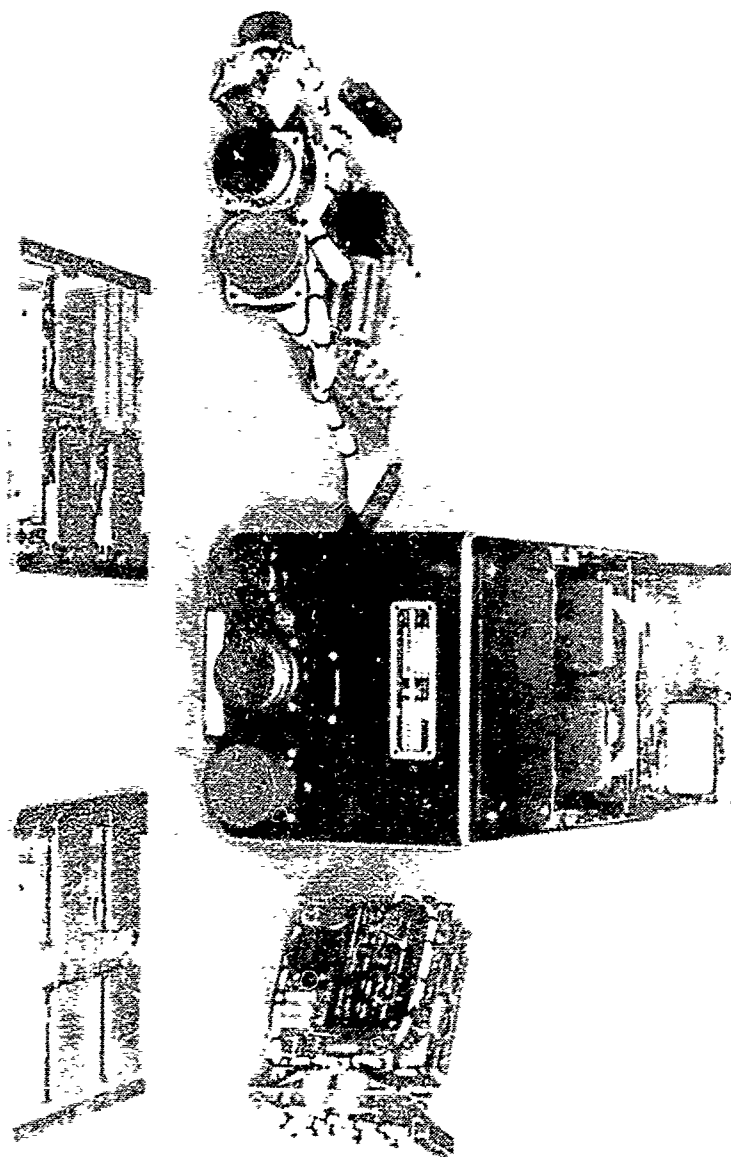


FIGURE 6. ALT ELECTRONICS UNIT - BROKEN OUT

<u>Circuit Function</u>	<u>Quantity Per System</u>	<u>Package No. Pins</u>	<u>Thin Film Resistors</u>	<u>Discrete Resistors</u>	<u>Capac- itors</u>	<u>Trans- istors</u>	<u>Diodes</u>	<u>Integrated Circuits</u>
Power Supply								
* DC Regulator	1	40	43	5	7	23	11	5
Logic Module								
* Tracking Filter	2	40	25	2	7	2	4	26
* Mode Control	1	40	12	7	6	-	4	19
Servo Interface Module								
* Servo Interface #1	1	32	49	4	6	9	2	15
* Servo Interface #2	1	40	49	5	6	11	6	14
* Servo Interface #3	1	32	64	3	8	2	12	12
* Scan Generator	1	32	34	-	5	4	--	17
BITE Module								
* BITE #1	1	40	7	3	7	-	3	23
* BITE #2	1	40	--	-	2	-	-	22
* BITE #3	1	40	19	-	2	4	6	19
* BITE #4	1	40	40	3	6	1	-	14
Decoding Module								
* Coding Logic	1	32	8	-	8	-	4	11
* Correlation Logic	1	40	5	2	4	1	2	28
* Programmable Counter	1	40	14	-	10	-	2	15
TOTAL (15 hybrids)			394	36	91	59	60	266

TABLE 2. ALT ELECTRONICS UNIT HYBRID CIRCUITS

use by the pilot's display.

The four BITE HTFC's of the BITE module provide the ALT with a complete self-test capability. When initiated on the control panel, the BITE sequence will verify the operation of the servo electronics, resolver chains, mode control logic, input-output circuitry, scan generator, detector, signal processor and coding circuitry. Fault isolation to the receiver unit or the electronics unit is provided by indicator lamps on the control panel. Operational readiness after successful completion of the test sequence is also indicated by lamps on the control panel.

The decoding module accepts laser pulse signals from the signal processor. If these pulses meet the coding criteria (set in by the thumbwheel switches on the control panel) a correlation signal is provided to the signal processor. Acceptance gates are also generated and furnished to the signal processor and the tracking filter which in turn furnishes a track enable signal to the mode logic module. A track discrete is generated by the mode logic module for display purposes. The decoding module's functions are executed by three HTFC's, two read-only memories and one crystal oscillator.

The above described circuit functions reveal the overall complexity of the ALT system. Yet, the ALT weighs 29 pounds: 19.875 pounds for the receiver unit (6 pounds in optics), 7.875 pounds for the electronics unit and 1.25 pounds for the control panel. In addition, performance capability is actually better than originally specified.

SYSTEM TEST RESULTS

A full test program was conducted as part of the ALT engineering development effort to ascertain ALT's performance as a fully militarized equipment. This program consisted of performance acceptance tests, environmental tests, a reliability demonstration and a maintenance demonstration.

The ALT met and/or exceeded all performance criteria originally specified including sensitivity, false alarm rate, tracking accuracy and track/rescan criteria. These performance characteristics were also tested before and after the environmental tests. Problems which arose during the environmental test sequence were not caused by failures of the HTFC's. The problems that were encountered were either mechanical, packaging or in some cases vendor induced problems (i.e. lack of proper conformal coating on edge-lit panel for the control panel).

The environmental tests of Table 3 were performed on the ALT system in accordance with the listed Methods and Procedures of MIL-STD-870B, "Environmental Test Methods". During the vibration test, a large magnitude resonance point was discovered in the Y-axis of the gimballed platform. Redesigning resulted in a reduced resonance magnitude, but the sinusoidal sweeps were reduced from 10 G peak to 2 G peak between 95 Hz and 120 Hz. 10 G levels were used otherwise. Other problems that surfaced included:

<u>Test</u>	MIL-STD-810B		<u>Results</u>
	<u>Method</u>	<u>Procedure</u>	
Temperature Altitude	504	I	Passed
Humidity	507	II	Passed
Vibration (with resonant dwell)	514.1	I	Passed (2 G peak from 95 Hz - 120 Hz)
Bounce, Loose Cargo	514.1	XI (Part2)	Passed
Shock, Basic Design	516.1	I and III	Passed
Shock, Bench Handling	516.1	V	Passed
Shock, Transit Drop	516.1	II	Passed
Acceleration	513.1	II	Passed
Sand and Dust	510	V	Passed
Fungus	508	I	Passed
Salt Fog	509	-	Passed
Explosive Atmosphere	511	I	Passed
Rain	506	I	Passed
Leakage (Immersion)	512	I	Passed

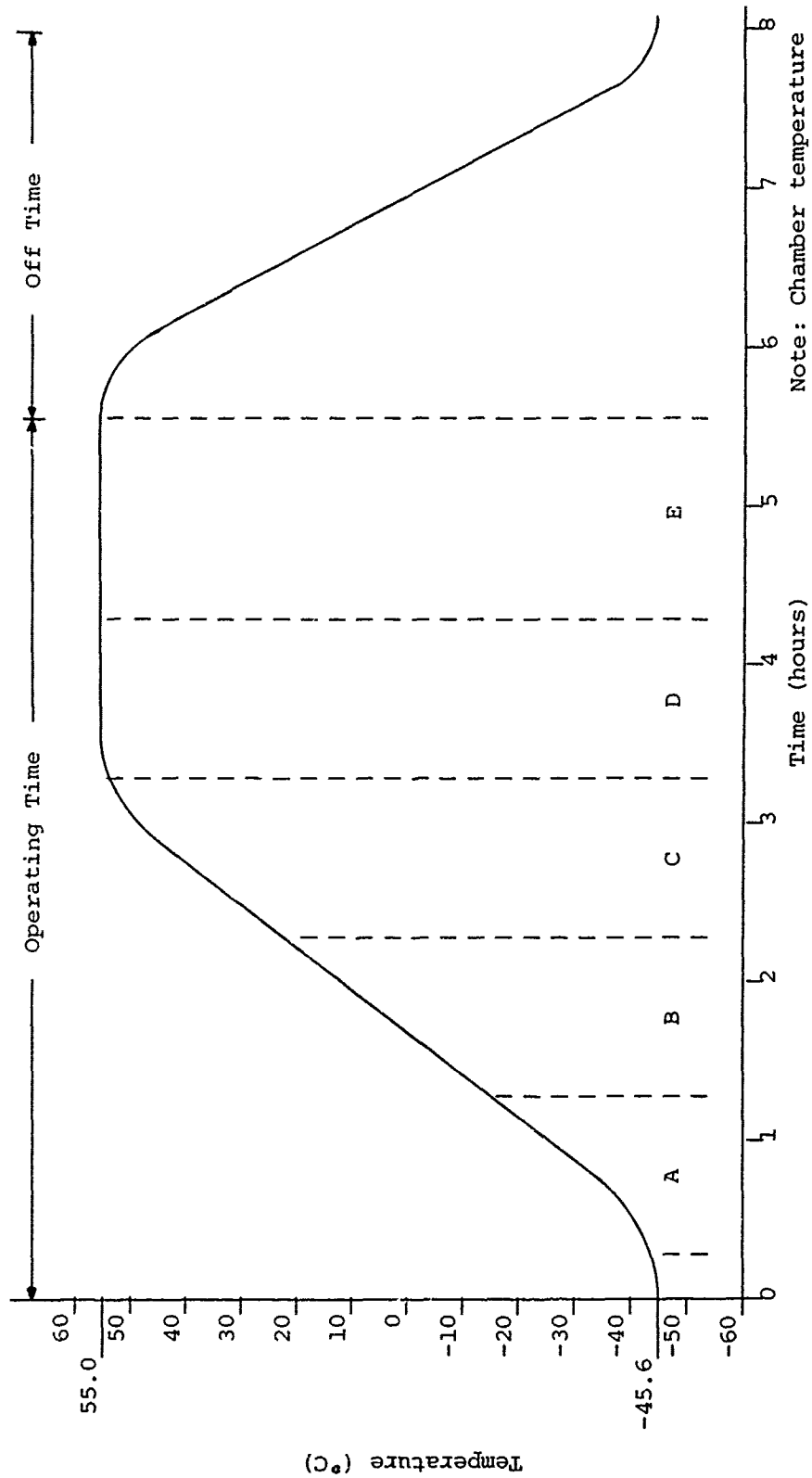
TABLE 3. ALT ENVIRONMENTAL TESTS

a shorted edge-lit panel during the rain test (lack of conformal coating), decoding module oscillator interference during design shock test (tight clearance on printed circuit board) and one corroded thumbwheel switch (of three present) during the salt fog test (vendor quality control problem since the switch was a military qualified component). The ALT HTFC's were not the causative agent for any of the problems that surfaced during the environmental test program and none of these problems caused sympathetic malfunction of the HTFC's.

The ALT requirements document specifies a Mean Time Between Failure (MTBF) of 100 hours (minimum acceptable) and 300 hours (best operational capability). During engineering development, the ALT was tested for the best operational capability of 300 hours. A discrimination ratio of three (3) was used which required the reliability test program to accumulate 900 hours of operating time with no more than five (5) failures. The reliability test was conducted in accordance with Test Plan XXII of MIL-STD-781, "Reliability Tests, Exponential Distribution", which required chamber temperature cycling (see Figure 7) from -50°C to $+55^{\circ}\text{C}$ and vibrational cycling (2.2 G peak) for ten (10) minutes of every hour during system operation.

The four ALT modes of operation (STBY, TEST, SCAN 1 and SCAN 2) were rotated in the one hour time-blocks A thru D of Figure 7 such that all modes of operation were exercised over the entire temperature range during test cycling. The ALT mode of operation during time-block E was set at SCAN 1 since this mode is operationally more demanding than the others. Strip chart recordings monitored the system's operation and tracking variation (azimuth and elevation). Sensitivity and the false alarm rate were manually measured during the test. After 931 hours of accumulated operating time, the test program was ended. The first ALT system accumulated 512.5 hours with no failures and the second system accumulated 418.5 hours of operation with one (1) unconfirmed failure (the failure could not be verified during troubleshooting). Thus, the reliability test resulted in a demonstrated MTBF of 931 hours versus the 300 hour requirement.

The final major test program conducted during engineering development was the maintenance demonstration. Selected maintenance requirements for both Organizational and Direct Support levels (there is no General Support for the ALT) were demonstrated and actual Mean-Time-To-Repair (MTTR) and Maximum-Time-To-Repair (M_{max}) were compared with the specified values. Organizational maintenance involves repair of the ALT by replacing the receiver unit, the electronics unit or the control panel as required. Direct Support maintenance involves repair of the receiver unit or the electronics unit by fault isolation and replacement of modules. HTFC's are only repairable at the depot level. The maintenance demonstration results are given in Table 4. In all cases, the ALT demonstrated an MTTR and an M_{max} better than that originally specified.



Note: Chamber temperature transition time (-50°C to +55°C) was 20 minutes.

FIGURE 7. RELIABILITY TEMPERATURE-TIME CYCLING

Mean-Time-To-Repair

<u>Level</u>	<u>Specified</u>	<u>Demonstrated</u>
Organizational	< 15 min.	3 min. 54 sec.
Direct Support	< 30 min.	17 min. 27 sec.
General Support	< 60 min.	None

Maximum-Time-To-Repair

<u>Level</u>	<u>Specified</u>	<u>Demonstrated</u>
Organizational	< 30 min.	4 min. 50 sec.
Direct Support	< 60 min.	40 min. 43 sec.
General Support	<180 min.	None

TABLE 4. MAINTENANCE DEMONSTRATION RESULTS

SUMMARY

The Airborne Laser Tracker AN/AAS-32 is one of the first USAECOM developed equipments to utilize hybrid technology as the major means of electronic circuit implementation. The ALT is military qualified by virtue of meeting the environmental criteria for military equipment. Further, the ALT has demonstrated an MTBF of over 900 hours, three times the best operational capability specified in the ALT requirements document. Finally, the ALT is an easy equipment for the Army to maintain at the lower maintenance levels and it exceeds the maintenance requirements such that the maintenance down-time is small. This will result in better operational readiness for the Army and a much greater probability of mission success.

HYBRID MICROCIRCUIT USAGE FOR THE AN/TPQ-36 RADAR SET

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ABSTRACT

Radar Set AN/TPQ-36 is a pulse doppler radar system using a phased array antenna. The system is capable of detecting weapon projectiles launched at any angle within a selectable azimuth sector. If a hostile projectile is detected, the radar set computes the hostile weapon location and displays this information to the operator on a terrain map. The radar also is capable of detecting and tracking friendly targets for registration purposes, and is capable of locating points of origin even when a combination of batteries are firing simulatenously. The radar set is lightweight, transportable, and capable of rapid set-up and tear-down. The system can be set-up and operable in less than 20 minutes. It is designed for dependable operation in a tactical field environment.

Approximately 133 hybrid microcircuits of 34 types have been designed into the AN/TPQ-36 radar exciter, receiver, signal processor, computer, and beam steering units to assure that size/weight/volume constraints could be met. Many of these microcircuits are RF types, comprising thick film screened-and-fired resistor-conductor networks on ceramic substrates, with reflow-solder microcomponent parts. The assembled microcircuits are hermetically sealed by a metal cover soldered to the base platform.

Digital-type microcircuits are used for various applications including signal processor control and phase shifter drivers. These utilize thin film vacuum-evaporated resistor-conductor network, hermetically sealed in soldered metal packages, with epoxy-attached capacitors and bonded/wired semiconductor chips.

The AN/TPQ-36 is a relatively new Army radar system, but it already is evident that the usage of hybrid microcircuits has contributed toward successful compliance with design goals; and toward excellent demonstrated field performance.

This paper outlines the functions performed by these hybrid microcircuits. Cost trade-offs are discussed to illustrate relationships between actual and potential hybrid microcircuit usage in systems such as the AN/TPQ-36.

SYSTEM DESCRIPTION

Radar Set AN/TPQ-36 is a highly-mobile pulse doppler radar utilizing computer-controlled electronic beam scanning to locate the origin of weapon projectiles fired from one or more batteries.

The system is designed for locating friendly or hostile mortar and artillery batteries within a selectable 1600-mil azimuth sector by detecting in-flight rounds, by tracking them, and then by extrapolating their trajectories back to the firing weapon; often before the first round hits the ground. Target location is displayed on a terrain map. System weight is 5,500 pounds, which makes it air-transportable.

The entire system comprises an Operations Control Group, housed within a standard S-250 shelter, mounted on a 1-1/4-ton M-561 vehicle; and an Antenna-Transceiver Group, mounted on a standard 3/4-ton M-116A1 trailer, towed behind the M-561. In the transport mode, shown in Figure 1, the antenna is horizontal, and extends from the rear of the rotating equipment enclosure to the forward edge of the turbine -powered electric generator. Cables for connecting the two groups are carried on the shelter.

Figure 2 depicts the equipment in the operational mode. The shelter and antenna-transceiver trailer may be separated by up to 150 feet for operation; the prime power generator is located on the trailer.

The antenna is raised to the vertical position, and the trailer is raised up on the three jacks and rough-leveled to 1°. The trailer has been situated so that the equipment enclosure azimuth axis is placed over a site marker. A survey marker about 100 meters distant is used for azimuth orientation by aiming the antenna-mounted telescope at it, and entering the 14-bit azimuth encoder output in the system computer.

The trailer equipment enclosure contains four compartments - three peripheral and one central. The right side compartment (looking forward to the back of the antenna)(Figure 3) contains the receiver/exciter. The rear compartment houses the transmitter high-voltage circuits and the RF amplifier tubes, while the left compartment contains the transmitter low-voltage circuits. The central area (with access from the enclosure top) holds microwave components and the antenna drive controls, as well as the system 28 VDC power supply. Detailed views of these areas are shown in the group descriptions presented later. System power and signal cables enter at a panel on the non-rotating base of the trailer.

A view of the interior of the Operations Shelter is shown in Figure 4. The operator is seated at the Weapon Location Assembly (WLA), which displays predicted weapon location on standard grid maps. Mounted above the WLA are the computer memory and the AN/UYK-15 computer. The line printer is at the right of the computer, and the R-442/VRC receiver is between the line printer and the right shelter wall.

Below the line printer is the USM-281 oscilloscope, which serves as the radar B-scope. A field telephone is at the right. Both the oscilloscope and the telephone are above the RT-524/VKC transmitter-receiver.

The signal processor, which houses circuit cards for the WLA, B-scope, and line printer, is located in the left rear corner of the shelter.

A simplified block diagram of the AN/TPQ-36 Radar Set is shown in Figure 5, which includes code numbers (in parentheses) identifying the various types of hybrid microcircuits within each major system components; and cross-referenced to the listing of Table I.

Antenna-Transceiver Group

As indicated in Figure 5, the Antenna-Transceiver Group in the trailer includes an electronically scanned antenna, an air-cooled transmitter, (including a fault processor to provide Built-in Test (BITE) outputs), the radar receiver, and a frequency exciter, plus a prime power unit. The antenna portion includes phase shifter drivers and logic circuitry packaged across the lower end of the array, together with a trailer synchronizer.

The antenna is mechanically tilted forward or backward by an electrically-driven linear actuator, connected to the lower part of the antenna. A tilt sensor measures antenna tilt and cross-tilt directly, and resistive sensors measure antenna temperature. Control relays for the elevation actuator are located in the central compartment of the trailer. The antenna is mechanically rotated in azimuth by a drive motor, also located in the central trailer compartment, together with its control relays. Mechanical positioning of the antenna (both elevation and azimuth) can be accomplished by means of controls within the shelter.

Hughes microcircuits used within the Antenna-Transceiver Group (Figure 5 and Table I) include two types within the antenna electronics compartment, three types within the exciter, and one type each within the trailer portion of the receiver, and in the transmitter.

Operations Control Group

The vehicle/shelter houses the Operations Control Group, which includes the signal processor, the display/control group (mainly the AN/UYK-15 computer), the weapons location assembly (WLA), the communications group, the environmental controls group, and various power supplies/distribution assemblies.

The main radar synchronizer is located in the signal processor, and a secondary synchronizer is located in the trailer with the bearing steering electronics. Synchronization is maintained between the two areas by means of sync pulses and a common clock. A circulating data bus aids in the process, and permits commands and data to be transferred over the cable between the trailer and shelter.

System control resides in the AN/UYK-15 digital computer. The computer commands the radar mode (search, track, or verify), accepts detection data, and extrapolates track data to the weapon location.

Display and control devices are provided to assist the operator in his tasks. A Type USM-338 "B"-scope presents a range-azimuth plan view of system performance, showing the position of search and track video returns. A line printer provides a permanent record of important data, and also provides cues for operator action during initial system set-up. Communications include a Type R-442/VRC receiver and a Type RT-524/VRC transmitter-receiver.

A key element in operations control is the weapon location assembly, which is an automatic plotting board. A map is placed on the drum of the WLA, and after calibration, the computer can indicate the predicted location of a weapon. The operator reads height of the terrain at the predicted position and, if different from the height used for extrapolation, enters a height correction. The computer performs a new extrapolation, and the sequence is iterated until the height on the map at the predicted weapon position correlates with the true height reference given to the computer.

Figure 5 and Table I indicate those hybrid microcircuit types used within the shelter. Five types are used in the shelter portion of the receiver, one type in the signal processor, and an assorted array of types have been used within the control computer.

DEVELOPMENT/PERFORMANCE RECORD TO DATE

Engineering development of the AN/TPQ-36 Radar Set has spanned the period 1973 through 1976. Five sets have been fabricated to date on a "design to cost" basis, with a target MTBF of 400 hours. A comprehensive testing program involving 6700 rounds of live firing took place during 1975 and 1976 at U.S. Army Yuma, Arizona Proving Grounds. This was a performance stress test against hostile U.S. mortars, and the equipment readily met performance design requirements for location probability. During these tests, weapon location accuracy was outstanding.

In addition, formal tests were conducted to check impact prediction of 81 mm mortar rounds and 105 mm/155 mm artillery rounds, with good results. Datum plane intersection and airburst location tests were conducted for 105 mm/155 mm artillery; also with good results.

Reliability/Maintainability/Mobility tests were initiated in mid-1976 by conducting long-term operability tests at 50°C. These will be followed by Development Tests and Operational Tests. Results to date indicate that the U.S. Army will realize its goal of procuring reliable, cost effective production units within the next several years.

ROLE OF HYBRID MICROCIRCUITS IN THE SYSTEM

A variety of hybrid microcircuit concepts have been utilized during the AN/TPQ-36 design phases, as indicated in Table I. These include solder reflow thick film, chip-and-wire thick film, chip-and-wire thin film, and beam lead thick film concepts. This versatility of concepts illustrates the variety of methods which can be employed in military systems to accomplish overall size, weight, reliability, and electrical performance goals. As an example of this versatility, the receiver/exciter microcircuits generally require low power drain, but they must operate at relatively high frequencies, with low-resistivity grounding and adjustable gain/bandwidth levels to meet stringent electrical performance requirements. The most economical and effective method of accomplishing these goals involves the use of hermetically-sealed discrete semiconductor packages and thick film solder reflow technology with toroidal tuning coils, as illustrated by the microcircuits shown in Figure 6. These microcircuits utilize platinum-gold conductor pastes and ruthenium-based resistor pastes. Lead-tin solder (2% silver) is used for microcomponent parts attachment.

In other applications, such as those illustrated in Figure 7, current drains are higher, and switching action takes place at lower digital circuit speeds. The semiconductor chips must dissipate heat directly to the ceramic-based thin-film resistor-conductor networks, and unshielded "flying lead" wire-bonded resistor networks pose no problem. For this type of application, flash evaporated nichrome/gold thin film panels are etched-back to form the resistor-conductor networks, to which the semiconductor chips are epoxy-attached and wire-bonded with one-mil gold wire. An alternative resistor-conductor network used for the more repetitive phase shifter driver microcircuits involves screened-and-fired ruthenium-based resistors and modified fritless gold conductors.

Hybrid microcircuits are involved in performing all major functions of Radar Set AN/TPQ-36; namely, the determination of target azimuth, elevation, range, and range rate; plus the elimination of clutter.

Signal Processor

The AN/TPQ-36 signal processor (Figure 5) controls signal generation, and processes the incoming radar return signal to determine range and remove both stationary and moving clutter. The hex fast line receiver microcircuit is a thin film chip-and-wire microcircuit (shown in Figure 7) which aids in the counting, buffering, and decoding operations associated

Signal Processor (Continued)

with the signal processor. The multiple usage of this functional micro-circuit aids considerably in reducing size and weight, and in eliminating the need for redundant designs of similar conventional circuitry throughout the processor itself. Most of the signal process or electronics comprise "flat-packs" and/or dual-in-line semiconductor packages mounted on nominal 5" x 5" printed wiring boards, as illustrated in Figure 8.

Exciter

The block diagram of Figure 9 illustrates the receiver-exciter interfaces, and also repeats the hybrid microcircuit location codes referred to in Figure 5 and Table I. The exciter functions as a signal generator to switch and sum various frequency combinations which are transmitted and subsequently received to provide target elevation information. Local oscillator reference signals, system clock signals, and rf/lf target simulation signals also are generated within this unit.

The thick film solder reflow hybrid microcircuits used in this portion of the radar set perform a number of r-f oscillator and switching functions. Many of their tuning characteristics are determined by properly adjusting the turns on toroidal coils, such as those illustrated in Figure 6.

Receiver

The radar receiver front end (A) is located in the antenna trailer, while the i-f limiter and phase detector portions (B) are located within the shelter. The printed wiring board on which the phase detector hybrid microcircuit is mounted is illustrated in the photograph of Figure 10.

The six types of hybrid microcircuits used in this portion of the radar set perform functions ranging from dynamic range control (sensitivity time control generator) to various signal limiting, phase detection, and tuned amplifier functions, as indicated in Table I. Both thin film chip-and-wire and thick film solder reflow concepts are utilized here, with the choice of concept selected during design phases in accordance with the frequency/power levels involved; and to obtain the maximum in performance/reliability and life cycle cost effectiveness.

The receiver processes target signal returns, utilizing the phase detector, and transmits these signals to the signal processor.

Receiver (Continued)

The photograph of Figure 11 shows the receiver-exciter compartment located on the trailer. All of the oscillator and switching hybrid microcircuits, plus much of the other electronics circuitry associated with the summing networks and harmonic generator are included in the two 6" x 6" x 1.5" packages shown in the lower left corner of the compartment, and illustrated separately in Figure 12.

These exciter oscillator units could not have been packaged within the illustrated dimensions without the use of hybrid microcircuits, and a significant weight savings was realized. It must be noted, however, that the receiver-exciter compartment includes much unused volume. The use of hybrid microcircuits thus must be justified on the basis of improved reliability, reduced system weight, and lower production costs, yielding potentially reduced system life cycle costs. In ground-based equipment such as the AN/TPQ-36, size reduction alone does not justify the usage of hybrid microcircuits.

Transmitter

Fiber optics are utilized within the AN/TPQ-36 radar transmitter for on-line signal monitoring and fault isolation of high-voltage circuitry.

This relatively new application of hybrid microcircuits involves the use of both light-emitting and light-sensitive diodes combined within single hermetic packages to transmit and amplify key signals which monitor active transmitter functions such as grid voltage, grid bias, and filament voltage.

Antenna

Phase scanning determines azimuth beam positions and this function is performed by the ferrite phase shifters. As indicated in the block diagram of Figure 13, the antenna phase characteristics are controlled by the computational unit and the shift register, which in turn control the 64 phase shifter driver hybrid microcircuits. The computational and shift register electronics circuitry is packaged on nominal 5" x 5" printed wiring boards or "cards" which are inserted into the slotted chassis shown in the photograph of Figure 14. One of the individual cards is shown in front of the chassis, which attaches to the lower portion of the antenna structure (Figure 3). One of the 16 cards on which the phase shifter driver hybrid microcircuits are mounted is shown in the photograph of Figure 15.

Antenna (Continued)

Thick film chip-and-wire methodology was selected for this application (Figure 7) to accommodate the relatively high power levels required. The usage of modified fritless gold thick film paste provides excellent adhesion and good bondability, while at the same time ensuring low-cost producibility in the relatively high quantities which will be required in the future. Thick film chip-and-wire concepts also are utilized for the hybrid microcircuit current regulators used within the antenna electronics package to aid in temperature sensing.

Display and Control

The AN/UYK-15 computer includes many dual-in-line TTL semiconductor devices mounted on nominal 4" x 4" printed wiring boards. A number of hermetically-sealed thick film hybrid microcircuits utilizing beam-leaded semiconductor devices also are used within this computer.

EQUIPMENT RELIABILITY

Radar Set AN/TPQ-36 utilizes more than 4,000 semiconductor integrated circuits, in addition to those included in the hybrid microcircuits. During the first 5,000 system operating hours on the engineering development models, a failure rate on SIC's of 0.097 failures per million hours was realized. As the system moves toward production, failure rates will be reduced even further by maintaining a realistic approach to the overall task. The problem is to enhance system reliability by utilizing controlled processes and MIL-STD-883-grade semiconductor devices for both conventional and hybrid microcircuit fabrication. At the same time, it is important that over-stress of semiconductor devices and hybrid microcircuits be avoided, since this can cause incipient field failures and also reduce production yields, thus raising life cycle costs.

These potential problems can be avoided by maintaining the closest possible liaison among those responsible for key equipment fabrication and acceptance tasks. It should be recognized that at least four separate organizational entities must be involved technically to assure proper mutual understanding of the reliability improvement tasks; in addition to the contractor and agency quality assurance offices through which they must interface. These are:

- (a) Agency Program Office (PMO).
- (b) Contractor Program Office (PMO).
- (c) Agency Microcircuit Technology Office.
- (d) Contractor Microcircuit Technology Organization.

The Agency and Contractor Microcircuit Technology organizations each have attained a relatively high level of technological understanding concerning the problems and pitfalls resulting from the processing involved, and their collective experience can enhance system reliability by preventing the usage of relatively risky concepts, and by monitoring against the inadvertent imposition of requirements which will overstress the electronics circuitry unnecessarily and inconsistently with respect to actual field needs.

CONCLUSIONS

Hybrid microcircuits have been designed into AN/TPQ-36 Radar Set across a broad spectrum of applications, each chosen to yield specific and sometimes unrelated advantages with respect to size, weight, performance, reliability, and equipment life cycle cost. Successful demonstration of this Radar Set through the Engineering Development Model phase tends to justify these design choices, although the exact role of hybrid microcircuits as a significant reason for success to date becomes difficult to evaluate precisely. In observing hybrid microcircuit usage on systems such as the AN/TPQ-36 Radar Set, it becomes more meaningful to assure that full usage be made of the versatility inherent in hybrid microcircuit technology, so that proper choices may be made between methodologies such as, for example, thick film solder reflow, thick film chip-and-wire, thin film chip-and-wire, and thick film beam-leaded devices. System advantages such as those described above thus will increase in accordance with the degree of background and knowhow through which such decisions are made.

This observation leads to the means by which equipment reliability can be enhanced, as described in the last section above: closer coordination between the agency/contractor program offices and the agency/contractor hybrid microcircuit technology organizations will bring about meaningful and workable specifications, resulting in higher subassembly and assembly yields; and once again improved reliability, together with reduced life cycle costs.

ACKNOWLEDGEMENTS

The author would like to acknowledge the assistance obtained from Hughes Ground Systems Group personnel under the direction of Mr. O.C. Mitchell in obtaining detailed information concerning the electrical and mechanical characteristics of Radar Set AN/TPQ-36. In particular, especially helpful and kind assistance was provided by Messrs. D.H. Baehr, William A. Engle, Carl C. Gebhardt, J.C. Hopkins, Cal Marvin, A.E. Saari, W.L. Scott, and P.A. Taylor.

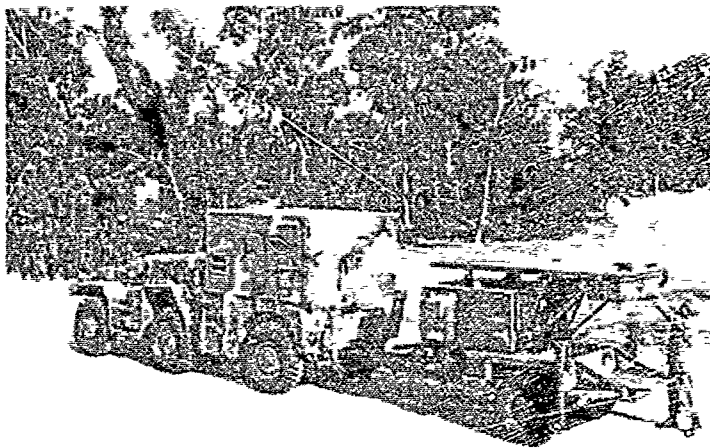


Figure 1. AN/TPQ-36 Transport Mode.

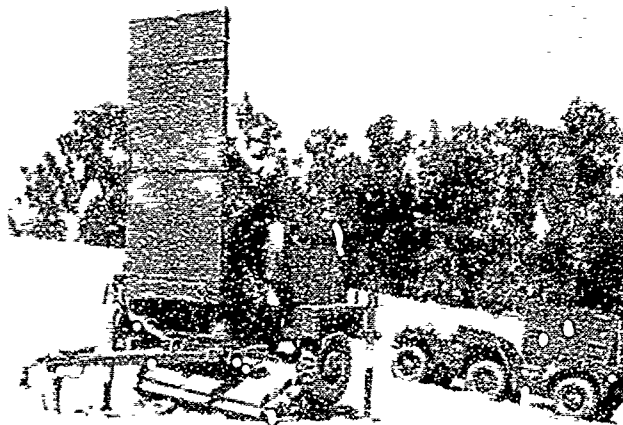


Figure 2. AN/TPQ-36 Deployment Underway.

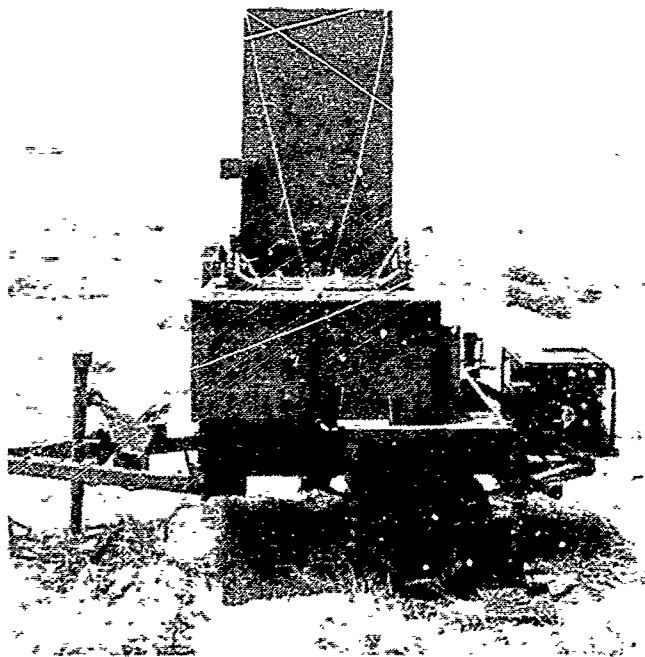


Figure 3. Rear View of Antenna.



Figure 4. Interior of Operations Shelter

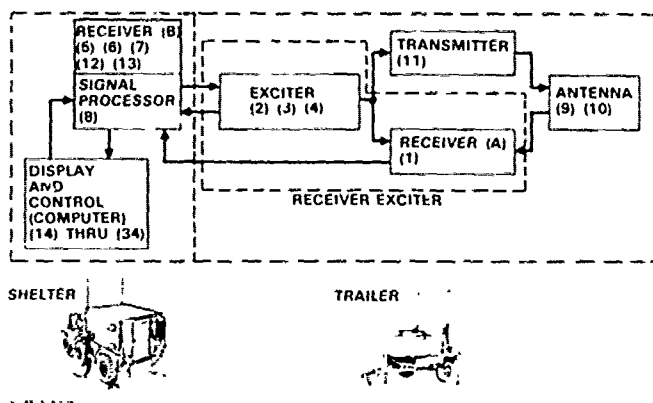


Figure 5. System Block Diagram.

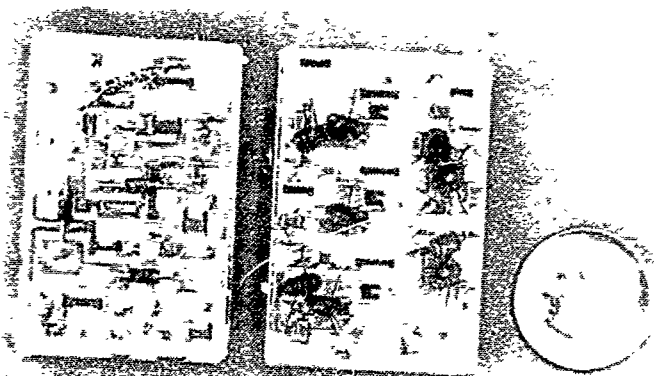


Figure 6. Typical AN/TPQ-36 Solder Reflow Hybrid Microcircuits.

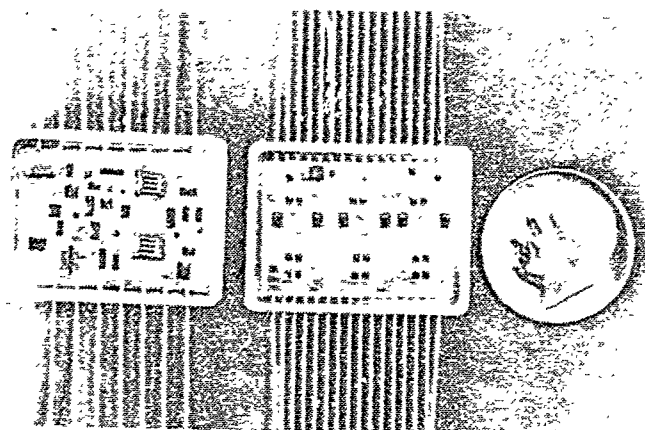


Figure 7. Typical AN/TPQ-36 Chip-And-Wire Hybrid Microcircuits.

Table I.

HYBRID MICROCIRCUIT USAGE FOR THE AN/TPQ-36 RADAR SET HYBRID MICROCIRCUIT LISTING

HUGHES

LOCATION COORD	DESCRIPTION	LOCATION	CONCEPT
1	SENSITIVITY TIME CONTROL (STC) GENERATOR	RECEIVER (TRAILER)	SOLDER REFLOW (THICK FILM)
2	CRYSTAL OSCILLATOR	EXCITER (TRAILER)	SOLDER REFLOW (THICK FILM)
3	OSCILLATOR SWITCH	EXCITER (TRAILER)	SOLDER REFLOW (THICK FILM)
4	POWER AMPLIFIER	EXCITER (TRAILER)	SOLDER REFLOW (THICK FILM)
5	LIMITER	RECEIVER (SHELTER)	SOLDER REFLOW (THICK FILM)
6	PHASE SHIFTER	RECEIVER (SHELTER)	SOLDER REFLOW (THICK FILM)
7	VARIABLE ATTENUATOR	RECEIVER (SHELTER)	CHIP AND WIRE (THIN FILM)
8	HEX FAST LINE RECEIVER	SIGNAL PROCESSOR (SHELTER)	CHIP AND WIRE (THIN FILM)
9	PHASE SHIFTER DRIVER	ANTENNA BEAM STEERING UNIT (TRAILER)	CHIP AND WIRE (THICK FILM)
10	CURRENT REGULATOR	ANTENNA (TRAILER)	CHIP AND WIRE (THICK FILM)
11	OPTICALLY COUPLED ISOLATOR	TRANSMITTER (TRAILER)	CHIP AND WIRE (THIN FILM)
12	VHF/UHF AMPLIFIER	RECEIVER (SHELTER)	CHIP AND WIRE (THIN FILM)
13	ULTRA FAST FET OPERATIONAL AMPLIFIER	EXCITER (SHELTER)	CHIP AND WIRE (THICK FILM)
14 THRU 34	G.P. DIGITAL	AN/UYK-15 COMPUTER (SHELTER)	BEAM LEAD (THICK FILM)

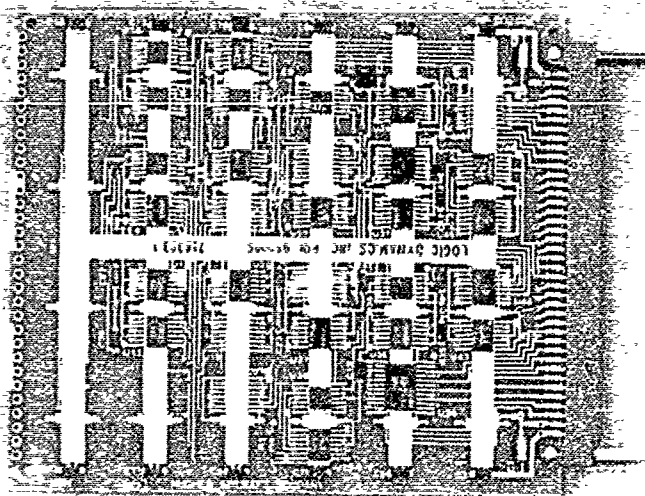


Figure 8. Typical Signal Processor Card.

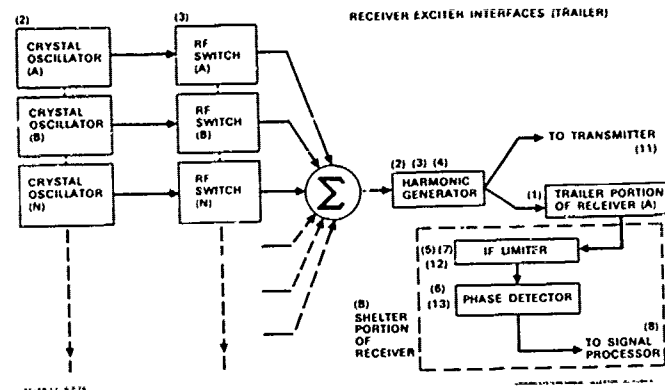


Figure 9. Receiver-Exciter Interfaces.

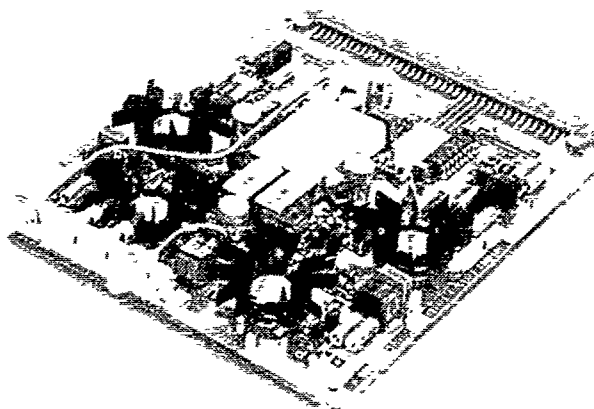


Figure 10. Receiver Phase Detector.

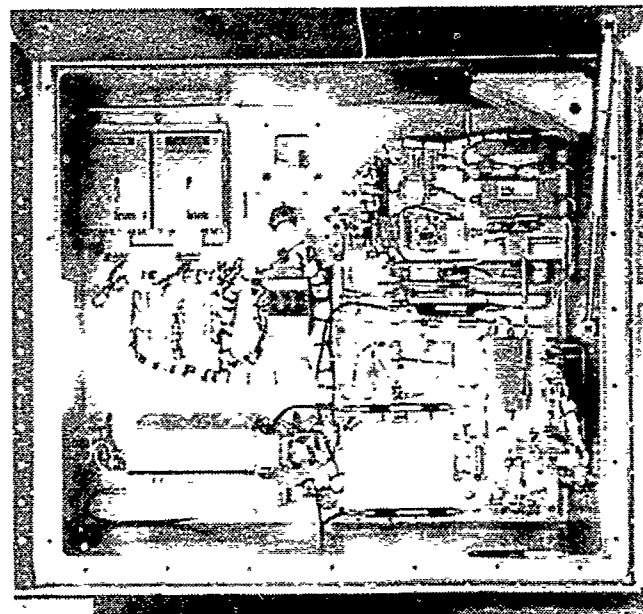


Figure 11. View of Receiver-Exciter Compartment.

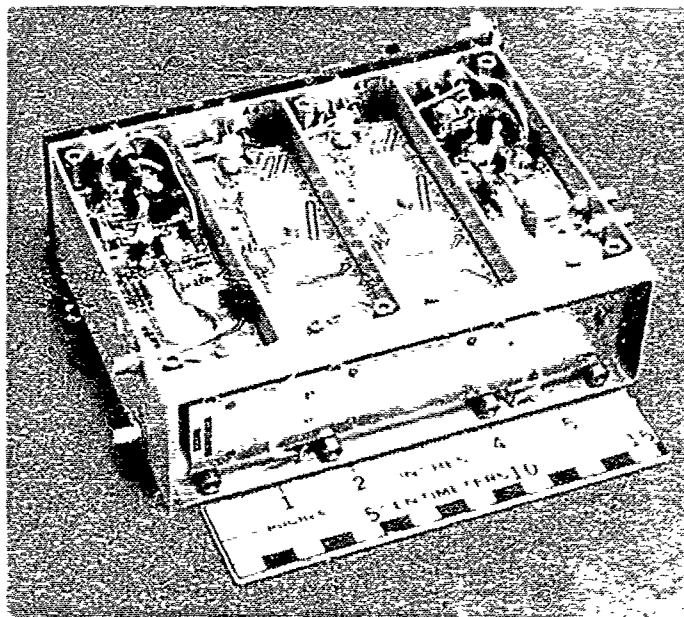


Figure 12. Exciter Oscillator.

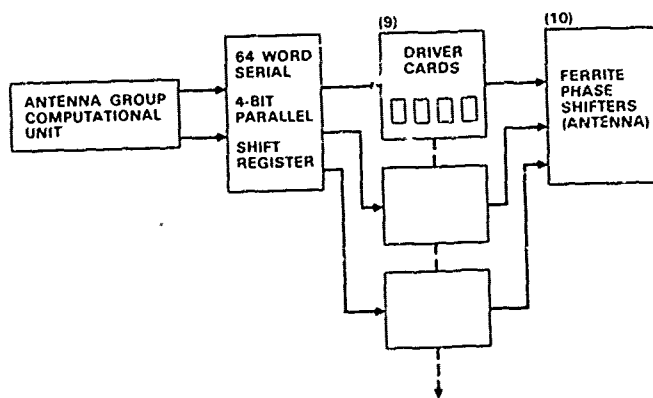


Figure 13. Beam Steering Unit.

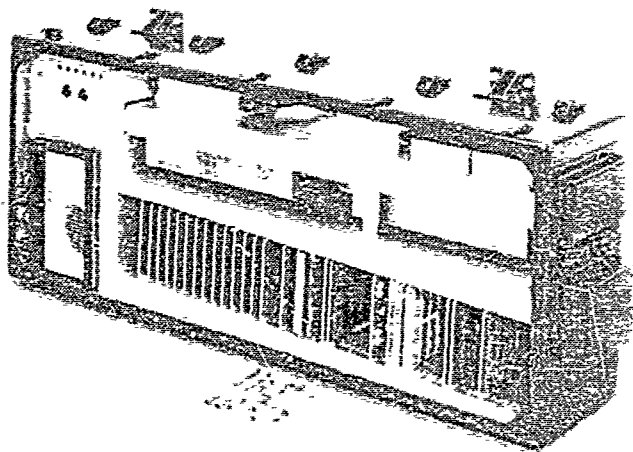


Figure 14. Antenna Beam Steering.

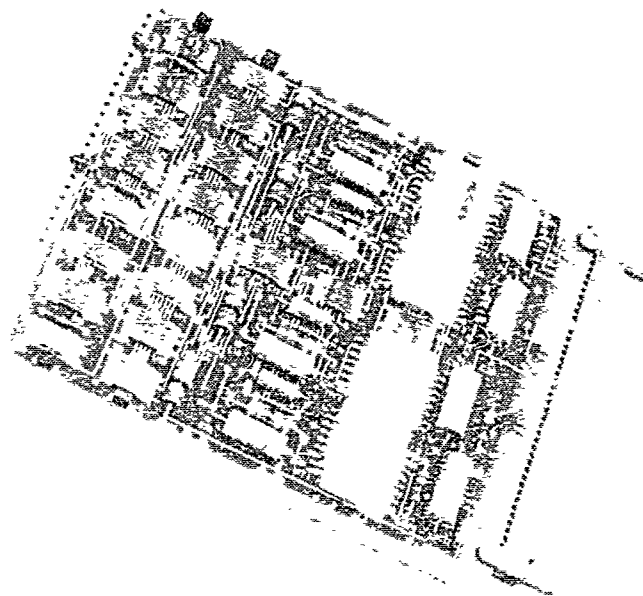


Figure 15. Antenna Beam Steering Card.

PACKAGING DESIGN FOR THE ARMY TACTICAL RADIO SET AN/URC-78*

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ABSTRACT

The performance and size requirements of the Army Tactical Radio Set AN/URC-78 dictated the maximum usage of microelectronic devices and packaging techniques to satisfy the equipment requirement. RCA developed a packaging design that was based on the lowest life cycle cost for this equipment.

This design made maximum use of the standard complex integrated circuit devices in conjunction with other semiconductors and components that were interconnected and packaged with thick film hybrid techniques.

The partition of the circuits for individual hybrid packaging was based on functional requirements, replacement costs, maintenance, and manufacturing yield considerations.

The hybrids were designed with the hermetic seal enclosure and the connectors as an integral part of the same alumina substrate that contained the circuit components. This approach allowed a considerable improvement in the hybrid's volumetric efficiency and reliability since a separate package to contain the alumina substrate was eliminated along with the substrate/package interconnections.

The materials and processes used in the hybrid design were selected on the basis of prior reliability experience and to optimize the electrical performance while maintaining compatibility with the equipment environmental requirements.

Approximately 85% of the circuitry of the Radio Family was packaged in 55 hybrids of both digital and analog types operating from DC to VHF frequencies.

Six hybridized AN/URC-78 equipments were submitted to a rigorous qualification test program which included the equipment environmental requirements. They performed without any hybrid malfunction or degradation.

*Paper unavailable for printing

MILITARY QUALITY CONTROL DOCUMENTS FOR HYBRID MICROCIRCUITS

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ABSTRACT

Hybridization of military electronic functions or subassemblies is relatively new and is still in an evolutionary phase. Performance reliability is highly dependent upon materials and processes. Standardization of military applications is essentially nonexistent. This paper defines aspects associated with granting approval to a manufacturer for the preparation of a hybrid microcircuit drawing or specification for use by the US Army Electronics Command (ECOM), and includes revisions being considered for inclusion in the military control documents for hybrid microcircuit procurement.

INTRODUCTION

The hybrid technology continues to provide the means of assembling circuits for analog, digital, and microwave applications in relatively small enclosures. The enclosure contains an insulating substrate with deposited networks, generally conductors and resistors, to which discrete semiconductor devices, integrated circuits, and passive elements are attached. For many ECOM field equipments now under development, weight and volume specifications are met by utilizing the hybrid assembly technology.

Hybrid and monolithic integrated circuits are generally procured by ECOM under MIL-M-38510 "Microcircuits General Specification for" and MIL-STD-883 "Test Methods and Procedures for Microelectronics." With these documents, standardization of device types is obtained by issuance of MIL-M-38510 detail specifications or "slash" sheets to procure reliable microcircuits.¹ To date, approximately eighty specifications have been issued for various monolithic microcircuits², however, none has been for a hybrid microcircuit.

MIL-M-38510 includes the general requirements for monolithic and hybrid microcircuits along with the quality and reliability criteria which must be met in the procurement of these microcircuits. Details on the quality and reliability requirements, however, are not entirely adequate for hybrid microcircuits since this document was formulated primarily for high volume monolithic integrated circuits. A tri-service committee³ is now in the process of improving screening and qualification procedures for the hybrid microcircuits that are accurate, cost effective, and will assure the reliability requirements for military systems.

DEVICE QUALIFICATION

Provisions are available in MIL-M-38510 to control device procurement using either military detail specifications for qualified (standard) parts or contractor prepared and ECOM approved specifications for nonstandard parts. Both types of specifications have been effective for procuring monolithic devices. For ECOM equipments, and essentially all military equipment, hybrid microcircuits have been procured only as nonstandard parts because no qualified MIL-M-38510 source exists for these types of circuits.

To obtain certification and device qualification, a manufacturer must demonstrate that he possesses the resources and technical capability to fabricate quality microcircuits. He must establish and implement a product assurance program and conduct qualification testing of the specified devices. The qualification process for a standard part and the preparation of a "slash" sheet can take several years. Compromises must be made on which devices to qualify and which devices to qualify first. In addition, it is preferable that selected devices meet at least one of the following: (a) multiple usage, (b) high volume production, or (c) moderate volume and multiple usage. These criteria are not hard and fast rules, but are guidelines. A comparison of hybrid and monolithic microcircuits (Table 1) indicates that military hybrids normally do not meet any of the criteria listed above, particularly volume of production and multiple usage.

NONSTANDARD PART REVIEW AND APPROVAL

When considering the use of a nonstandard part, a requirement is that it should be better than a standard part, or, as for most hybrids, possess unique characteristics which are essential to the proposed use and are not inherent in the standard part.

As ECOM equipment development proceeds through various design phases from conceptual through validation up to full scale production, provisions are made, starting at the advanced development phase, for the preparation and submission of data and the preparation of contractor prepared specifications to insure an adequate level of hybrid microcircuit quality.

The specifications are prepared in accordance with MIL-STD-749 "Preparation and Submission of Data for Approval of Nonstandard Parts." Prior to preparation of the specification, an on-site review is made by ECOM of the equipment contractor's source facilities. To assist the ECOM reviewer, a checklist is used to review the various parts of the manufacturer's processes and facilities. A document is being prepared which contains processing standards which will be used in the future by ECOM as a more rigorous guideline for on-site reviews.⁴

Step I data is the original request by the manufacturer for non-standard part approval with reasons for its use. Along with Step I data, ECOM requires a description of the materials and processes used in

TABLE 1. COMPARISON OF MONOLITHIC AND HYBRID MICROCIRCUITS

	<u>HYBRID</u>	<u>MONOLITHIC</u>
<u>TECHNOLOGY</u>	MULTIPLE	SINGLE
<u>MANUFACTURE</u>	DEVELOPED TO DIFFERENT DEGREES OF MATURITY	PROGRESSION OF ENGINEERING, PILOT PRODUCTION, PRODUCTION
<u>PRODUCTION</u>	LOW VOLUME	HIGH VOLUME
<u>SOURCE</u>	ONE (CUSTOM-BUILT)	TWO
<u>MULTIPLE USAGE</u>	NO	YES

TABLE 2. DESCRIPTIVE INFORMATION REQUIRED WITH STEP 1 DATA

- A. MATERIALS AND PROCESSES
 - 1. PROCESS FLOW CHARTS
 - 2. DESCRIPTION OF FILM NETWORK
 - 3. INTEGRALLY BONDED PARTS
 - 4. DISCRETE PARTS
 - 5. CHIP MOUNTING PROCEDURES
 - 6. WIRE BONDING PROCEDURES
 - 7. SUBSTRATE TO PACKAGE ATTACHING TECHNIQUE
 - 8. PACKAGE DESIGN
 - 9. SEALING PROCESS AND MATERIALS
 - 10. REWORK PROCEDURES
- B. ELECTRICAL, MECHANICAL, ENVIRONMENTAL AND RELIABILITY CHARACTERISTICS OF CIRCUITS
- C. PLANS TO ACHIEVE REQUIRED MICROCIRCUIT RELIABILITY
- D. PROPOSED QUALITY CONTROL MEASURES TO ASSURE MAINTENANCE OF REQUIRED QUALITY LEVELS

the fabrication of each hybrid microcircuit in sufficient detail to indicate suitability and compatibility for the intended application. Table 2 includes the descriptive information required from process flow charts through rework procedures. Also required are the effective plans for achieving the microcircuit reliability corresponding to the level of reliability specified for the equipment and proposed quality control measures to assure maintenance of required quality levels.

The contractor prepared specification which constitutes the Step II data of MIL-STD-749 should be as complete and as rigorous in both content and format as similar available MIL- Specifications. Table 3 lists the ECOM requirements for inclusion in the specification. A similar listing of requirements for the preparation of such specifications has been added to MIL-M-38510 as Appendix F.

Step III test data must be available to provide evidence of circuit compliance with the requirements of the specification. This, along with Step I and Step II data, is required before the specification will be accepted into the system as a procurement document.

PACKAGING

Hybrid microcircuits are packaged normally in hermetically sealed enclosures to satisfy environmental and life requirements. These circuits are subjected to tests of methods 5004 and 5005 of MIL-STD-883. Method 5004 establishes the screening procedures for the hybrid microcircuits and defines three reliability classes (A, B, & C) of parts for achievement of levels of quality and reliability commensurate with intended application. Devices for ECOM equipment are normally tested under Class B; the class where maintenance is difficult and reliability is vital. Method 5005 includes Group, A, B, C, and D tests and is intended for initial circuit qualification, requalification when required, and retention of qualification. Group A and B tests are intended for quality conformance inspection of individual inspection lots as a condition for acceptance for delivery, whereas Group C and D tests are carried out periodically (every 3 and 6 months, respectively).

Of concern has been the relative capability of larger size packages to withstand certain levels of MIL-STD-883 environmental tests originally recommended for smaller integrated circuit packages. Recent development work has determined stress limitations of some hybrid packages (up to 1 inch by 2 inches)* in terms of these environmental tests.⁵ Bomb pressure and moisture resistance tests indicated that screening effects were taking place on all packages. For the other tests, there was no positive proof of screening capability; for example, most packages went through the temperature cycling without trouble, whereas acceleration tests affected all parts uniformly. Additional experimentation is required to determine exact screening limits and requirements for large size packages.

*See last page for metric equivalent units.

TABLE 3. HYBRID MICROCIRCUIT SPECIFICATION (NONSTANDARD PART)
REQUIREMENTS

<u>GENERAL</u>	<u>FABRICATION</u>
CIRCUIT NOMENCLATURE AND FUNCTION	DESIGN, CONSTRUCTION, AND PHYSICAL DIMENSIONS*
PART NUMBER	PHYSICAL LAYOUT - CIRCUIT ORIENTATION
DEVICE CLASS	REWORK*
ABSOLUTE MAXIMUM RATINGS	CASE OUTLINE - DIMENSIONS AND TOLERANCES*
SUPPLY VOLTAGE RANGE	LEAD MATERIALS AND FINISH*
STORAGE TEMPERATURE	MARKING*
POWER DISSIPATION	CHANGE NOTIFICATION (MATERIALS, PARTS, PROCESSES)
LEAD TEMPERATURE	
AMBIENT OPERATING TEMPERATURE	
RECOMMENDED OPERATING CONDITIONS	<u>COMPONENT REQUIREMENTS</u>
<u>ELECTRICAL CRITERIA</u>	ELECTRICAL VALUES AND TOLERANCES
CIRCUIT SCHEMATIC	ADD-ON PARTS - PROCUREMENT SPECIFICATIONS
BLOCK DIAGRAM AND TERMINAL CONNECTIONS	
ELECTRICAL PERFORMANCE CHARACTERISTICS	<u>PRODUCT ASSURANCE PROVISIONS**</u>
ELECTRICAL TEST REQUIREMENTS	SCREENING - QUALITY CONFORMANCE
REQUIRED ELECTRICAL TEST CIRCUITS	
BURN-IN AND LIFE TEST CIRCUITS	

*MIL-M-38510 } UNLESS SPECIFIED AND
**MIL-STD-883 } APPROVED BY ECOM

TABLE 4. HYBRID MICROCIRCUIT MATERIALS AND PROCESSES

<u>NETWORK FABRICATION</u>	<u>SUBSTRATE MOUNTING</u>	<u>DEVICE ATTACHMENT</u>	<u>LEAD ATTACHMENT</u>	<u>LID SEALING - PACKAGING</u>
<u>FILM TECHNOLOGY TYPES</u>	<u>TYPES</u>	<u>TYPES</u>	<u>TYPES</u>	<u>TYPES</u>
THIN THICK	AL ₂ O ₃ BEO	ACTIVE PASSIVE	WIRE	FLATPACK
<u>CONDUCTORS</u>	GLAZED UNGLAZED	FACE UP METAL TAB BEAM LEAD	RIBBON BEAM	METAL PLUG-IN TO TYPE HEADER SUBSTRATE BASE
NI Pd AG AU AU CR Pt AU CU Pd AU	<u>MOUNTING</u>	FACE UP RIBBON LEAD BEAM LEAD END METAL	<u>MATERIAL</u>	<u>SEAL</u>
<u>RESISTORS</u>	SOLDER CONDUCTIVE ADHESIVE NONCONDUCTIVE ADHESIVE	<u>MOUNTING</u>	AU AL	<u>HERMETIC</u> <u>NONHERMETIC</u>
NI-CR RU O TA PD-BASE TAN PT-BASE		EUTECTIC AU-SI AU-GE AU-SN	<u>BOND</u> TCB US WOBBLER	SOLDER WELD POLYMER SEAL ENCAPSULANT
<u>DIELECTRICS</u>		AG CEMENT CONDUCTIVE ADHESIVE NONCONDUCTIVE ADHESIVE BEAM SOLDER		
SiO GLASS TITANATE				

MIL-M-38510 does not permit delidding of the package seal after circuit completion and evaluation. Because of the complexity and relative cost of many completed hybrid packages, lid removal and rework has been under consideration. An evaluation of techniques for sealing large hybrid packages indicated that very few of the package types could be resealed with any degree of confidence regardless of the method by which they were sealed.⁶

ECOM discourages the use of polymer sealed or encapsulated packages in Army equipment because of uncertainty in storage and operating life of circuits in such enclosures; however, to be responsive to industry developments, continuing efforts are being made to assess the risk of such packages for ECOM equipments, particularly for discrete semiconductor devices.

Packages sealed with polymer adhesive when compared to the conventional welding, brazing, and solder sealing processes have advantages for the hybrid manufacturer including good rework capability and lower temperature sealing processes. Packages sealed with polymer adhesive have retained their seal integrity as determined by the MIL-STD-883 helium seal test after having been subjected to thermal shock, temperature cycling, mechanical shock, and constant acceleration test environments;⁷ however, this does not negate the fact that gases such as water vapor can permeate through such organic seals within limited time periods,⁸ adding uncertainty to the electrical behavior and life of moisture sensitive components.

Discrete semiconductor devices intended for most consumer and industrial applications are predominantly encapsulated in plastic packages. To a limited degree, hybrid microcircuits are encapsulated for industrial applications. Evaluation of intrinsic properties of polymer coated materials and their interactions with thick-film hybrid circuit materials (passive parts only) under several regimes of environmental stress indicated that none provided the protection achieved by hermetic sealing.⁹ For the discrete semiconductor devices, storage and operating reliability characteristics are still uncertain, varying with process and plastic, with the failure rate for such devices being ten times greater than hermetically sealed ceramic-metal packages. The problems inherent with plastic packaged semiconductors are translated to an encapsulated hybrid microcircuit with certain problems compounding when the circuit complexity increases. Of particular concern are open or intermittent bonds, susceptibility to moisture and impurities in the encapsulants, and cracking of the package when flexed on a circuit board.

MATERIALS AND PROCESS CONTROLS

Hybrid technology includes a broad range of microcircuit types, materials, and processes. Two general network processes (thin- and thick-films) are utilized as the planar interconnection means for integrally bonded or discrete (cased, uncased, encapsulated) parts. Other

significant processes, with various approaches, include device attachment, lead attachment, mounting of substrates, lid sealing, and packaging. Table 4 is a listing of the predominant materials and processes (except for nonhermetic packages) which are used in ECOM hybrid microcircuits; with the listing probably representative for all military hybrids. A thorough listing of materials and processes used for this technology would be more extensive.

A large number of vendors supply hybrid microcircuits for military use. Most manufacturers are familiar with the basic processes and their defined approaches; however, the specific process parameters employed or controlled during circuit fabrication may vary from one manufacturer to another and are not readily available. The reliability of these circuits is highly process-oriented and difficult to establish.

Specification and quality control at the material and process level is relatively limited as reflected in the military control documents. In fact, the present quality assurance exemplified by MIL-M-38510 emphasizes device post-production screening and qualification testing. For hybrid microcircuits, this procedure can be very costly in testing expense and network yields, since exceeding a specified percent defective allowable may result in scrapping a product lot at the point where the hybrid microcircuit includes the maximum cost of both materials and labor. Such a concept can be tolerated for discrete devices made in large volume but not for the normal military custom built hybrid microcircuits. In addition, tests must be conducted frequently below MIL-STD-883 minimum conditions because of the limitations of a material or a part in the circuit, adding a further note of uncertainty to the screening and quality conformance inspection. As substrates become larger (4 inches by 5 inches) and circuits more complex, control at the process level will become mandatory because of the unsuitability of certain post-manufacturing screens.

A flow diagram (Figure 1) indicates the various areas in the manufacture of a hybrid microcircuit from the circuit schematic through delivery. Essentially each part of this diagram is referred to in either MIL-M-38510 or MIL-STD-883; however, the level of control specified varies for different areas. Specific and detailed controls are defined primarily for screening and quality control of the packaged unit as indicated above. Although the remainder of the boxes may require some form of product assurance documentation by the manufacturer, there are very limited specified details as to what aspects of the hybrid microcircuit to control, to what extent, and in what manner.

Detailed in-process controls are required in the fabrication area. Such details are required to enhance the concept of building-in reliability and reducing dependence on the concept of screening-out unacceptable circuits. The parts of the process which are most critical and which require maximum control must be determined for this to succeed. From this, it must be determined what balance of process control and post-seal screening will economically give the required quality and reliability.

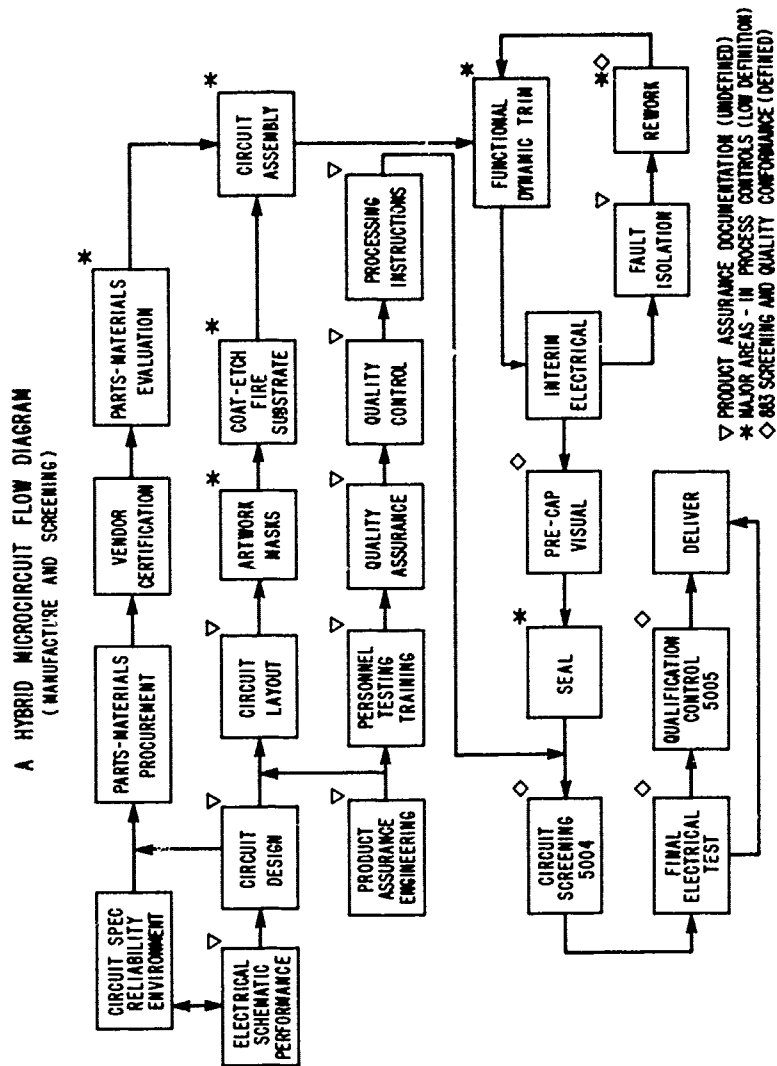


Figure 1

NEW TEST PROCEDURE—Method 5008

A new hybrid microcircuit test procedure (Method 5008) is being coordinated with industry by the tri-service committee³ prior to inclusion in MIL-STD-883. The procedure establishes screening, quality conformance, and qualification procedures for the testing of hybrid microcircuits and consists of a single level of testing in contrast to the conventional three-product assurance levels of Methods 5004 and 5005. Method 5008 relates to hybrid packages which have an inner seal perimeter of 2.0 inches or greater, whereas packages with perimeters of less than 2.0 inches will continue to be screened and qualified in accordance with Methods 5004 and 5005. The intent is to define quality and reliability requirements which are amenable to the larger hybrid microcircuit packages and are separate from the testing sequences where principal emphasis is on silicon monolithic circuits.

Quality control records for a hybrid microcircuit fabrication line have shown that active devices and wire repairs are the major causes of hybrid microcircuit rework (prior to package sealing), whereas failure analysis reports have indicated that active devices, wire bonds, and contamination are the major failure causes for low power hybrid microcircuits which have been screened to MIL-STD-883 Method 5004 Class B prior to delivery.¹⁰ Method 5008 includes a number of tests to insure that at least a minimum degree of screening is carried out in these critical fabrication areas of military hybrid microcircuits. Screening and qualification procedures of Methods 5004 and 5005 are compared with those of Method 5008 in Table 5.

To indicate some of the major changes in the new hybrid microcircuit procedure, tests have been divided into preassembly, in-process, and post-assembly sections. Preassembly tests include package qualification and dc electrical test of all semiconductor and integrated circuit chips. It is anticipated that probing of all chips is just a first step when selecting and testing semiconductor devices along the fabrication line to reduce the amount of pre-seal circuit rework and post-seal circuit failure due to active device problems. To reduce testing cost, packages used for large hybrids will be qualified with a substrate only in the package, without deposited or attached components.

The relatively large hybrid packages eliminate the use of high (30,000) g accelerations because of the inability of the large substrates to tolerate levels much higher than 7,000 g. The stress for post-assembly acceleration testing of the large packages has been reduced to condition A (5,000 g). Mechanical shock is optional upon approval of the procuring activity. To compensate for this change, bond and die shear strength tests have been added as in-process interconnection and device attachment manufacturing controls. The manufacturer will have the option of using destructive or nondestructive pull testing to determine wire bond integrity. The die shear strength will determine the integrity of materials (solder, eutectic, or polymer) used for attaching active and passive components to the substrates.

TABLE 5. SCREENING AND QUALITY CONTROL PROCEDURES

<u>TEST</u>	<u>METHOD 5004-5005 CLASS B</u>	<u>METHOD 5008</u>
<u>PREASSEMBLY</u>		
PACKAGE QUALIFICATION - GROUP D (SUBSTRATE ONLY - NO DEPOSITED OR ATTACHED COMPONENTS)	No	Yes
DC ELECTRICALS (ALL SEMICONDUCTOR AND INTEGRATED CIRCUIT CHIPS)	No	Yes
<u>IN-PROCESS</u>		
BOND STRENGTH	No	Yes
DIE SHEAR STRENGTH	No	Yes
<u>POST-ASSEMBLY (PRE-SEAL)</u>		
PRE-SEAL BURN-IN	No	Yes
INTERNAL VISUAL	Yes	Yes
<u>POST-ASSEMBLY (POST-SEAL)</u>		
STABILIZATION BAKE	Yes	Yes
TEMPERATURE CYCLING	Yes	Yes
CONSTANT ACCELERATION	(30,000 g) Yes	(5,000 g) Yes
BURN-IN	Yes	Yes
SEAL	Yes	Yes
FINAL ELECTRICAL	Yes	Yes
GROUP A (ELECTRICAL)	Yes	Yes
GROUP B (MECHANICAL)	Yes	Yes
PARTICLE IMPACT ACOUSTICAL NOISE TEST	No	Yes
GROUP C (DIE RELATED)	Yes	Yes
FREEZE-OUT TEST (NiCr RESISTORS)	No	Yes
GROUP D (PACKAGE RELATED-ALL DEVICES IN PACKAGE)	Yes	No

A new Method 5008 test procedure, pre-lidding burn-in, should prove to be effective in screening the hybrid microcircuit so that higher yield may be obtained. The manufacturer, after approval of the procuring activity, has the option of dividing total minimum burn-in time between pre-seal and post-seal burn-ins, if the total burn-in time equals or exceeds the specified burn-in time (160 hours) and the post-seal burn-in equals or exceeds 96 hours. The stabilization bake may be deleted from the screening procedure when pre-seal burn-in is performed.

The majority of contaminants in a hybrid microcircuit package are particulates normally which result from limited process controls. The particulates may be either metallic or nonmetallic. A particle impact acoustical noise test has been added under Group B testing to detect loose particles inside the package.

A new freeze-out test has been added to the Group C tests for circuits containing thin-film nichrome resistors to insure that the resistors are suitably passivated against any moisture in the package as unpassivated thin-film nichrome resistors are subject to an anodic dissolution at potentials above 2.5 V.¹¹

CONCLUSIONS

Hybrid microcircuits are procured for ECOM equipments under contractor prepared and ECOM approved specifications. Standardization of these circuits is nonexistent. The circuits are fabricated, screened, and qualified in accordance with MIL-M-38510 and MIL-STD-883 requirements. Hybrid microcircuit revisions and updating of these documents are underway with a new proposed hybrid microcircuit test procedure (Method 5008) soon to be incorporated into MIL-STD-883. A new military hybrid microcircuit specification will probably evolve as new testing procedures and related control documents are established.

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METRIC EQUIVALENT UNITS

<u>INCHES</u>	<u>mm</u>
1	25.4
2	50.8
4	101.6
5	127.0

THE APPLICATION OF HYBRID MICROCIRCUITS IN THE SPACE SHUTTLE AVIONICS SYSTEM

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ABSTRACT

A discussion is presented on the application of hybrid microcircuits in NASA's Space Shuttle, a reusable vehicle which has flight characteristics of both an aircraft and a spacecraft. Usage of hybrid microcircuits in the Shuttle's avionic system is large, varied and widespread in order to meet the need for functional redundancy and self check-out. Cost considerations and short delivery schedules required the use of off-the-shelf system hardware where possible, and where reliability could be proven. As a consequence, a large number of microcircuit vendors and fabrication techniques are involved. MIL-M-38510 and MIL-STD-883 were imposed to the maximum extent possible and augmented by special techniques to improve quality and reliability. Specific controls were negotiated on a case-by-case basis, where necessary, depending on the method of manufacture and the degree of rework allowed. Fundamental questions concerning the limits and extent of rework are covered and apply to other programs if large, expensive hybrid microcircuits are involved. The first large scale use of PIND (Particle Impact Noise Detection) testing was made as a result of conductive particulate contamination failures which occurred with certain integrated circuits in the Apollo Program. It has proven to be quick, reliable, and low cost method for eliminating the problem in flight hardware.

INTRODUCTION

On the morning of July 20, 1969, a message was transmitted to the planet Earth from 250,000 miles in outer space. It was-----"Houston.... The Eagle has landed". That terse, but historic message culminated a long and intense effort by this country to assert its technical superiority in a new field and to thereby regain its pride. It marked the beginning of the end of the golden era of space exploration and gave birth to a new age which would be based on utilitarian objectives rather than national goals. The new phase would concentrate on the exploitation of space instead of exploration and cost would be a dominant factor in its implementation. The program was named the Space Shuttle and this paper will describe the role hybrid microcircuits are playing in its development.

COST CONSIDERATIONS

The significance of cost in space exploration is typified by figures 1 and 2. Here we see that in early space programs, mission success was

the highest in priority and cost was the lowest. However, in later programs cost moved up in priority until now, with the Shuttle Program, it is almost in second place.

The Mercury, Gemini, Apollo and Skylab space programs were characterized by several factors which, though necessary at the time, were quite costly. These factors are listed in figure 3 and are the ones which the Shuttle Program will either eliminate or greatly minimize.

The most fundamental difference in the Shuttle vehicle is that it is reusable (up to 100 missions) and thus its high development cost can be amortized over many flights. It is also capable of lifting a large payload into Earth orbit and of returning it to Earth. This reduces the cost-per-pound of payloads low enough to be available to a wide variety of users who are interested in non-scientific activities such as space manufacturing.

The large launch and mission control crews are a luxury that the Shuttle Program cannot afford. Instead, the vehicle will be almost entirely self-sufficient and will therefore have a greater dependency on automatic electronic systems than ever before. Special diagnostic circuits will check each flight system continuously to detect malfunctions and to indicate them to the crew.

Elimination of the sea-borne recovery forces is made possible with the Shuttle vehicle by using land recovery techniques that are common to aircraft. As in previous programs, re-entry will be computer controlled, but in the case of the Shuttle, it will include the glide path and touchdown as well. Unlike conventional aircraft, the Shuttle vehicle has no go-around capability and will land dead-stick. As such, it must land perfectly each time.

CHARACTERISTICS OF THE VEHICLE

The Space Shuttle is a unique combination of spacecraft and aircraft; literally a spacecraft with wings. It is launched vertically (figure 4) with the aid of two solid-rocket boosters which are jettisoned later (figure 5), recovered by parachute, refurbished, and reused on subsequent flights. The liquid hydrogen-oxygen fuel for the Shuttle's main engines from lift-off to orbit insertion is supplied by a large external tank which is under the vehicle. This tank is also jettisoned but is not recovered. Re-entry is achieved with a nose-high attitude in the aerodynamic heating region (figure 6). It then rotates to a slight nose-down attitude in the denser portion of the atmosphere to improve the vehicle's glide characteristics. Landing will occur at about 200 mph on a special 17,000 foot long runway at the Kennedy Space Center (figure 7). The vehicle can be completely refurbished and ready for another flight in approximately 14 days.

AVIONICS SYSTEM DESIGN CHARACTERISTICS

The factors which reduce the operational cost of the Space Shuttle vehicle are also those which have a direct bearing on the design of its avionics system. These characteristics are shown in figure 8 and, in general, cause the system to be much more complex than usual.

Since the vehicle functions at various times as either an aircraft or a spacecraft, it must carry the normal complement of electronic equipment for each (i.e., TACAN, automatic landing and braking systems, and inertial navigation, star trackers and computers). Except for a few common items, such as communication equipment, this requirement almost doubles the amount of flight hardware that is usually carried.

The automatic check-out capability provides a status check of all critical equipment to verify their operation. This places an added circuit design burden in each system which must be accommodated in as little volume as possible. It is, however, a fundamental requirement that is necessary if the vehicle is to be truly divorced from ground assistance.

Systems reliability is achieved through multiple redundancy and permits the equipment to fail twice to backup operational modes before it fails to a final, safe condition. In some cases, this redundancy is obtained from completely separate systems and in others, it is through redundant internal circuits. High reliability pieceparts are used wherever possible, but the emphasis is on use of level "B" of MIL-M-38510 quality rather than on the more costly level "A".

A coaxial data bus is used in the avionics system, instead of dedicated wires, to minimize cable weight. This system used coded messages to communicate with each major piece of hardware, and over this party-line flows commands, timing signals, status information, and other data. Each piece of hardware has an internal miniaturized transmit-receive system plus special signal processors to enable it to communicate with the data bus. By necessity, the bus communication system must be small to minimize the volume required of each piece of hardware in which it is placed.

The above considerations not only justify the use of hybrid microcircuits in the avionics system, but makes it absolutely necessary. Without it, the functional density required of the system would not be possible in a reasonable volume and weight. Fortunately, the growth in hybrid microcircuit technology coincided with that of the Shuttle vehicle and it is therefore being used to a large extent.

HYBRID MICROCIRCUIT APPLICATIONS

The degree to which hybrid microcircuits are being applied in the Shuttle avionics system is shown in figure 9. It represents the largest total number and configuration types known to the writer thus far for a single system.

It should be noted that a particularly large amount of the Shuttle hybrids are either off-the-shelf items or are in off-the-shelf hardware. The use of off-the-shelf hardware, where possible, was dictated by cost considerations. Where the exact hardware was not available, a modification of the basic design was used, and where neither was available, the systems were custom designed.

The numbers of hybrid microcircuits vendors involved thus far is 29 and this quantity is expected to increase in the near future as are the number of subsystem manufacturers which are using the microcircuits. Figure 10 lists the various vendors which are presently being used along with the number of circuit configurations and total quantity for each shipset. A review of the list will show that there are wide variations in the quantity each vendor supplies and this somewhat typifies the hybrid microcircuit industry today. The trend is expected to persist in the future and raises basic questions of control and the need for a comprehensive specification for large programs.

As would be expected with the large number of vendors which are involved, almost every conceivable combination of hybrid microcircuit fabrication techniques is used in the Shuttle devices. Figure 11 contains a partial listing of the basic construction variations. Quantity-wise, thick-film circuits outnumber thin-film circuits by 2:1 and primarily use single layer metallization construction. Also, with few exceptions, single substrates are used in the packages. The overwhelming technique for die attach is non-conductive epoxy. It greatly facilitates chip removal for repair procedures and has excellent strength. Wire bonding is predominantly by an ultrasonic process. The thermo-compression bonding process is also used to a large degree and in some off-the-shelf equipment small amounts of conductive epoxy have even been employed. Flatpacks, usually 1" x 1" and to much lesser extent 1.25" x 1.25", comprise the largest volume of packages used in the Shuttle. The most common form of sealing is by edge welding. It has proven to be an extremely reliable and high yield process and is expected to replace the eutectic method for large packages. At present, neither coating nor potting of hybrid microcircuits is required by the Space Shuttle Program, although it is being performed by two vendors of off-the-shelf hardware.

A summary of the characteristics of the most complex Shuttle microcircuit, the transmit/receive hybrid, is shown in figure 12. It is manufactured by two different vendors and each uses a different technique. The thin-film version is shown in figure 13 and the thick-film version is shown in figure 14. The thick-film version appears to have a simple layout, but it is only because multiple layers of metallization have been used. It is also distinguished by having its active devices mounted on a small separate substrate. This technique involves additional wire bonds, but minimizes rework because the active devices can be thoroughly tested before the small substrate is mounted on the larger one.

Figures 15 and 16 represent the most common type of hybrid microcircuit which is used in the Shuttle avionics system. These circuits are digital logic modules and are constructed with thick-films.

HYBRID REWORK PHILOSOPHY

Cost considerations have caused the Shuttle Program to carefully analyze the philosophy which governs delidding and rework. This topic was carefully reviewed with each Shuttle microcircuit vendor and the findings are reflected in figure 17.

Rework appears to be characteristic of hybrid microcircuit technology at least at this stage of its maturity. The chief cause of rework is the active device because it usually can only be tested to dc parameters at room temperature. Attempts to specify better quality devices, or to have additional tests performed, have been only minimally successful. In most cases, the chip supplier charges a prohibitive amount to perform additional tests and it is therefore left to the vendor to perform his own testing. It is also apparent that more complex tests are very difficult to perform with unpackaged devices and that few hybrid microcircuit vendors have the equipment to do the comprehensive testing that is necessary.

The breakover point of determining whether a hybrid microcircuit should be delidded and reworked is about \$100.00. Below that amount, it seems that little can be gained because of the high cost of recycling the circuits back through the electrical and environmental tests. In the Shuttle Program, only the larger microcircuits are delidded and repaired.

Although the use of epoxy is forbidden in MIL-M-38510, we have found it to be entirely acceptable because it enables chip components to be removed and replaced with a minimum of effort and degradation to the circuit. Its use in large-area hybrids, which have many chips, is necessary because eutectic die mounting is not practical.

Removal of welded lids is a relatively new practice, and one which has been done with excellent success under controlled conditions. Once the seal perimeter has been prepared, it can be rewelded as well as the original surface. Some vendors have found that the process can be repeated as many as five times or as long as a good mating surface can be obtained. The Shuttle Program limits delidding to three times, maximum, and experience has indicated that it is not commonly done more than once and rarely, if ever, a second time. Delidding with a eutectic seal is also possible, but is not nearly as successful as welding.

Rework of large, expensive hybrids which failed in the field was a new and unanticipated requirement for the Shuttle Program, but is being done for reasons of cost. The parts are handled in the same manner as inhouse failures and are subject to the same restrictions as they were when originally manufactured. The significance of this unique operation is that

it has little precedent and therefore is not adequately covered by existing control specifications which were designed for in-plant use. Nevertheless, it is a problem that all users of microcircuits will have to cope with in the future because the trend of industry is clearly toward large, expensive hybrids.

PIND (particle impact noise detection) testing was imposed on the hybrid microcircuits for the Shuttle Program because of hardware failures which have occurred with integrated circuits in previous programs. It was felt that the hybrid microcircuits would be more susceptible to conductive particulate contamination than integrated circuits because (1) more separate operations are performed on them, (2) many different materials are involved, and (3) the package volume is quite large. Estimates from various Shuttle vendors about their anticipated test loss ranged as high as 40% in one case. In reality, however, it turned out to be an average of 16% at the start of the program and is now down to less than 5%.

The test was accepted somewhat reluctantly by the vendors at first, but has since proven its worth. It, for the first time, provided hard data on an industry-wide problem, and more than anything else, has been responsible for causing manufacturers to improve their package cleaning techniques prior to sealing. The test is simple, quick, non-destructive, low in cost, and can be performed by relatively unskilled personnel. Equipment to perform the test is available and reasonable in cost (\$2500). Of 17,000 parts which have been tested thus far, only two possible escapes have been identified. Use of the technique is being adopted by other Government agencies and a military specification of the technique is in preparation.

SUMMARY

The application of hybrid microcircuits in the avionics system of the Space Shuttle represents one of the largest and most diverse uses of the technology to date. It enables this highly sophisticated system to achieve the functional density, which is necessary for its unique operation, in a minimum amount of volume and weight. Some unusual reclamation techniques have been adopted to minimize cost where large circuit modules are concerned and have proven to be successful when properly controlled. The first large-scale use of particle testing was employed and it was found to be an effective means for reducing failures in flight hardware.

MERCURY-GEMINI PRIORITIES APOLLO PRIORITIES

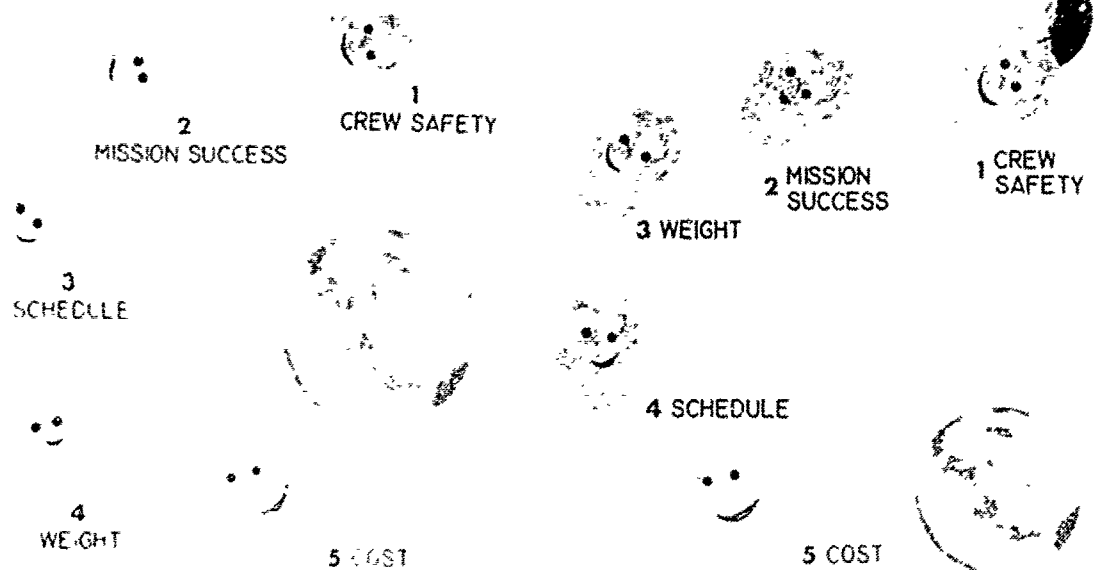


FIGURE 1 - EARLY SPACE PROGRAM PRIORITIES

SKYLAB-ASTP PRIORITIES

SHUTTLE PRIORITIES

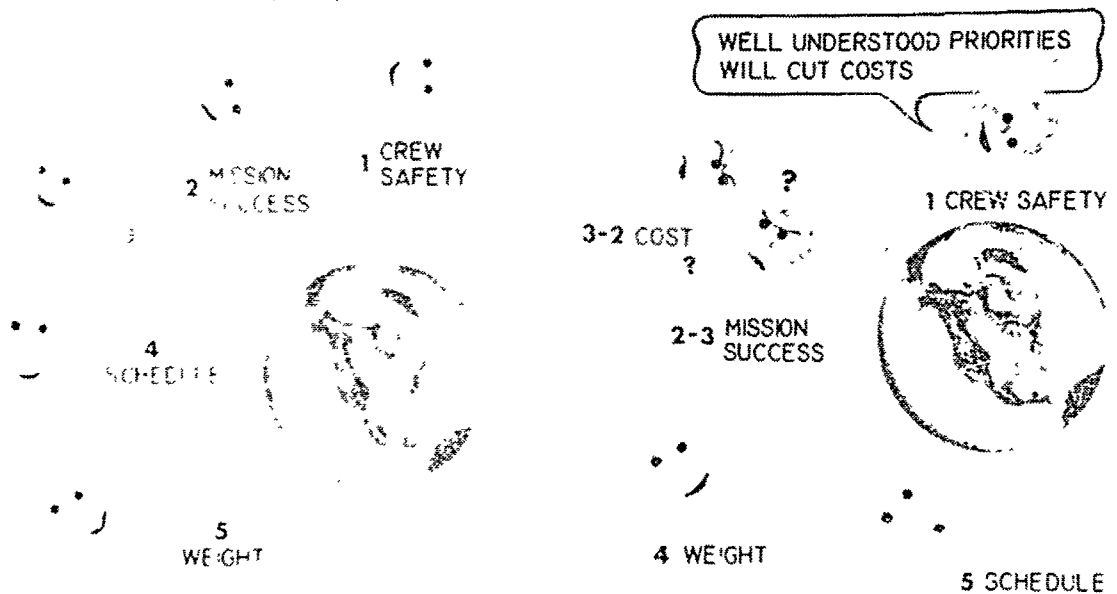


FIGURE 2 - LATER SPACE PROGRAM PRIORITIES

- o SINGLE-USE LAUNCH AND CREW VEHICLES
- o LIMITED PAYLOAD CAPABILITY
- o LARGE LAUNCH AND MISSION CONTROL CREWS
- o LARGE SEA RECOVERY FORCE

FIGURE 3 - HIGH COST FACTORS OF EARLY SPACE EXPLORATION

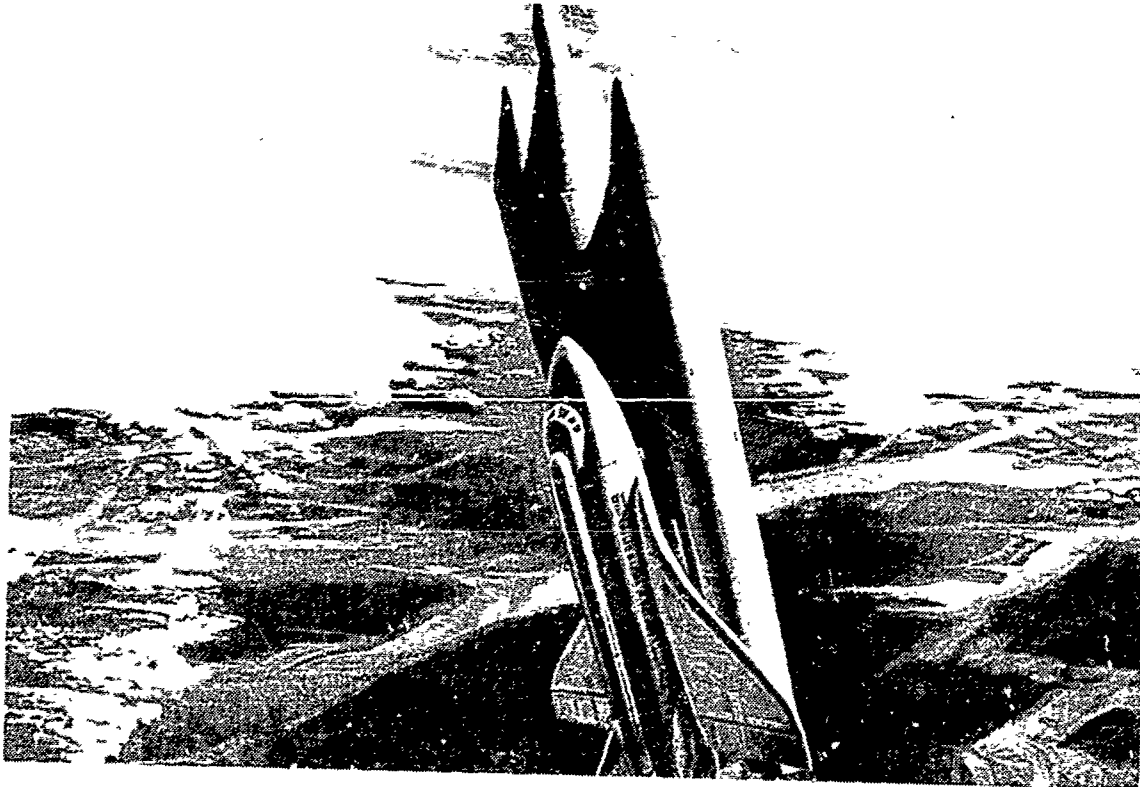


FIGURE 4 - VERTICAL LIFT-OFF AT KENNEDY SPACE CENTER

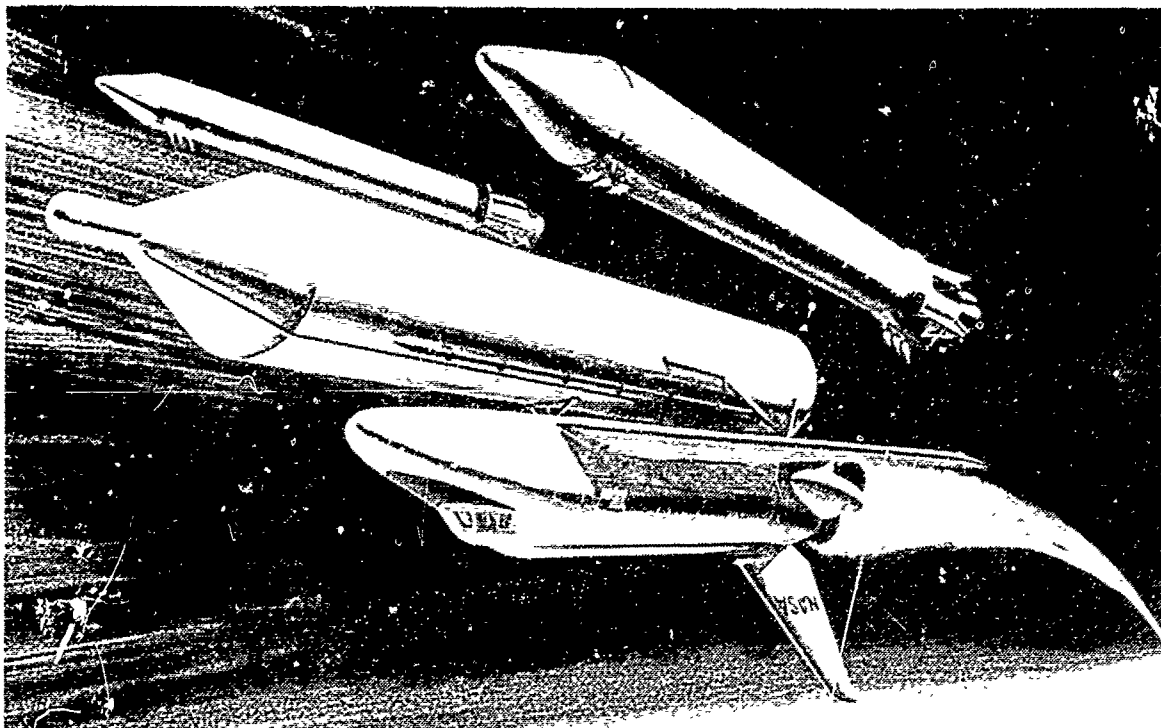


FIGURE 5 - JETTISON SOLID ROCKET BOOSTERS

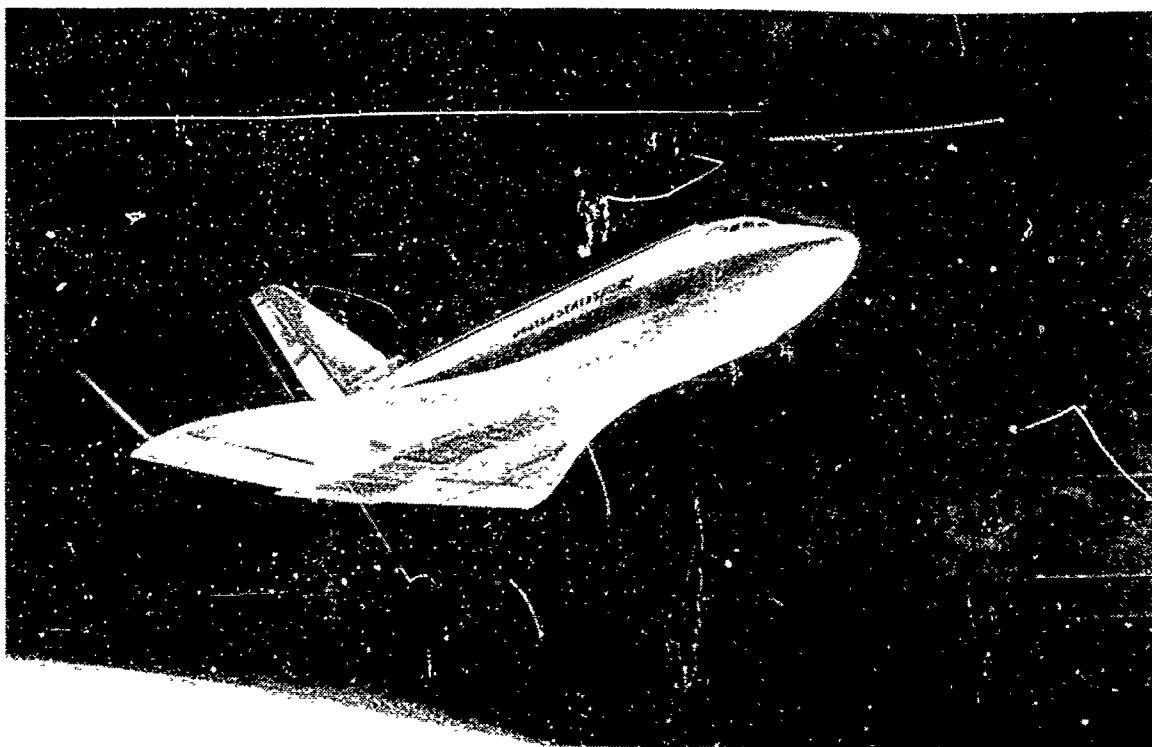


FIGURE 6 - AERODYNAMIC HEATING DURING RE-ENTRY

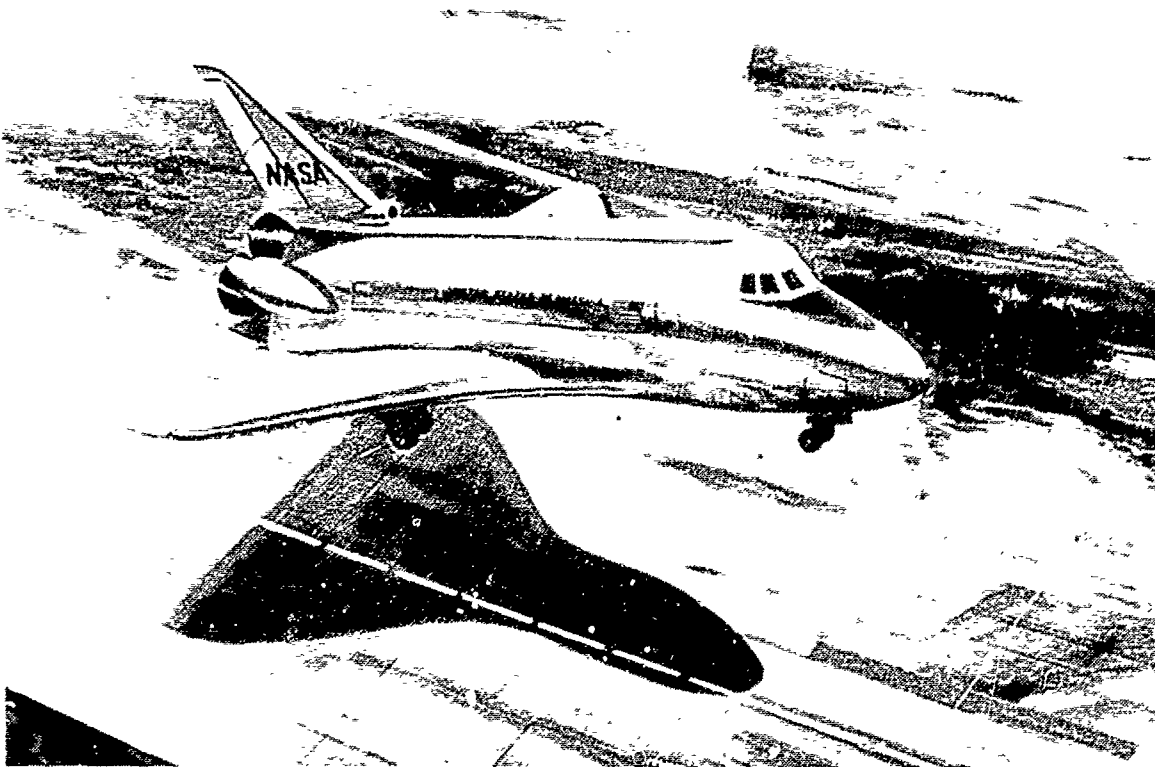


FIGURE 7 - LANDING AT THE KENNEDY SPACE CENTER

- o DUAL FUNCTION EQUIPMENT COMPLEMENT
- o AUTOMATIC SYSTEM CHECKOUT
- o FAIL-SAFE REDUNDANCY
- o DATA BUS EQUIPMENT CONTROL

FIGURE 8 - AVIONICS SYSTEM DESIGN CHARACTERISTICS

TOTAL HYBRID MICROCIRCUITS PER VEHICLE	14,746
(OFF-THE-SHELF INLINE SYSTEM HYBRIDS)	(4,007)
HYBRID MICROCIRCUIT CONFIGURATION TYPES	215
HYBRID MICROCIRCUIT VENDORS	29
SUBSYSTEM MANUFACTURERS USING HYBRID MICROCIRCUITS	30
COST RANGE	\$50 - \$1,000

FIGURE 9 - HYBRID MICROCIRCUIT APPLICATION SUMMARY

FIGURE 10 - HYBRID MICROCUT VENDOR, CONFIGURATION TYPE AND
QUANTITY COMPARISON FOR EACH SHIPSET

NATIONAL SEMI. CORP., SANTA CLARA, CA	8/131
SILICONIX, SANTA CLARA, CA	8/666
TELEDYNE MICROELECTRONICS, LOS ANGELES, CA	13/3135
Q-TECH, LOS ANGELES, CA	10/40
STERER, LOS ANGELES, CA	4/8
LEACH RELAYS, LOS ANGELES, CA	*0/400
AUTONETICS, ANAHEIM, CA	0/1200
TELEDYNE RELAYS, HAWTHORNE, CA	0/24
CRANE/HYDROAIRE, BURBANK, CA	6/56
HALEX, TORRANCE, CA	1/2
BECKMAN INSTRUMENTS, FULLERTON, CA	6/206
HUGHES, NEWPORT BEACH, CA	1/6
SPERRY/FSD, PHOENIX, AZ	85/3000
COLLINS RADIO CORP., DALLAS, TX	12/1322
MICROPAC, GARLAND, TX	2/4
TEXAS INSTRUMENTS, DALLAS, TX	2/3035
ELECTRONIC RESISTOR CORP., MISSION, KS	2/7
WESTINGHOUSE, LIMA OH	1/200
MAGNAVOX, FORT WAYNE, IN	0/18
LEAR-SIEGLER, GRAND RAPIDS, MI	14/74
VECTOR, NEWTON, PA	3/376
GENERAL ELECTRIC, UTICA, NY	3/12
MICRONETWORKS, WORCESTER, MA	2/4
FILM MICROELEC., BURLINGTON, MA	1/78
RAYTHEON, QUINCY, MA	3/12
GENERAL INSTRUMENTS, HICKSVILLE (L.I.), NY	13/183
CTI, FARMINGDALE (L.I.), NY	3/263
SINGER/KEARFOTT, LITTLE FALLS, NJ	5/5
WESTINGHOUSE, BALTIMORE, MD	1/200
IBM/HUNTSVILLE, HUNTSVILLE, AL	1/70
TRAK MICROWAVE, TAMPA, FL	2/5
MOTOROLA/GED, PHOENIX, AZ	1/0
UNITRODE CORP., WATERTOWN, MA	2/4
*To Be Determined	

TECHNOLOGY DISCIPLINES	WIRE BONDING
THICK FILMS	THERMOCOMPRESSION
THIN FILMS	ULTRASONIC
	EPOXY
METALLIZATION	PACKAGES
SINGLE	FLATPACK
MULTIPLE	ROUND CAN
	DUAL INLINE
SUBSTRATES	SPECIAL TYPES
SINGLE	
MULTIPLE	SEALING TECHNIQUE
	WELDING
DIE ATTACH	EUTECTIC
EPOXY	SOLDER
EUTECTIC	
SOLDER (LIDS)	COATING
	PARYLENE
	SILICONE

FIGURE 11 - TECHNOLOGY VARIATIONS IN SHUTTLE HYBRID MICROCIRCUITS

SIZE	1.25" x 1.25"
WEIGHT	12 GRAMS
PACKAGE	FLATPACK
SEAL TECHNIQUE	EUTECTIC
ACTIVE COMPONENTS (CHIP)	49
TRANSISTORS (25)	
DIODES (18)	
INTEGRATED CIRCUITS (6)	
PASSIVE COMPONENTS (CHIP)	39
CAPACITORS	
RESISTORS	
PASSIVE COMPONENTS (FILM)	15
THIN-FILM RESISTORS (15)	
BOND WIRES	384

FIGURE 12 - CHARACTERISTICS OF THE MOST COMPLEX SHUTTLE HYBRID MICROCIRCUIT

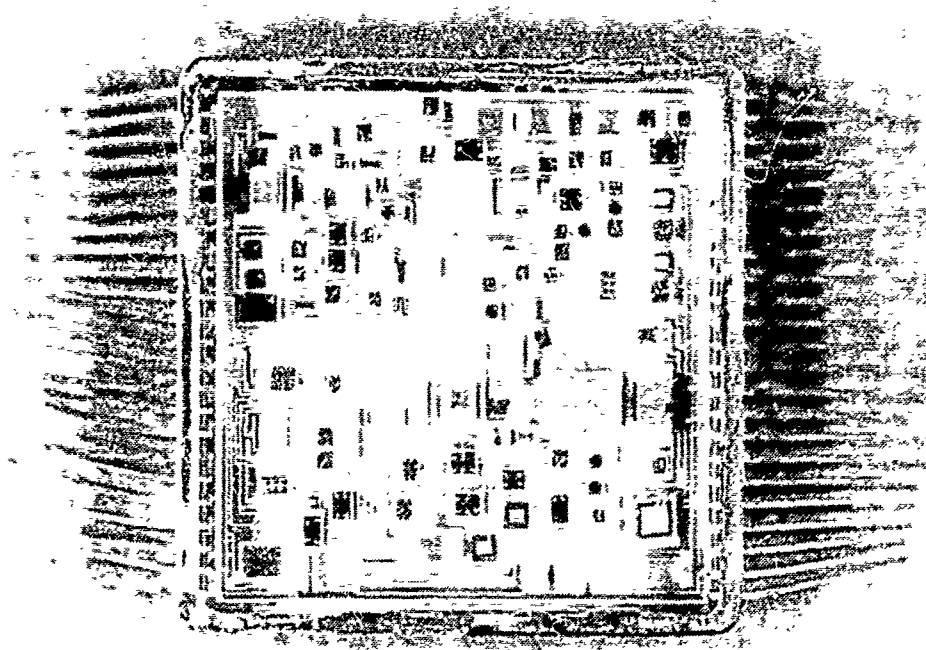


FIGURE 13 - COMPLEX THIN-FILM HYBRID MICROCIRCUIT

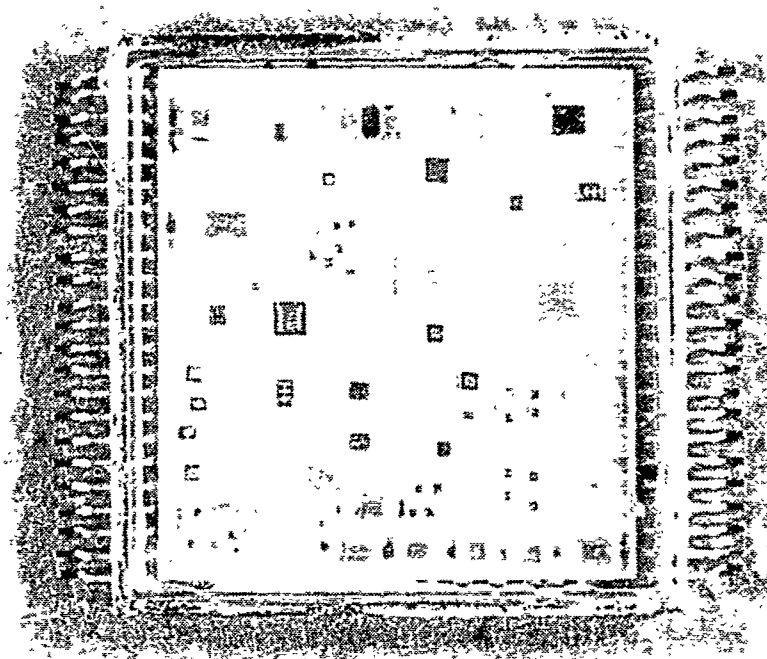


FIGURE 14 - COMPLEX THICK-FILM HYBRID MICROCIRCUIT

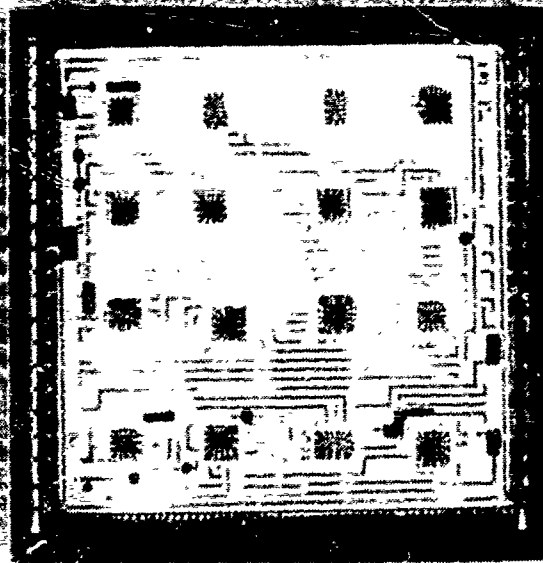


FIGURE 15 - TYPICAL 1"x1" THICK-FILM HYBRID MICROCIRCUIT

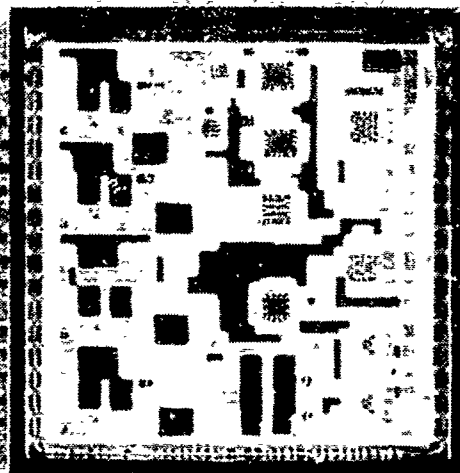


FIGURE 16 - INSULATING GLASS ON THICK-FILM HYBRID MICROCIRCUIT

- o CHARACTERISTIC OF THE TECHNOLOGY
- o ACTIVE DEVICE FAILURE IS CHIEF CAUSE
- o COST BREAKOVER POINT IS ABOUT \$100
- o FIELD FAILURE REWORK IS A NEW REQUIREMENT
- o ADHESIVE DIE ATTACH AIDS REWORK
- o WELDED PACKAGE LID FACILITATES REMOVAL AND REPLACEMENT
- o PARTICLE IMPACT NOISE DETECTION TESTING

FIGURE 17 - HYBRID MICROCIRCUIT REWORK EXPERIENCE

HYBRID MICROCIRCUIT FAILURE MODES

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ABSTRACT

This paper describes the results of two hybrid microcircuit surveys: one of in-process rework and the other of field failure analyses. The microcircuits were typical of those found in military applications. There was a definite similarity in the causes of in-process rework and causes of low power microcircuit field failures. The major causes of problems both during fabrication and operation were active devices and wire bonds.

INTRODUCTION

Hybrid microcircuits have been utilized extensively by the military services in recent years because of weight, size, performance, system cost, and reliability advantages. As electronic systems increase in complexity there are subsequent pressures to increase the complexity of hybrid microcircuits which make up these systems. One inevitable consequence of higher complexity is higher cost and lower reliability. Both the hybrid microcircuit manufacturers and their military customers have a strong motivation to counter this reliability and cost impact.

In order to improve the reliability of microcircuits, we need to first understand why they fail. This information is not, however, readily available or easily acquired. The causes of failures are of course strongly related to the microcircuit design, construction, performance specifications, and application. Failure data from a wide population of microcircuits, even if available, would be of limited value; such data needs to be further reduced to group microcircuits of a similar nature. One source of valuable information is the Failure Analysis Report (FAR) which is the result of a well defined procedure to determine the cause of failure as well as the appropriate corrective action for individual microcircuit failures. While FAR s have a number of shortcomings, they are invaluable and were used as the major source of microcircuit failure data in this study.

The successful fabrication of complex hybrid microcircuits requires a certain amount of in-process rework. The degree and nature of such rework are of vital concern to the microcircuit manufacturer since they directly influence his costs. An understanding of this rework is also useful with respect to reliability since there is no doubt a relationship between the two. This relationship may in fact be twofold in nature.

First, in-process rework, especially that required due to component failure during screening tests, may reflect inherent reliability problems, just as field failures do. Secondly, the process of rework may itself introduce additional reliability problems.

This paper describes the results of a study conducted for the U.S. Army Electronics Command in which analyses of both the causes of hybrid microcircuits in-process rework and the causes of failure in delivered hybrid microcircuits were performed. It is part of a broader program conducted under contract DAAB07-75-C-1311 aimed at the development of functional controls and tests to be used to detect and avoid failure modes during the hybrid microcircuit fabrication.

IN-PROCESS REWORK

The Quality Control History Records of over five hundred low power hybrid microcircuits (fabricated by the process shown in Figure 1) were analyzed. The microcircuits were relatively large in size, with areas from 6 to 13 cm². They were also relatively complex, containing from 8 to 12 components/cm² (a component is defined here as either an active or passive device).

The in-process rework causes and the percentages attributed to each are shown in Figure 2. Active device causes accounted for the majority (60 percent) of rework. Wire, resistor, and passive discrete causes together accounted for 37 percent of the rework.

The cause categories identified in Figure 2 imply that failures in these categories were the cause of rework. Actually, the categories encompass more than failed components and must be regarded with this in mind. Workmanship errors (incorrect component, miswired, damaged, etc.), for example, required a small portion of the rework in both the active device and wire categories. The active device category is also greatly influenced by the diagnostic skill of technicians during troubleshooting. Even after taking these factors into account, however, there is little doubt that faulty active devices and loose wire bonds were the major causes of in-process rework on this group of hybrid microcircuits.

HYBRID MICROCIRCUIT FAILURE CAUSES

A review of 396 Hughes Aircraft Company Failure Analysis Reports (FAR s) was performed. The FAR s were accumulated over the past 5 years by the Failure Analysis Laboratories at various Hughes facilities. The FAR s dealt primarily with military, medium-complexity microcircuits purchased from 21 commercial suppliers as well as with medium- to high-complexity microcircuits manufactured at Hughes Aircraft Company. In general, all microcircuits had been screened to MIL STD 883, method 5004, class B, prior to delivery. Each FAR represented an attempt to analyze a reported field failure (or failure after delivery of the microcircuit). Not all failures were verified and others were considered not to have identified the true cause of the failure. Only "primary" failures were evaluated in-depth in this task. "Primary" failures are explained in the following discussion.

When a microcircuit is submitted for failure analysis it undergoes visual inspection, electrical testing, and de-lidding. Each reported failure is assigned to one of the following categories:

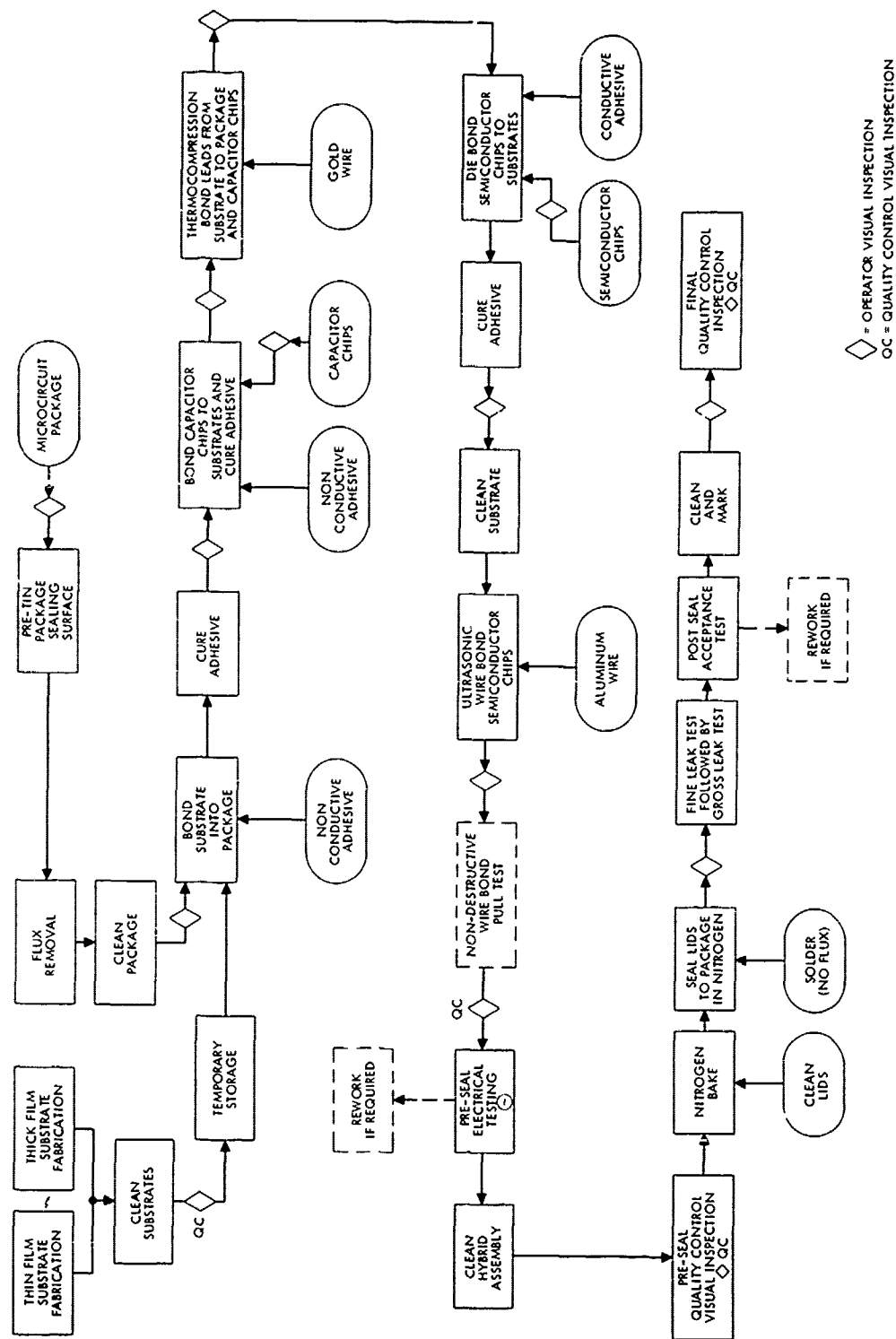


Figure 1. Process flow for typical hybrid microcircuit.

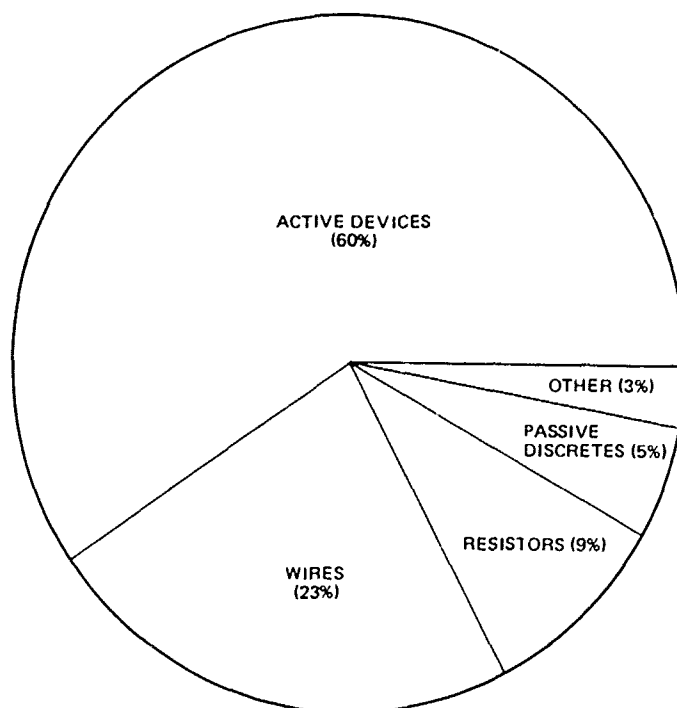


Figure 2. Distribution of low power microcircuit in-process rework causes.

- Unconfirmed – The failure is unconfirmed if testing of the microcircuit (by the failure analysis group) to the procurement specification results in acceptable performance. Such a finding might result in immediate return of the microcircuit for use or in further analysis, depending on the nature of the reported failure and other factors.
- Secondary Failures – The failure is secondary if testing of the microcircuit confirms it to be inoperative or otherwise out-of-specification, but the cause is external to the microcircuit itself. An example is a case in which the microcircuit is exposed to excessive voltage or temperature which render it inoperative.
- Primary Failures – The failure is primary if the microcircuit operates out of specification because of factors in its own construction. The objective of the FAR is to determine the cause of the failure and make recommendations to prevent similar failures in like microcircuits.

The FAR s were first divided into the three categories described, then the primary failure category was broken into two subcategories (see Figure 3). The primary-failure subcategories were created when it was found that there were characteristic differences in causes of failures between microcircuit types (for example, high-power microcircuits exhibited many failures due to thermal-path problems).

It is evident from this division that all reported failures were either not failures at all, or were not related to the reliability of the microcircuits; only 56.3 percent of reported failures were determined to be primary failures.

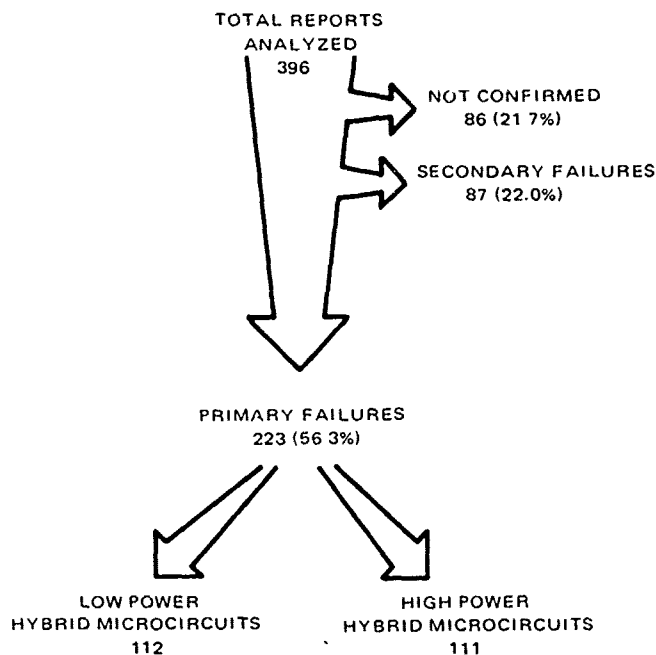


Figure 3. Size of Failure Analysis Report categories

The high- and low-power microcircuit subgroups were further divided into failure-cause categories. The category names do not necessarily describe the mechanism or causes of the failure. For example, the active device failure category might include cases of dice fractures. Such fractures may have resulted from dice manufacturing, microcircuit assembly, or improper heat sinking of the active device. In this case, an active device failure cause does not necessarily represent an indictment of the active device. This should be kept in mind during the discussion of further breakdowns in the subgroups

LOW-POWER HYBRID MICROCIRCUITS

The failure-cause category distribution for this group is shown in Figure 4. The following is a brief discussion of each category:

Active-Device Failures

This is the largest single failure-cause category. Most such failures were attributable to the active device itself, rather than to damage occurring during assembly into microcircuits. A prominent mechanism of failure cited was "oxide defects". Another mechanism listed was "channeling", which might have been caused by contamination of the semiconductor surface. Metallization defects, such as smears, opens, and shorts were also listed. A cracked chip is shown in Figure 5.

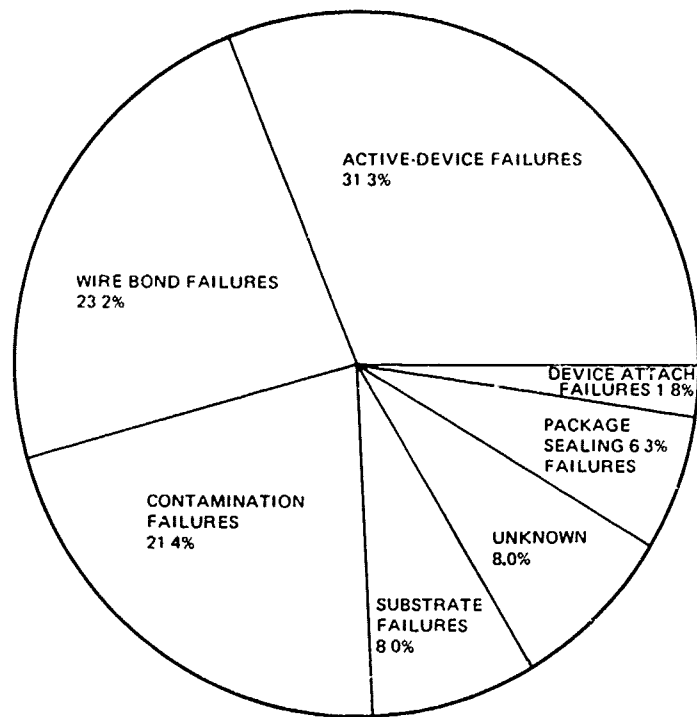


Figure 4. Distribution of low-power hybrid microcircuit failure-cause categories.

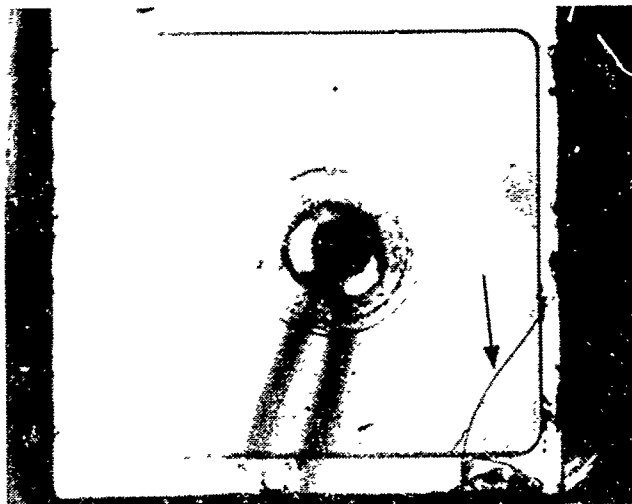


Figure 5. Crack in diode chip (157X).

Wire Bond Failures

This category is relatively unambiguous; the wire bonds were loose. Most loose bonds occurred between the wire and active-device metallization, mainly in thermocompression-bonded gold wires (ball end). Most ultrasonically bonded aluminum-wire bonds failed because of "over-bonding," or neckdown. Figure 6 shows a typical loose ball bond.

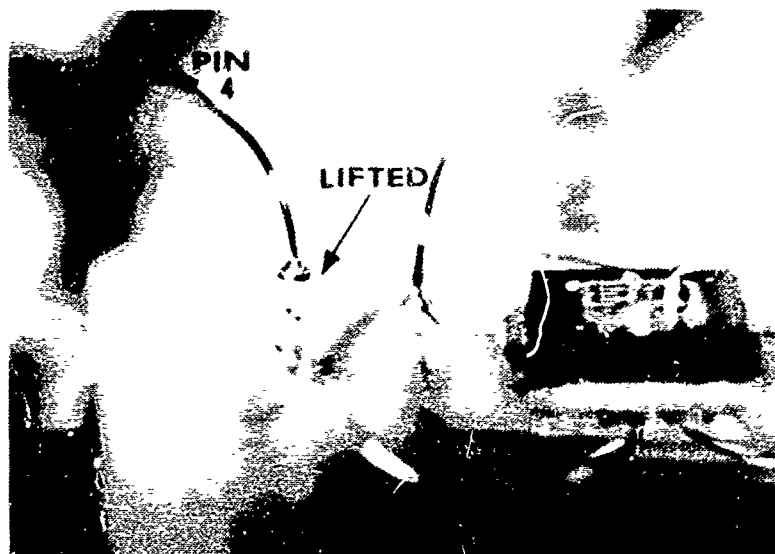


Figure 6. Gold ball bond failure (to thin-film metallized substrate) 60X.

Contamination Failures

This category comprises chemical contaminants (25 percent) and particulate contaminants (75 percent). The chemical contaminant was mainly chlorine, which attacked aluminum metallization. One case of moisture contamination and subsequent electrochemical "disappearing" of nichrome resistors was reported. Many of the cases of chemical contamination were reported to result from packages with faulty hermetic seals. (It is likely, but not certain, that damage occurred because of the combined effect of chemical residue and moisture which entered through a leaky package seal.)

Particulate contamination is a dilemma to the analyst. When the cause of failure is not obvious (a loose wire bond, for example), the analyst looks closer and usually finds signs of contamination. The contamination might be large metallic particles, or small nonmetallic particles. The analyst then tries to relate the exhibited failure to the observed particle. A common concluding remark on the FAR s is: "While the particle is not likely to have caused the observed failure, it is not allowed by specification, therefore this is a primary failure."

In the FAR data reduction, only cases of failures which could have been caused by particles were counted as particulate-contaminant failures. The others were put into the "unknown" category. Even so, contaminants were a major cause of microcircuit failure. Loose gold and aluminum wires accounted for a large percentage of the failures. Solder balls were also a common contaminant (see Figure 7); these were generated either during package sealing or substrate attachment to pins.

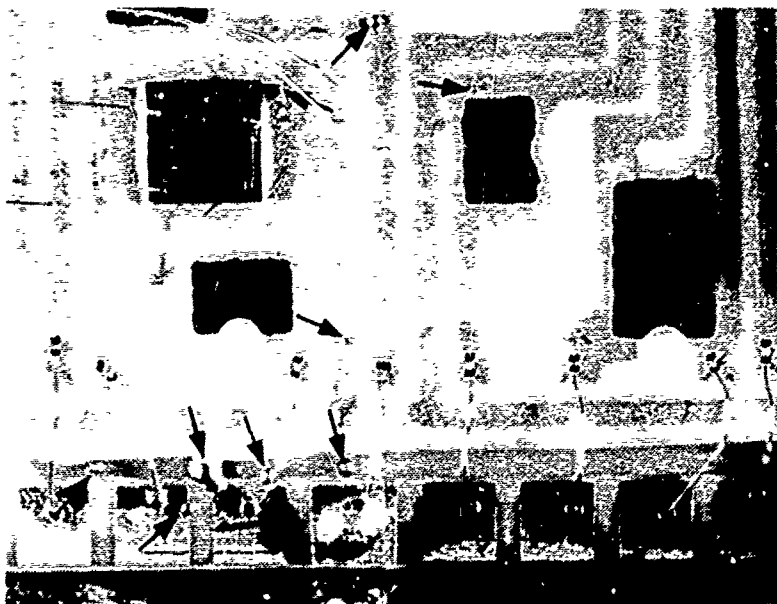


Figure 7. Contamination by solder balls (10X).

Substrate Failures

This category comprises substrate-related defects, primarily open solder joints caused by leaching of thick-film metallization. A few substrate cracks and one thin-film tantalum resistor failure were recorded. No cases of thick-film resistor drift were found.

Package Sealing Failures

The major problem in this category was package pins shorting during solder sealing.

Device Attachment Failures

No active-device attachment problems were reported. However, chip capacitors were reported that had loosened because of faulty solder or conductive adhesive attachment.

HIGH-POWER HYBRID MICROCIRCUITS

The failure-cause category distribution for this group is shown in Figure 8. The following is a brief discussion of each category:

Solder Joint Failures

Most of the power hybrids utilize a thick-film substrate soldered to pins of a TO-type package. Most failures in this category were caused by solder leaching of the thick-film metallization in the region of the pins, causing metallization opens.

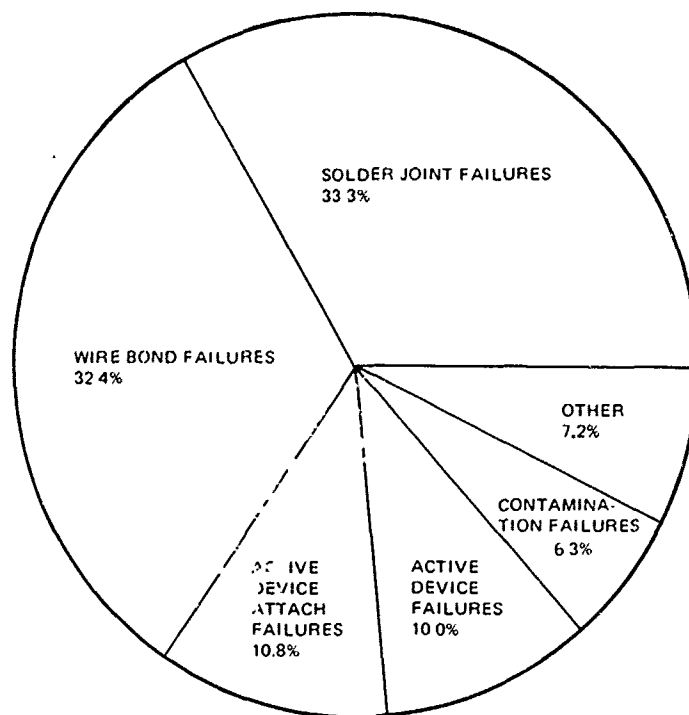


Figure 8. High-power hybrid microcircuit failure-cause categories.

Wire Bond Failures

Power hybrids usually use one or more power transistors, interconnected by heavy [1.5-mil (38 μm) to 5-mil (127 μm)] aluminum wire, the bonding of which is often difficult and imprecise. Also, smaller diameter wires on power hybrids have higher failure rates because of the higher temperatures associated with these devices. Figure 9 shows a typical bond problem caused by overbonding and fatigue.

Active-Device Attach Failures

This category consisted entirely of active devices that were not attached adequately. The devices were soldered to the package or substrate with or without a heat spreader. The major cause of problems was improper wetting of surfaces. Voids (air pockets) in the thermal path were very detrimental to the performance and reliability of the devices. Figure 10 shows a power-pill assembly (with copper heat spreader) that is loose from the package bottom. Figure 11 shows a large number of voids in the solder joint that caused excessive temperature rise and failure of the power transistor.

Active-Device Failures

Most of the active-devices that failed were low-power chips. Prominent causes were leaky diodes, fractured dice, and emitter-to-collector shorts.

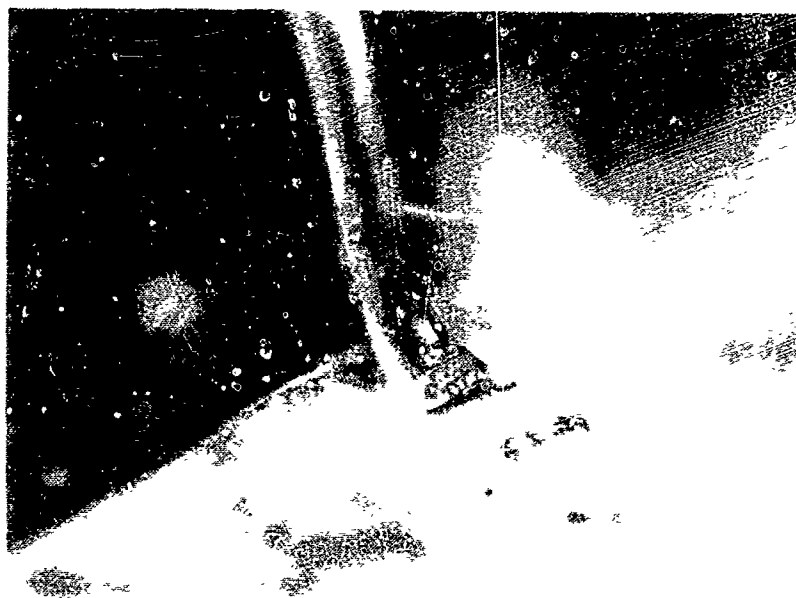


Figure 9. Partial fracture at heel of 5-mil (127 μ m) aluminum wire bond (40X).

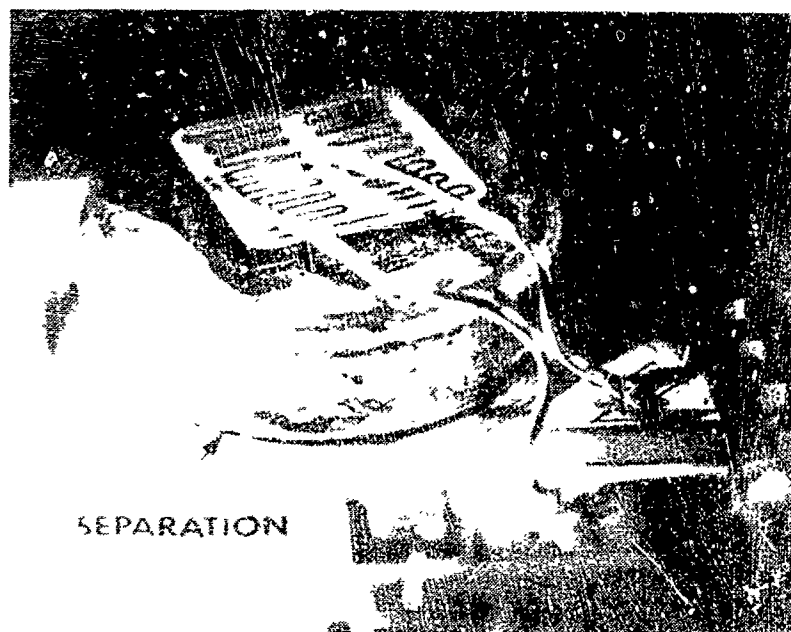


Figure 10. Power transistor mount lifted (8X).



Figure 11. View of large void area in solder interface between power transistor mount and package bottom (8X).

Contamination

This category applies more to low-power hybrids than high-power hybrids for the following reasons:

- (1) High-power hybrids tend to be less complex and therefore less likely to contain contaminants.
- (2) Power hybrids do not contain highly complex IC devices that are readily damaged by particle shorting.

DISCUSSION

Active devices were clearly identified in this analysis as the major cause of both in-process rework and subsequent field failure. This may come as a surprise to many who are aware of the high reliability record of individually packaged active devices. Individually packaged active devices can, of course, be much more thoroughly tested and screened than their chip counterparts which are used in hybrid microcircuits. The inability to fully test (AC, DC, full temperature range) active devices in chip form is probably the major problem, reliability- and cost-wise, that the manufacturer of military hybrid microcircuits faces.

"Flying wires" of gold or aluminum still predominate as the most widespread method of interconnection in hybrid microcircuits. That wire bonds are a major cause of hybrid microcircuit rework and failure is not surprising considering the large number of interconnecting wires in a typical microcircuit and the sensitive methods of bonding. Ultrasonic and thermo-compression bonding are quite dependent, for example, on the nature of the metallization, requiring different machine parameters for thick film, thin film, or electroplated metallization. The use of non-destructive pull testing of flying leads is thought to be the most effective (although expensive)

insurance against subsequent wire bond failures. The renewed activity in alternate methods of active device interconnection (flip chips, beam leads, tape carriers) appears fueled primarily by economic factors. Little is known at this time about the reliability of these competing interconnection techniques.

Particulate contamination is becoming a more prominent cause of failures of hybrid microcircuits. There are two primary reasons for this. First, the complexity of microcircuits increases with each new generation and the opportunity for contamination expands with increased processing. Second, the more complex microcircuits, with higher density of interconnections, result in a greater likelihood of damage being incurred by entrapped particles. Yet another factor which, strictly speaking, does not affect failure rates but may be cause for rejection, is the improvement in methods of detection of entrapped particles. The acoustical particle detection technique (PIN) is fast becoming an invaluable tool for both in-process control as well as a final acceptance test. The in-process use of the PIN test has been found very effective in providing feedback information at the first signs of particulate contamination problems.

CONCLUSIONS

A compilation and analysis of in-process rework and field failure records of complex hybrid microcircuits has identified active devices and wire bonds as the major problem areas for low power hybrid microcircuits. The distribution of failure causes was strongly related to the nature of the microcircuit as shown by the predominance of solder joint failures in power microcircuits which use solder joints for thermal, mechanical, and electrical interconnection.

This study highlights a number of serious problems in the fabrication of reliable hybrid microcircuits, including pretesting or conditioning of active device chips, control over wire bonding, and detection and prevention of particulate contamination.

THE HYBRID MICROELECTRONICS PROCESS AND QUALITY CONTROL GUIDE

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INTRODUCTION

In June of 1975, Honeywell was awarded a contract* by the U.S. Army Electronics Command, Ft. Monmouth, N.J. to study Hybrid Microelectronics Processing Standards. The goal of this study was to evaluate critical processes, components, and materials used in hybrid fabrication with respect to qualification procedures, process controls, and post-assembly screens. During the course of this investigation, the feasibility of establishing tighter process controls in an attempt to eliminate several costly screens (e.g. burn-in, temperature cycle, etc.) has been studied. The overall objective was to reduce the cost of manufacturing hybrids for military applications while at the same time improving their quality and reliability. The end product of this investigation was a book in loose leaf form entitled "The Hybrid Microelectronics Process and Quality Control Guide".

GENERAL INFORMATION

Definition

The Guide may be defined as a book which summarizes information on all areas of currently used hybrid manufacturing processes, controls, materials, components, and screens. Information is specific, easily found, and succinctly presented.

Purpose

The following objectives were identified for the Guide:

- a. The establishment of process and quality control information so that these controls may be established in lieu of certain post assembly screens. This is one of the key objectives and the Guide is organized to facilitate accomplishment of this goal.
- b. The book may be used to aid the military procurement agencies and technical personnel in evaluating prospective vendors. Because of the ordered manner in which qualification, process control, quality control, etc. information is presented,

*DAAB-07-75-C-1367

each page in the Guide may serve as a checklist to review existing processes.

- c. The Guide may also be used by hybrid vendors themselves in evaluating their own processes. For the same reasons, described above, it may serve as a checklist and remind them of areas possibly left uncontrolled or with inadequate control.
- d. A fourth possible use for the book may be to aid newly established manufacturers of hybrid devices in establishing proper controls and identifying all areas of concern.
- e. Finally, the Guide will serve as a book of general information and reference because of the extensive use of notes and references to military and federal specifications, and literature.

Sources of Information

To compile the large amount of information contained in the Guide, the writers drew from a number of different sources of information.

The following three basic sources of information were used to obtain the presented data:

- a. Hardware Tests Performed By Honeywell. At the beginning of the contract effort the Honeywell team identified certain areas where they felt significant contribution could be made through performing in-house tests. The areas of testing were selected on the basis of Honeywell's significant prior work and included wire bonding, epoxy chip attach and package sealing.
- b. Hybrid Vendor Survey. Although Honeywell's hybrid capability is diversified and includes many different disciplines with in-depth experience in all areas, it was felt that in order for the book to be representative of the industry, inputs from sources other than Honeywell were required. For this reason an exhaustive survey of other hybrid vendors was planned. This survey, which was conducted by the authors in December 1975 covered 14 of the major hybrid houses and posed 134 questions on nine topics. The questions pertained to currently used processes as well as established process controls and screens. By no means were all existing vendors surveyed; nevertheless, the survey provided a significant input to the guide.
- c. Other Reports and Literature. Much information for the guide has been gleaned from other papers on related subjects and especially from reports from other ECOM contracts. The latter represents data from interim and final reports on study contracts performed by other vendors for ECOM. All these

reports and literature inputs are referenced in the appropriate places in the Guide.

Controls in the Manufacturing Cycle

Process and quality controls as well as qualification tests and screens may be used during different phases of the manufacturing cycle. Figure 1 shows three distinct phases for use of the information supplied in the Guide.

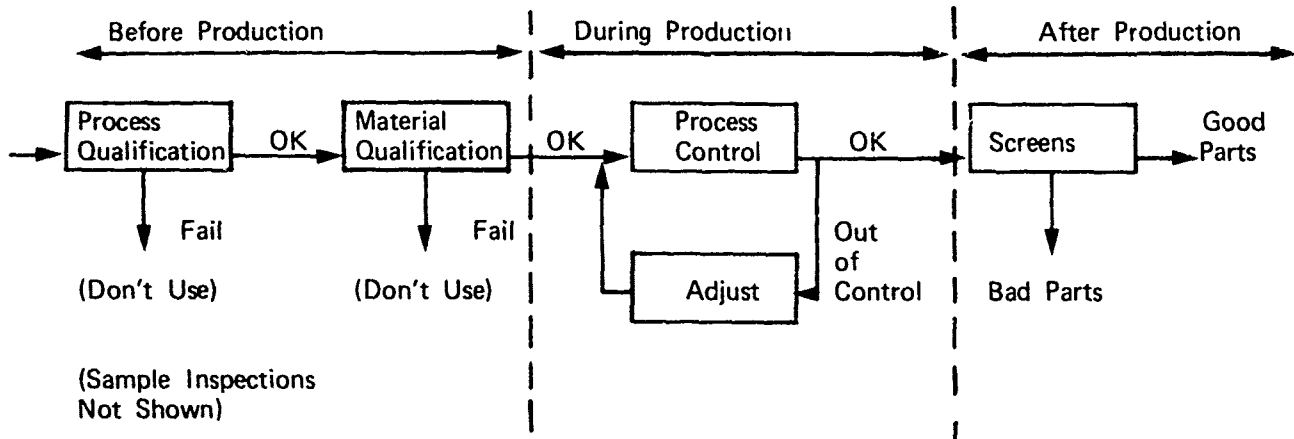


FIGURE 1. APPLICATION SEQUENCE OF "CONTROL" INFORMATION

Let us consider, for example, a chip attach process for which a new eutectic material has been submitted for use. Prior to committing this material to an existing manufacturing line, one must assure that it will, in fact, perform the die attach function adequately and with acceptable yields. A pilot run must be made and the resulting hardware thoroughly tested. This is the Process Qualification activity. Obviously, if the new material does not meet specifications, it will not be used for production. If, on the other hand, the material is accepted and purchased for regular use, then each incoming lot must somehow be assessed for content, uniformity, melting point, etc. These parameters must be reasonably close to the original lot parameters. This quality assessment of each new lot is the Material Qualification. Both of the above qualifications take place prior to the actual production sequence.

During fabrication a number of tests should be made periodically under the category of Process Controls. In the case of our chip attach example, such tests may consist of a simple visual inspection or, more elaborately, a chip adherence or shear test. The tests are normally performed on small samples randomly selected immediately upon completion of the process. If the device fails the test, one knows that it is not the material which is at fault because it was qualified earlier. Some other parameter (e.g. substrate temperature) may be incorrect and may require adjustment.

Finally, because of random causes, there may still be devices fabricated whose quality is unacceptable. These must be removed from the lots of good devices. This removal process is done by screening, which may consist of a number of tests such as visual inspection, electrical/environmental testing, etc. applied in sequence. Screening is by definition performed on 100 percent of the produced parts and takes place after the manufacturing process. Not mentioned in this sequence are periodic sample inspections which take place, usually as QC audits.

It should be noted that many individual tests which are applied during each of these basic qualification, control, and screening operations may be identical. For example, a chip adherence test may be performed as part of (1) the initial process qualification, (2) during the material qualification and (3) possibly as a process control test. Because it is usually destructive it cannot be used as a screen. In the same way a temperature cycle test can be used for (1) process qualification, (2) material qualification and (3) as a screen.

Cost Considerations

One objective of Honeywell's work was to consider the cost trade-off of process controls versus screens. Therefore, a brief review of the cost assessment is included here. Figure 2 identifies the areas where "control" costs are incurred. For comparison purposes, the process schematic is identical to that shown in Figure 1.

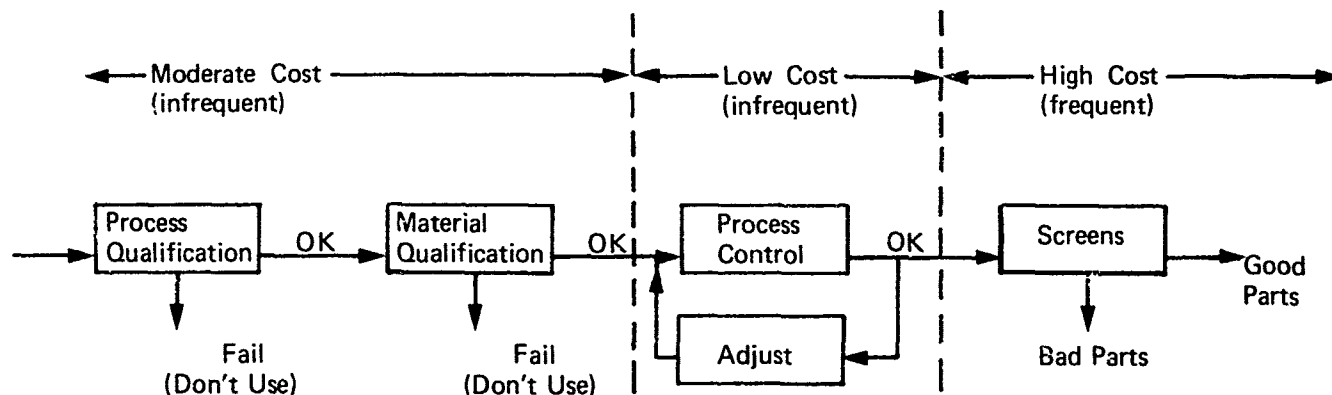


FIGURE 2. COST ASSESSMENT

In addition to the "control" cost, also the frequency of application must be taken into consideration in order to arrive at the total cost. Thus, one can see that the overall cost of the process and material qualification is only moderate, because although the cost of the tests are high, the frequency of application is low (once for every new process for the former and once

every shipment for the latter). The process control costs which occur during the production cycle are low as well because the cost of process adjustment is generally low and adjustment is relatively infrequent. High costs enter in after the assembly sequence is complete, as screening expenses are high (e.g. burn-in, centrifuge) and 100 percent of the completed devices must be tested in this manner. Thus it can be seen that an advantageous trade-off would occur if a screen could be eliminated by tightened controls during the manufacturing process. However, in order to apply adequate process controls, an intimate knowledge of the process is required. This knowledge is often lacking in hybrid processing which accounts for the relative ease with which imposition of screens is accepted.

ORGANIZATION OF THE GUIDE

The Guide has evolved as a loose leaf notebook with one page for each process or material*. It is believed that a one-page listing greatly facilitates indexing; it also ensures that adequate space is available for listing the most pertinent data, while allowing the same amount of space for each process without proliferation of data.

The Guide is divided into four major sections plus an appendix (see Figure 3), as follows: (1) Manufacturing Processes, (2) Parts/Components Inspection and Test, (3) Materials Inspection and Test, and (4) Rework. The appendix lists a number of the most commonly used qualification tests. Each of the four sections above is subdivided into individual process subsections as shown in Figure 3.

Process Sheet Contents, Organization and Use

As the major emphasis of the Guide is on processes, the process sheet is of great significance and much thought has been given to its organization. The sheet make-up is divided into three major areas: (1) identification, (2) areas of key interest, and (3) areas of peripheral interest (see Figure 4).

Identification includes the process described (e.g., wire bond), the materials used (for example, aluminum to gold) and the method employed (e.g., ultrasonic). This identifying information is placed across the top of the sheet for quick referral. In addition, a section number has been assigned to locate each page in the proper sequence within its chapter in the book. Figure 5 shows a sample page of Section 1.4.1 which clearly indicates the organization of the data on the sheet. (Note this is a draft only-- not the final document.)

The major portion of the sheet contains information on areas of key interest. These items include: (1) process qualification, (2) process controls and (3) screens. Figure 5 shows examples

*Several of the qualification tests excepted.

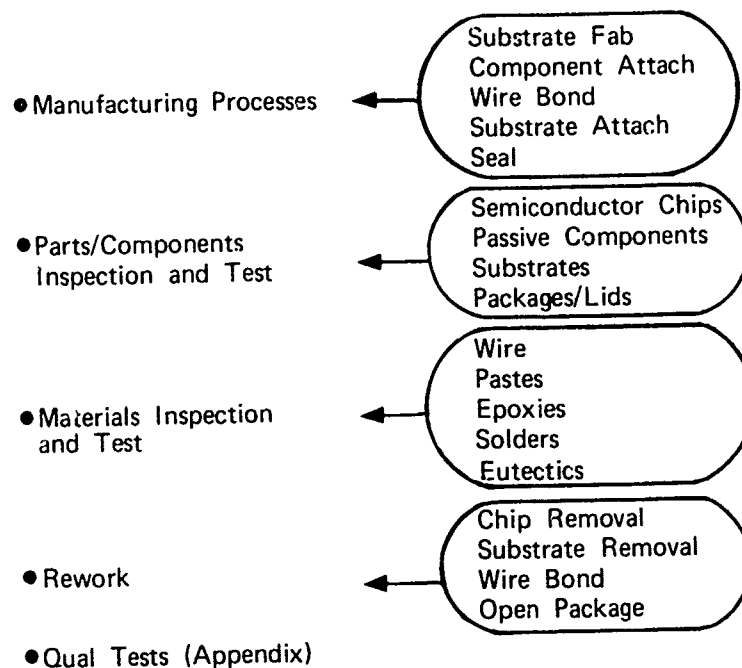


FIGURE 3. ORGANIZATION OF GUIDE

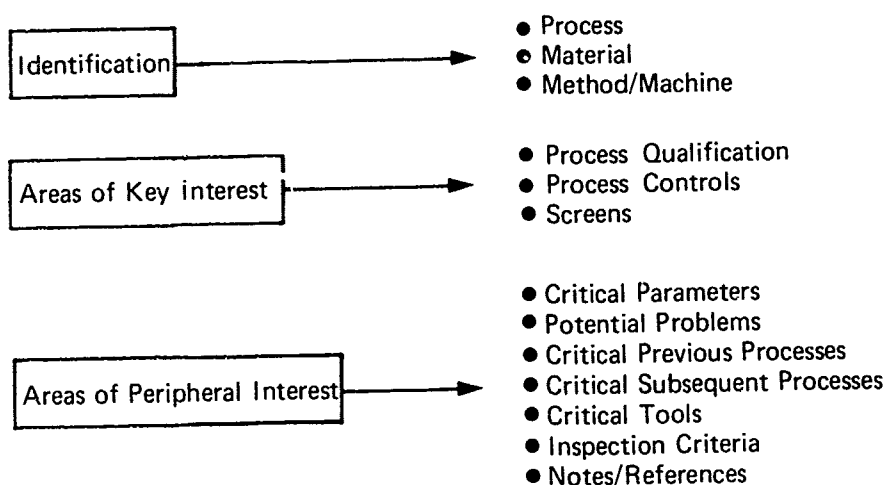


FIGURE 4. PROCESS SHEET ORGANIZATION

PROCESS: Wire Bond	MATERIAL(S) : Aluminum to Gold	METHOD/MACHINE : Ultrasonic
Process Qualification Tests: (1) Bondability (Appendix A, Test Nr. 3). (2) Visual Inspection.		
Process Controls: (1) Min. of 5 bond loops pulled to destruction once per shift. (2) Monitor energy, time, force. (3) Visually inspect sample immediately after bonding.		
Screens: (a) Mandatory: (1) Visual inspection. (b) Optional: (1) Non-destruct pull test. (2) Centrifuge. (3) Temp. cycle. (4) Mech. shock.		
Critical Parameters: (1) Pull Strength (2) Bond Resistance (after heatage) (3) Wire quality/consistency (4) Substrate/chip cleanliness	Potential Problems: (1) Non-Sticking during bonding. (2) Increased resistance after heatage (Burn-In). Will occur if substrate temp. reaches 160°C or higher. (3) Control of ultrasonic coupling.	
Critical Previous Processes: (1) Gold deposition or screen. (2) Cleaning of all surfaces. (3) Chip attach (flatness)	Critical Subsequent Processes: (1) Burn-in or other high temp. processing. (2) Handling. (3) Cleaning.	
Critical Tools: (1) Bonding Machine. (2) Bonding Tool. (3) Pull Tester. (4) Chuck or holding fixture.	Inspection Criteria: MIL-STD-883 Method 2017 Para. 3.1.6	
Notes/References: (1) "Changes in strength and resistance after burn-in of Aluminum Wire Bonds to Thick & Thin Film Gold." William R. Rodrigues de Miranda and R. G. Oswald - ISHM 1974. (2) "Changes in strength and resistance of Aluminum to Gold Ultrasonic Bonds after Temperature, Electrical and Environmental Stress." R. G. Oswald, W. R. Rodrigues de Miranda, C. W. White - ISHM 1975.		

FIGURE 5. SAMPLE OF PROCESS SHEET

of such information for the above listed wire bonding process. Note that screens are divided into mandatory and optional screens. This was done in response to the desire to place greater emphasis on process control than on post assembly screens. The mandatory screens are recommended regardless of which process controls are adapted. The optional screens may be eliminated, provided the above recommended process controls and qualification procedures are instituted.

The remainder of the sheet is designated to information of lesser importance, but nonetheless highly desirable. This information includes areas such as critical parameters, potential problems, critical previous processes, critical subsequent processes, critical tools and inspection criteria. It is this type of information that is often difficult to obtain in writing in organized fashion, and for which many manufacturers depend on experience and intuition of their team members. Finally, a space is provided for notes, and references where additional information and detail can be found.

Figure 6 depicts schematically how each of the items listed on the sheet provides an input in the manufacturing sequence. The square boxes represent production entries, while the rounded windows contain process sheet information details. Process control information, together with critical tools, critical parameters and potential problems deal directly with process "X". Before the start of process "X", qualification information deals with the qualification tests for this process and critical previous processes warn of potential problems which may have been created prior to, but may affect process "X". Upon completion of "X", inspection criteria list the basis for accept or reject and screens are recommended as optional or mandatory. Finally, subsequent processes are identified which may adversely affect the quality of the work just performed.

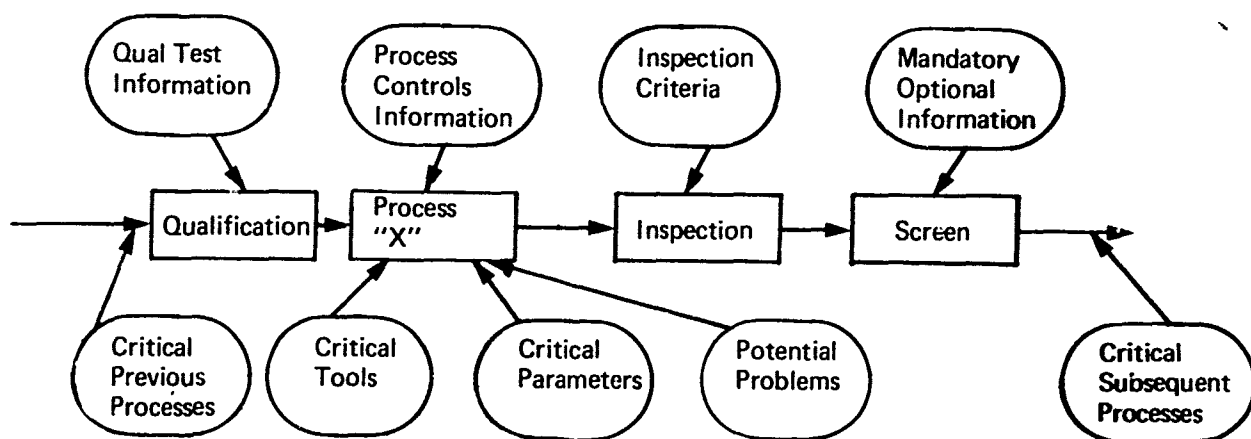


FIGURE 6. USE OF PROCESS INFORMATION

Components/Materials Sheet Contents, Organization, and Use

The second major sheet arrangement is used for both components and materials used in the hybrid manufacturing processes. Because of the similarities in areas of interest identical sheet organization is used for both. The information contained on the sheets may be divided into three main topics: (1) identification, (2) areas of key interest, and (3) additional information. (See Figure 7.)

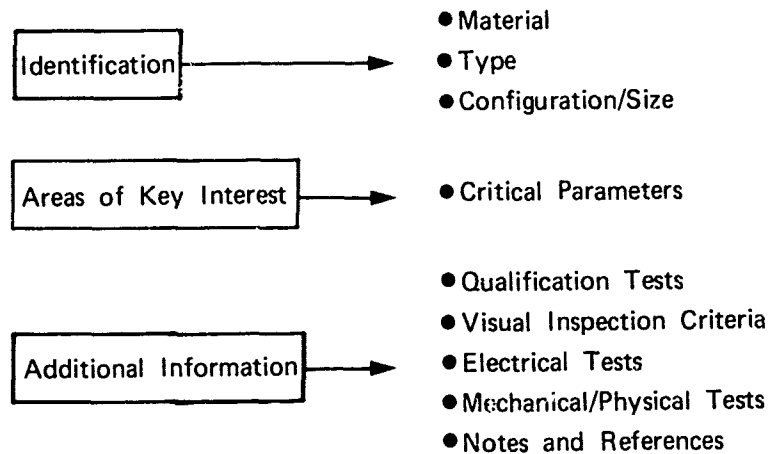


FIGURE 7. PARTS/COMPONENT/MATERIALS SHEET ORGANIZATION

Identification information includes the material or component nomenclature, the type of usage it sees, and configuration or size. There is some latitude in interpreting the use of the latter two headings, as long as adequate identification is retained. Again, for quick referral, the identification information is listed across the top of the page. Figure 8 shows a sample of a material sheet, Figure 9 shows a component sheet. Both figures are draft sheets and do not show the final printed version.

The areas of key interest include the critical parameters. In the case of the example shown on Figure 8, these parameters are specific mechanical and electrical properties. In the case of the materials (Figure 9) the critical parameters may include physical and chemical properties as well as age.

The category of additional information provides for a listing of such items as qualification tests, electrical test, mechanical or physical tests and inspection criteria. As with the previously discussed sheet format, a space for notes and references has also been provided.

MATERIAL: Thick Film Paste (Ink)	TYPE: Conductor	CONFIG./SIZE: A11
<u>Critical Parameters/Properties:</u> (1) Chemical/physical constituents (2) Viscosity (3) Age		
<u>Mechanical/Physical Tests</u> (1) Infrared analysis (2) Viscosity test (3) On fired sample: a) Thickness b) Porosity (SEM) c) Bondability d) Adhesion		<u>Electrical Tests:</u> (1) On fired sample: a) Conductivity
<u>Visual Inspection Criteria:</u> (1) Physical condition of container (must be sealed) (2) Review of records (lot number, ship date, expiration date, etc)		<u>Qualification Tests:</u> (1) Film Thickness - Optical Method (Appendix A, Test #1). or (optional): Film Thickness - Stylus Method (Appendix A, Test #2). (2) Bondability (Appendix A, Test Nr. 3). (3) Adhesion - Oiler Method (Appendix A, Test Nr. 4)..
Notes/Reference's 1) ECOM Report 75-1331-1.		

FIGURE 8. SAMPLE OF MATERIAL SHEET

COMPONENT:	TYPE:	CONFIG/SIZE:
Package	Kovar	16 Pin DIP
<u>Critical Parameters:</u> <ol style="list-style-type: none"> 1) Electrical Isolation 2) Thermal Resistance (Θ_{JA}) 3) Resistance to Corrosion 4) Mechanical Strength 5) Hermeticity *6) EMI/Tempest 		
<u>Qualification Tests</u> <ol style="list-style-type: none"> 1) Mechanical Shock Test 2) Thermal Shock Test 3) Thermal Cycle Test 4) Vibrational Test (variable freq.) 5) Lead to Ground Resistance 6) Hermeticity Test 7) Salt Atmosphere Test (Corrosion) 8) Lead Strength 		<u>Visual Inspection Criteria</u> MIL-STD-883A Method 2017
<u>Electrical Test</u> <ol style="list-style-type: none"> 1) Lead to Ground Resistance 2) Pin-Pin Isolation 		<u>Mechanical/Physical Test</u> <ol style="list-style-type: none"> 1) Mechanical Shock Test 2) Thermal Shock Test 3) Thermal Cycle Test 4) PIND Test
<u>Notes/References:</u> <ol style="list-style-type: none"> 1) M. Fogiel, Modern Microelectronics (Research and Education Association, N. Y. 1973). 2) ISHM-SPA-001 <p>*Depending on Application</p>		

FIGURE 9. SAMPLE OF COMPONENT SHEET

Figure 10 shows the sequence of use of information provided on the parts or material sheets. Referring to the centrally located component or material "X", qualification takes place prior to use and qualification test information is provided therefore. Critical parameters play a role in both qualification tests and visual inspections as well as being a dependent property of the part or material. Finally, electrical, physical and mechanical test information is used during such test, generally prior to use.

Rework Sheet Contents, Organization and Use

The sheets to describe the rework processes were kept basically the same as the process sheets, with minor modifications. The resemblance stems from the fact that the rework cycle may be considered an assembly process or a series of such processes. The rework sheet differs from the process only in the following ways:

1. The title/identification heading is simplified, listing only the process and the method.
2. The space for process qualification has been replaced by Process Description. This is a summary of the rework process described.
3. The spaces provided for critical previous and subsequent processes have been replaced by blocks to list Rework Limitations and Replacement Procedure.

Qualification Test Sheet Organization and Use

In order to provide some measure of standardization in the type of qualification testing deemed desirable for the diverse processes, an appendix has been provided with 13 different recommended qualification tests. These tests are suggested for use with certain processes and may consist of single tests or groups of different sub-tests to be performed in the listed sequence. The tests are described in considerable detail. The information is provided to aid the user in determining how to go about qualifying a material or process for use.

The qualification test sheet again has its information divided into three basic sections: (1) identification, (2) areas of key interest, and (3) test information. As with the previously described sheets, the identification lists nomenclature. However, in this case it lists also the applicability of the test (see Figure 11). Areas of key interest give basic information needed in order to conduct the test, such as objectives, parameters, conditions, sample size and test vehicle. Finally, the last category gives a brief summary plus a detailed description of the test, or alternately, it may refer to literature where a detailed description may be found.

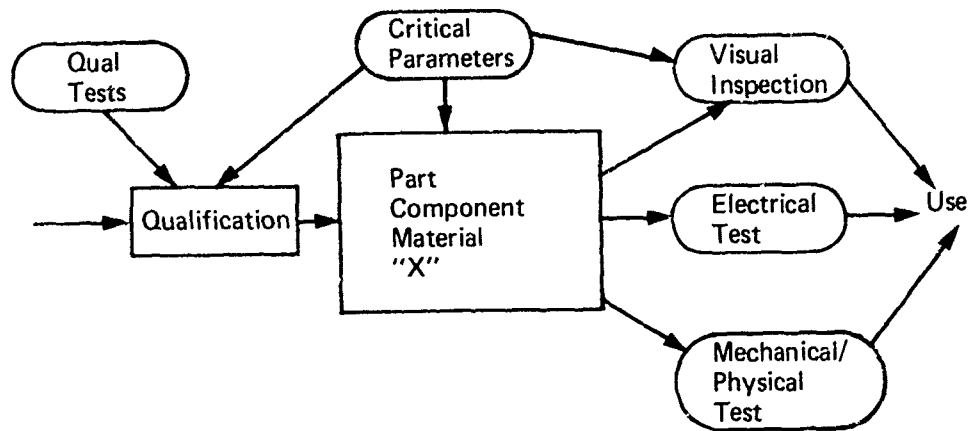


FIGURE 10. USE OF PART/COMPONENT/MATERIAL INFORMATION

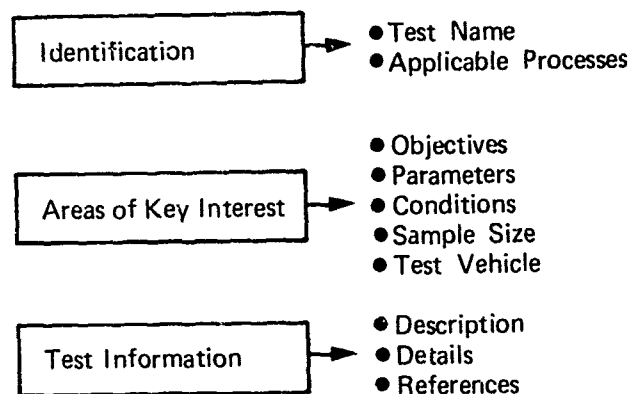


FIGURE 11. QUALIFICATION TEST SHEET ORGANIZATION

Figure 12 shows a sample of one of the qualification test sheets (draft copy). Note how the information is divided on the page. Each of the above mentioned areas is distinctly listed.

CONCLUSIONS AND RECOMMENDATIONS

The authors believe that in the Hybrid Microelectronics Process and Quality Control Guide a valuable tool is created for future use as intended and outlined in the introduction. Furthermore, an existing need has been met in a unique way, as no such guide book previously existed. It should be noted that the Guide is just that, a "guide", and not a specification. The information contained in it are recommendations only, even though such words as "mandatory" are used. In no case is it intended that the data listed be used as requirements to be imposed on a prospective vendor.

The authors recognize the limitations of the Guide. Undoubtedly, there are many processes which are "standard" at certain manufacturer's facilities which have not been mentioned, although an attempt at completeness has been made. Also, the information on the listed processes and materials may be improved and updated. Furthermore, although a survey was conducted, this book remains essentially a "one man" (one company) job, as opposed to certain military documents which were created by sizable committees of users and producers. For all the above reasons, the final version of the Guide will contain a tear-out comments sheet, which solicits user's inputs to ECOM and ensures a method whereby these comments can be evaluated and incorporated through periodic revisions.

TEST NAME: Film Thickness - Stylus Method		APPLICABLE PROCESSES: 1. Substrate Fabrication - Thick Film 2. Substrate Fabrication - Thin Film	
<u>Objectives:</u> 1. Assure consistency in application and firing of thick film pastes. (Alternate to optical method.) 2. Assure proper control of thin film sputtering of evaporative processes.			
<u>Parameters:</u> Thick Film Conductors (all) Thick Film Resistors Thin Film Conductors		<u>Thickness:</u> 8 microns 10 microns <u>Test Conditions:</u> Room Temp.	
<u>Sample Size:</u> 5 pices from qualification lot.		<u>Test Vehicle:</u> Sample production boards.	
<u>Test Description:</u> The Tally-surf or stylus method of measuring thickness does so by mechanically sensing the steps of the metal thickness elevation above the uncoated portions of the substrate.			
<u>Test Details:</u> 1. <u>Thick Film:</u> Run Tally-surf (or equivalent) stylus across several parallel conductor lines on the boards. Determine thickness from trace read-out. 2. <u>Thin Film:</u> Etch several parallel conductor lines on the boards. Then run Tally-surf (or equivalent) stylus across several of the lines and determine thickness from trace readout.			
<u>References:</u>			

FIGURE 12. SAMPLE OF QUALIFICATION SHEET

MATERIAL REQUIREMENTS AND PROCESS CONTROLS FOR
EPOXY ADHESIVES USED IN HYBRID MICROCIRCUITS

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ABSTRACT

The key adhesive material and process parameters considered to be most critical to hybrid microcircuit reliability have been defined, tests have been established for their measurement, and a guideline specification has been written. Experimental data were developed as a result of three studies sponsored by both Army/ECOM and NASA/MSFC. A review is given of the technical basis for the preparation of the specification with emphasis on bond strength retention under various military stress conditions, long-term electrical stability, thermal stability, and outgassing effects on devices.

INTRODUCTION

The use of electrically conductive and electrically insulative epoxy adhesives (both for commercial and military applications) is now a widespread practice among manufacturers of hybrid microcircuits. About five years ago when we started our studies, there was considerable confusion and a scarcity of data on the use of epoxy adhesives. This coupled with a proliferation of new and proprietary adhesives and the inherent complexity of epoxy polymer chemistry provided the thrust for the initiation of several studies. Three of these programs were conducted by Rockwell International, Autonetics Division during the past four years. Two programs were sponsored by NASA/MSFC and one by Army/ECOM. A fourth program, now in progress, is also being sponsored by Army/ECOM. The general objectives of these programs are given in Table 1. Our approach was first to define the adhesive material and process parameters that were considered to be most critical to device and microcircuit reliability, then to develop tests to measure these parameters, to establish minimum requirements, and finally to generate a guideline specification. The adhesive parameters considered to be most critical to hybrid microcircuit reliability are:

- Adhesion (bond strength)
- Electrical Stability
- Thermal Stability
- Outgassing and Effects on Devices
- Corrosivity
- Metal Migration

In this paper we shall summarize some of the work we have performed and the results obtained in the areas of bond strength, thermal stability, electrical stability, and outgassing effects on devices. Corrosion and metal migration

results have been reported in other papers (references 1, 2 and 3). These inherent material properties are extremely important for the initial qualification of an adhesive. It should be noted however that there are two aspects to adhesive reliability: initial selection and qualification based on inherent material properties and subsequent in-process tests and controls. The best adhesive from the standpoint of its chemical, physical and electrical properties may be completely unreliable if poor application procedures or inadequate process controls are used. Among some critical process parameters are:

- ° Adhesive Shelf Life/Pot Life
- ° Surface Cleanliness
- ° Wettability of Adhesive
- ° Application Method
- ° Thickness and Uniformity
- ° Cure Schedule (Time and Temperature)
- ° Cure Ambient
- ° Compatibility with Processing Solvents
- ° Sealing Conditions

TABLE 1. ADHESIVES CONTRACTS

Agency	Contract No.	Description
NASA/MSFC	NAS-826.84 (Modification 7)	Establish tests and guidelines for use of insulative adhesives in hybrid microcircuits.
NASA/MSFC	NAS-826384 (Modification 8)	Establish tests and guidelines for use of conductive adhesives in hybrid microcircuits.
Army/ECOM	DAAB07-74-C-0637	Evaluate reliability of adhesives used in ALT microcircuits, establish tests and guidelines for selection and in-process control for adhesives.
Army/ECOM	DAAB07-76-C-1311	Establish low cost standard accelerated test to determine effects of adhesive outgassing products on hybrid microcircuits.

ADHESIVE BOND STRENGTH

The main function of an adhesive is to mechanically attach devices, substrates, and other hybrid components. Hence, the initial adhesive bond strength and retention of this strength after subsequent processing conditions, stress tests, and long-term operation are important quantitative data. Six electrically insulative and six conductive adhesives were used to bond a variety of devices and materials simulating hybrid surfaces (Table 2).

TABLE 2. ADHESIVE BOND STRENGTH TEST SPECIMENS

	Glazed Alumina	Unglazed Alumina	Thin Film Gold	Thick Film Gold	Aluminum Panels
Silicon Chips	X	X	X	X	
Gold Backed Resistors			X		
Aluminum Panels					X
Viclan Capacitors Small (50 x 40 x 40 mils)			X		
Viclan Capacitors Large (170 x 125 x 65 mils)			X		
Monolithic Dielec- tric Capacitors Medium (100 x 50 x 40 mils)				X	

The shear strength to completely detach the adhesively bonded chips was measured using a micro-shear tester. Measurements were made at room temperature, at 150°C, and sequentially after immersing in three cleaning solvents, stress testing to MIL-STD-883 Class A, and burning-in at 150°C for 240 hours. In almost all cases, the shear strengths were very high, well above 1,000 psi, and considered more than adequate to meet military requirements (Table 3). Two failure modes, however, occurred during this testing. Corners of silicon chips broke loose at the 30,000g acceleration level and were clearly due to insufficient adhesive coverage at the chip corners (Figure 1). Also, microcracks and separation occurred when capacitors bonded with DuPont 5504 were exposed to Freon TMC solvent (Figure 2). This is not surprising since Freon TMC contains methylene dichloride which is known to soften and attack epoxies. In separate experiments where 2,000 hours aging at 150°C was conducted, only two adhesives degraded to less than 1,000 psi. Capacitors bonded with several adhesives were thermal cycled (-65°C to 150°C) up to 500 times. Though little deterioration of bond strength was noted, capacitors bonded with several of the adhesives (Hysol 0151 and Eccobond 104) developed microcracks sometime between the 200th and 500th thermal cycle. All capacitors, however, passed 200 cycles without any visual or functional degradation -- a stress test that far exceeds the military requirement of 10 thermal cycles. The general conclusion from these bond strength results is that most adhesives retain sufficient strength even after undergoing sequential MIL-STD-883 tests combined with solvent exposure, and after long-term elevated temperature aging and thermal cycling.

For specification purposes, it is difficult to arbitrarily set a minimum shear strength requirement because this is a function of the mass of the device, the bonded area, and the acceleration forces to which the hybrid will be subjected. Hence, in our specification (reference 4) we have defined



Figure 1. Chip with corner missing.



Figure 2. Viclan capacitor with lifted adhesive after solvent Freon TMC exposure.

a minimum shear strength which must be equal to or greater than 10S, where

$$S = \frac{9.8Wg}{A}$$

W = the weight of the device or substrate in kilograms

g = the constant acceleration requirement

A = the bond area in m²

S = the pressure exerted on the bond line in Newtons/m²

A safety factor of 10 was specified so that the shear strength of the adhesively bonded device is at least 10 times the theoretically calculated value for device detachment. S may be converted to psi by multiplying by 1.45 x 10⁻⁴.

TABLE 3. SUMMARY OF ADHESIVE BOND STRENGTH TESTS AND RESULTS

Sequential Tests

Immersion in Freon TF,
isopropyl alcohol, and
Freon TMC

Essentially no change, fillet
separation after immersion in
Freon TMC on DuPont 5504 bonded
capacitors.

After MIL-STD-883,
Class A Tests

All >1000 psi
Many improved
One chip failure at 30,000 g
due to insufficient adhesive.

After 240 hours at 150°C

No change
All >1000 psi

Parallel Tests

Initial at R.T.

Most >3000 psi
All >1000 psi
Little difference between glazed
and unglazed substrates.

At 150°C

Most retained >1000 psi,
DuPont 5504, <100 psi, but
reversible.

After 2000 hours at 150°C

No change,
All >1000 psi except Cu-filled
epoxy (800 psi) and Epo-Tek H55
(one failure).

Capacitors - 500 thermal
cycles, -65 to 150°C

No change, some improved;
Microcracks after 200 cycles for
some adhesives.

ELECTRICAL STABILITY

The second main function of an adhesive is to provide either an electrical contact (electrically conductive adhesive) or dielectric isolation (electrically insulative adhesive). In either case, the long-term retention of electrical properties is important. In our studies, we have shown that some conductive adhesives display erratic resistances which increase significantly on aging at 150°C. This can be due to chemical oxidation of metal fillers or to a time-temperature chemical interaction of one of the epoxy constituents with the metal fillers. To measure the electrical stability of conductive adhesives, a test was set up simulating actual conditions for chip capacitor bonding. Gold terminated capacitors (Monolithic Dielectric 100 x 50 x 40 mils) were attached with silver, gold and copper-filled epoxies to thick film gold pads on a ceramic substrate. The D.C. bond resistances were measured by probing from the top of the gold terminals to the thick film gold pad adjacent to the bottom of the capacitors. The specimens were aged at 150°C and measurements were made at incremental periods up to 1500 hours (Table 4). The resistance of one silver-filled epoxy, in particular Epo-Tek H-31, increased significantly and behaved erratically. The two gold-filled epoxies (Ablebond 58-1 and Epo-Tek H-44) were extremely stable over the entire 1500 hours of aging at 150°C. As a result of this work, a requirement was established that changes in average values of resistance should be no greater than a factor of five over initial values to qualify for military or space applications (reference 4). For some circuit functions, however, this factor may have to be even less.

THERMAL STABILITY AND OUTGASSING

There is considerable concern among the military/NASA procurement agencies on the extent of outgassing, nature of the outgassed products, and the effects on hybrid devices and metallization. This concern is not unfounded considering the bad experiences that were encountered when epoxies were first introduced some fifteen years ago for semiconductor packaging. Since then, it has been shown that with care in the initial selection of the adhesive, and with further care in the processing of the adhesive (cure, post-cure, vacuum baking and temperature exposure conditions) the percent of outgassed products can be kept to a minimum and adhesives may be chosen that evolve only inert gases. The thermal stability of an adhesive may be quantitatively determined by thermal gravimetric analysis (TGA) -- a precision method for dynamically recording the weight loss as the sample is heated at a constant rate of 10°C/minute to a temperature of 400°C. TGA curves, referred to as pyrograms, were obtained for many adhesives. The most thermally stable of the adhesives tested was Eccobond 104; among the least stable adhesive was Ablebond 150-6 (Figure 3). All organic adhesives were found to decompose at 350 to 375°C. For purposes of the specification, a requirement of less than 0.3% weight loss at 250°C as determined from the TGA curve was established.

Though TGA is a quick, easy and quantitative method for determining thermal stability over a temperature range, it does not provide outgassing data as a function of time at constant temperature. Unfortunately, there is no quick method for determining this; adhesives must be aged at elevated temperatures for at least 1000 hours and weight losses measured periodically.

TABLE 4. DC BOND RESISTANCES (MILLIOHMS) OF ELECTRICALLY CONDUCTIVE ADHESIVES AFTER AGING AT 150°C

	Hours at 150°C									
	Zero	24	48	120	264	572	720	810	1200	1500
Silver-Filled Epoxy (36-2)	5.3	5.9	6.2	7.1	6.8	9.1	9.4	9.6	11.2	12.5
Silver-Filled Epoxy (H-31)	6.6	11.0	18.9	80.2	139.7	202.0	171.0	236.0	197.0	281.0
Gold-Filled Epoxy (58-1)	6.6	6.6	6.3	6.7	6.2	6.7	6.4	6.4	5.5	6.4
Gold-Filled Epoxy (H-44)	5.7	5.7	5.1	6.5	5.9	6.2	6.0	5.8	5.4	6.1
Copper-Filled Epoxy (163-14)	17.4	11.6	-	11.7	12.3	-	12.4	12.2	13.7	14.9

Note: All values are average of 16 bond measurements.

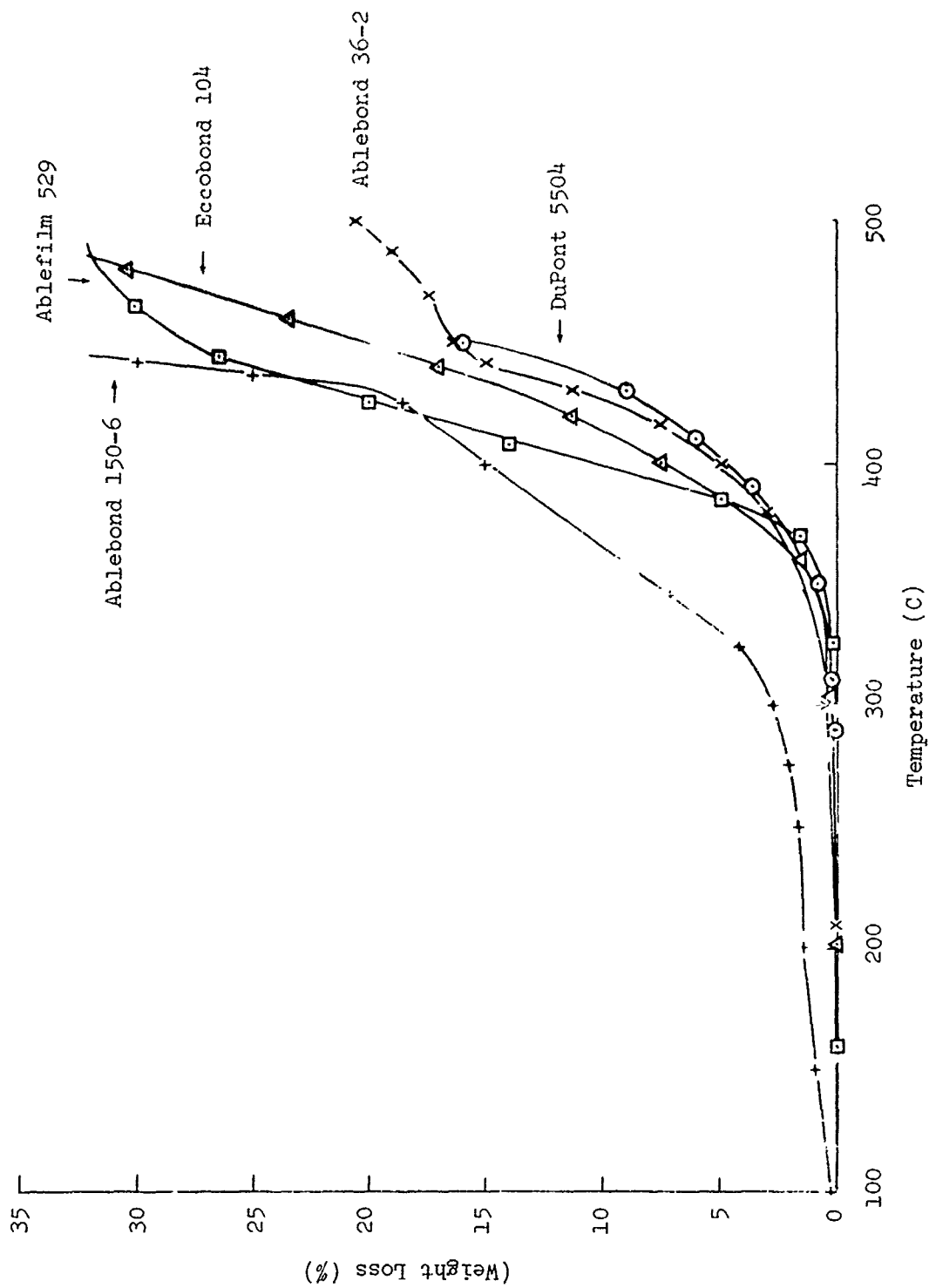
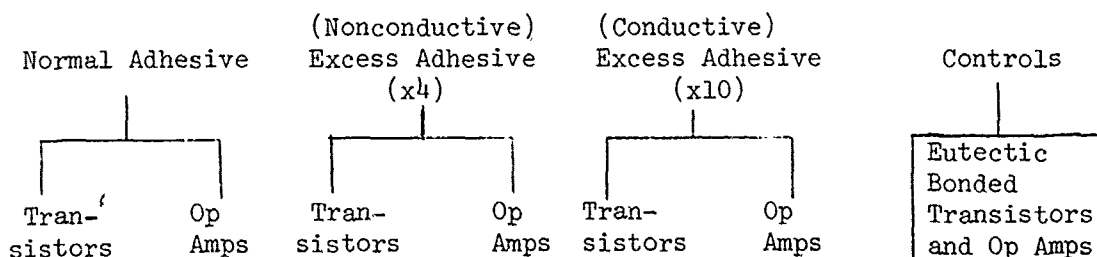


Figure 3. Thermal gravimetric analysis of several adhesives (temperature rise 10°C/min. in N₂).

In Figures 4 and 5, weight loss data for some electrically conductive and nonconductive adhesives at 150°C are plotted as a function of time to 1,000 hours. In interpreting these data it should be noted that there are several mechanisms for outgassing. First, residual solvents used in the formulation of the adhesive and adsorbed or absorbed water will be driven off during the first few hours at 150°C. Some highly polar solvents such as dimethylformamide or tetrahydrofuran may require longer (up to 24 hours) for complete removal. Post-curing or vacuum baking prior to sealing a hybrid package will usually remove these gases. Secondly, low molecular weight polymer fragments or additives that are not chemically bonded to the polymer may continue to be released over a long period of time (hundreds of hours) depending on their vapor pressures and the amount contained in the adhesive. Lastly, thermal decomposition of the polymer may occur which is indicated by a large positive slope in the weight-loss-time curve. Adhesives that gradually or rapidly decompose at 150°C, such as Ablebond 150-6, should not be used. Adhesives which outgas according to the first two mechanisms can be used if process controls such as postcuring and vacuum baking are used. As a specification requirement, we have established a maximum of 1% weight loss at the end of 1,000 hours at 150°C in nitrogen.

EFFECTS OF OUTGASSED PRODUCTS ON DEVICE PERFORMANCE

Though we have set requirements for the maximum amount of outgassing allowable, little correlation has been found between the amount of outgassing and electrical degradation of devices. We have found, however, that the nature of outgassed products is more critical than the amount. Characterizing the gases chemically and determining which are damaging to devices involves a long and expensive program. For example, mass spectrographic analysis of outgassed products can indicate dozens of different compounds many of which cannot be clearly identified because they exist as fragments or free radical species. Therefore, a semi-empirical approach is dictated: measuring the effects of the outgassed products from a particular adhesive on devices that are considered to be the most sensitive to contaminants. For the Army Airborne Laser Tracker (ALT) hybrid circuits, we selected a npn transistor (2N2222A) and an operational amplifier (LM741) as the two most sensitive devices. Test circuits were fabricated; each transistor circuit contained nineteen transistors and each op amp circuit contained ten op amps. Specimens were fabricated in which devices were mounted with the normal amount of adhesive, with four times the normal amount of insulative adhesive, and with ten times the normal amount of conductive adhesive. Other circuits, used as controls, were eutectically bonded.



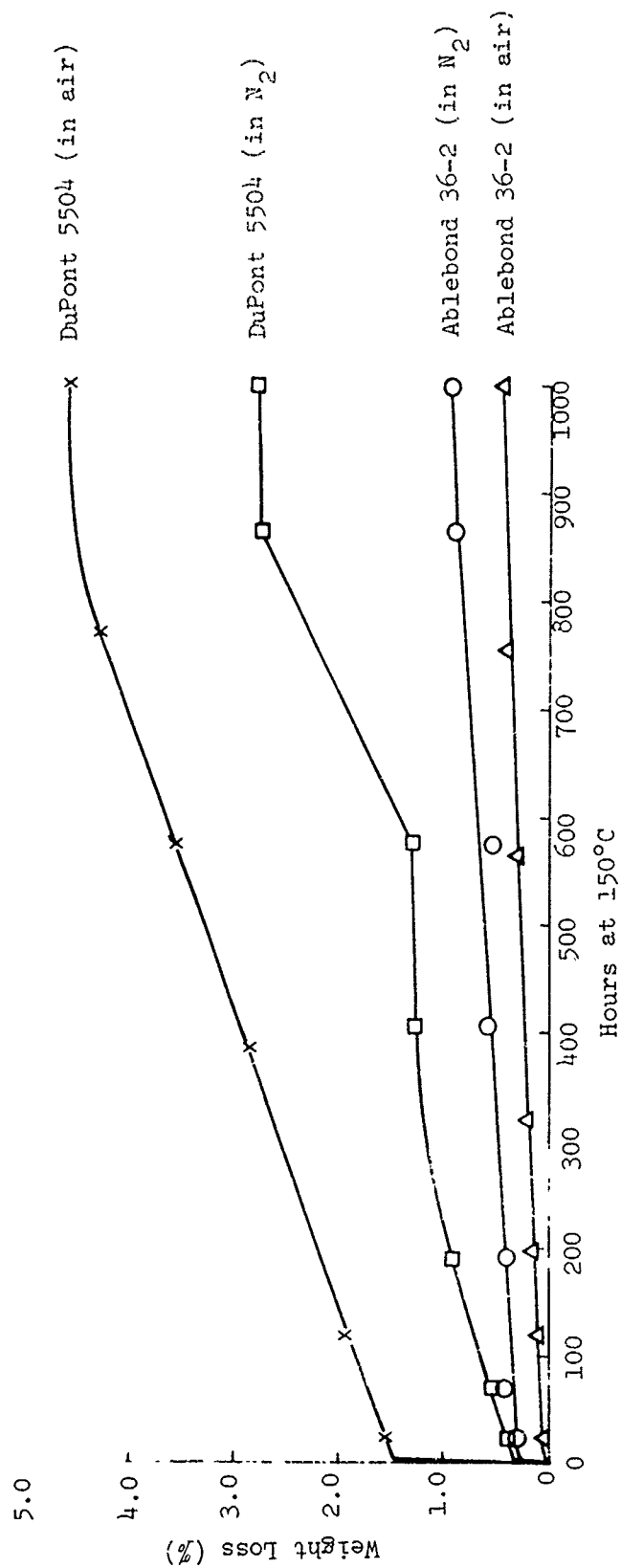


Figure 4. Weight loss of conductive adhesives versus time at 150°C in air and nitrogen.

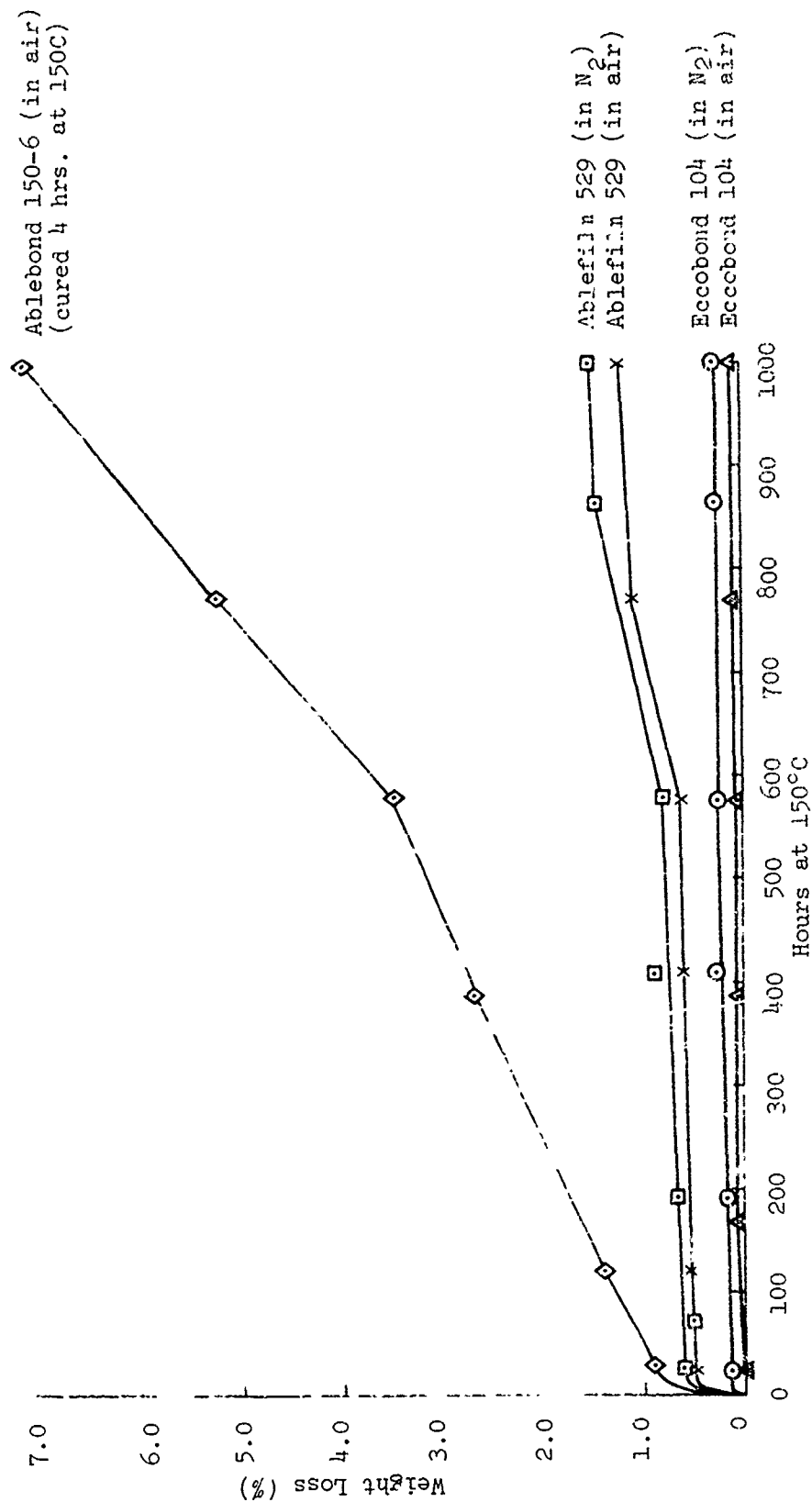


Figure 5. Weight loss of insulative adhesives versus time at 150°C in air and nitrogen

The transistors were reverse biased at 125°C for 1000 hours and I_{CBO} measured and used as an indicator of adhesive outgassing (Tables 5 and 6). Devices where I_{CBO} exceeded 10 na, were considered failures. For the npn amps, changes in V_{OFFSET} , I_{B+} and I_{B-} were monitored and the criterion for failures was out-of-specification values. Of the four adhesives tested, only Ablefilm 529 used in four times the normal amount was found to degrade the I_{CBO} values for the transistors. Eight failures out of 18 occurred after only 187 hours increasing to 10 failures at the end of 1000 hours. Acetone or methyl ethyl ketone solvents are possibilities for the increase in I_{CBO} . It is interesting to note, however, that DuPont 5504, which was a greater outgasser than Ablefilm 529, had no effect on the transistors. The operational amplifiers were not affected by any of the adhesives. The failures which occurred with the Ablebond 36-2 in ten times the normal amount are not considered to be due to adhesive outgassing because the second set showed no failures and because no more failures occurred as a function of time. A need exists for a standard test to determine the effects of outgassed products on electronic devices. Off-the-shelf devices that are reproducibly sensitive to contaminants are to be selected and a set of test conditions defined for qualification. It is the objective of the current Army/ECOM program to establish this test.

SUMMARY

In summary, four adhesive material properties that are important for the reliability of microcircuits have been discussed. Several conclusions drawn from these studies are:

- ° Adhesive bond shear strength and retention of strength are not a serious problem with device attachment with the exception of large capacitors and large substrates.
- ° Electrical bond resistance changes occur with some silver-filled epoxies.
- ° Large differences among adhesives exist in their outgassing rates and amounts -- some show decomposition and should not be used. The anhydride cured epoxy (Eccobond 104) displayed the lowest outgassing of all adhesives tested.
- ° The chemical nature of outgassed products is more critical than the amount.

- Solvents evolved from Ablefilm 529 degraded the I_{CBO} values for npn transistors.

TABLE 5. LEAKAGE CURRENT FAILURES FOR NPN TRANSISTORS*

Circuit	Adhesive	Transistors	I _{CBO} Failures			
			187 Hours	528 Hours	702 Hours	1011 Hours
1	None	17	1	1	1	1
2	DuPont 5504	19	0	0	0	0
3	DuPont 5504 (10X)	18	0	1	1	0
4	Ablebond 36-2	18	0	0	0	0
5	Ablebond 36-2 (10X)	17	0	0	0	0
6	Eccobond 104	18	0	1	1	1
7	Eccobond 104 (4X)	13	0	1	1	0
8	Ablefilm 529	15	1	1	1	1
9	Ablefilm 529 (4X)	18	8	9	11	10

* I_{CBO} greater than 10 nanoamps constituted the failure criterion.

TABLE 6. OPERATIONAL AMPLIFIER FAILURES

Circuit	Adhesive	Operational Amplifiers Tested	Failures			
			187 Hours	528 Hours	702 Hours	1011 Hours
1	None	10	0	0	0	0
2	None	10	0	0	0	0
3	DuPont 5504	10	0	0	0	0
4	DuPont 5504	10	0	0	0	0
5	DuPont 5504 (10X)	10	1	1	1	1
6	DuPont 5504 (10X)	10	0	0	1	1
7	Ablebond 36-2	10	0	0	0	0
8	Ablebond 36-2	9	0	0	0	1
9	Ablebond 36-2 (10X)	10	4	4	4	1
10	Ablebond 36-2 (10X)	10	0	0	1	0
11	Eccobond 104	10	0	1	1	2
12	Eccobond 104	10	1	1	1	1
13	Eccobond 104 (4X)	9	0	0	0	1
14	Eccobond 104 (4X)	10	0	0	0	1
15	Ablefilm 529	10	0	0	0	0
16	Ablefilm 529	10	0	0	0	0
17	Ablefilm 529 (4X)	9	0	0	0	0
18	Ablefilm 529 (4X)	10	1	1	1	1

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QUALIFICATION REQUIREMENTS FOR THICK-FILM NETWORKS -
IN-PROCESS CONTROLS AND INSPECTIONS

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SUMMARY

An in-process quality control plan has been developed for the thick-film process.¹ This plan consists of a series of flow charts, a description of the processing steps, and specific inspection criteria for three reliability levels. The quality control plan is discussed in the context of the three reliability levels.

BACKGROUND

This plan was developed under contract DAAB07-73-C-0326 with the U.S. Army Electronics Command, Fort Monmouth, New Jersey. Preliminary work involved studying the literature and surveying the hybrid industry to determine what materials and processes were in common use, what failure modes have been observed, what corrective action eliminated these failures, and what potential problems existed in the technology. From the results of the survey and literature search, an industry consensus was determined.² Failure modes were ranked in order of significance and versus failure mechanisms.³

From all this information, flow charts were developed listing every common step in the thick-film process. Inspection points were added where necessary, and the inspection criteria were developed. The aim of the inspection plan was to be cost-effective. In other words, the bulk of the inspections are in-process inspections which locate failures or potential failures as early in the process as possible. This eliminates wasting time and money on further processing of an already out-of-tolerance network. It also greatly reduces the amount of costly post-processing screening tests.

It must be pointed out here that this paper deals only with networks constructed by thick-film screen-dry-fire techniques using thick-film conductor, resistor, and dielectric materials applied to ceramic substrates in circuit patterns, and does not include any components attached by any other means. The scope of this paper deals only with the networks as defined above, and does not encompass any component attachment technique except to the extent that the quality of the film affects the attachment of the component.

THE THICK-FILM PROCESS

Figure 1 is an overview chart of the thick-film process. The entire process is presented from the left, starting with the particular circuit requirements and the universal specifications (universal for all circuits manufactured at any one facility). These are shown in the blocks to the left of the dotted line. To the right of the dotted line are the major processing steps:

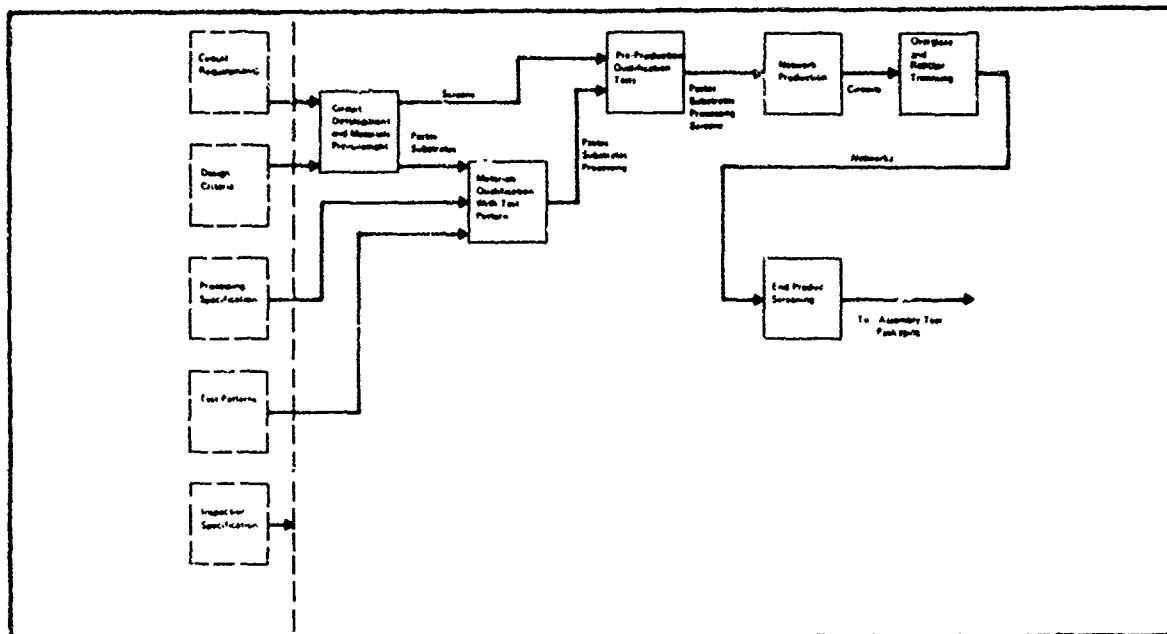


Figure 1. Thick-Film Process Control Flow Chart

- Circuit Development and Materials Procurement
- Materials Qualification with Test Pattern
- Pre-Production Qualification Tests
- Network Production
- Overglaze and Resistor Trimming
- End-Product Screening

Each of these major processing areas is further expanded in a separate flow chart. Figure 1 also shows the interrelation between the major processing areas, as well as the inputs and outputs of these areas.

The starting point for any thick-film network is Circuit Requirements. These requirements are grouped into four major areas: Electrical Performance; Physical Performance; Reliability Requirements; and Environmental Performance. The various circuit specifications under each area are listed in Figure 2. The specifications listed may be considered a shopping list from which the network user should specify particular requirements. These requirements will vary greatly as a function of reliability, use, environment, life, circuit purpose, etc. Not all of the requirements listed will be defined for each and every network manufactured. Care must be taken by the user to specify all parameters which are important, but not to overspecify, since this can easily cause a drastic and unnecessary increase in cost due to the difficulty in fitting a design to the specifications. Specifications should be as complete and as loose as possible. Without proper and accurate circuit specifications, the final reliability level will be difficult to achieve.

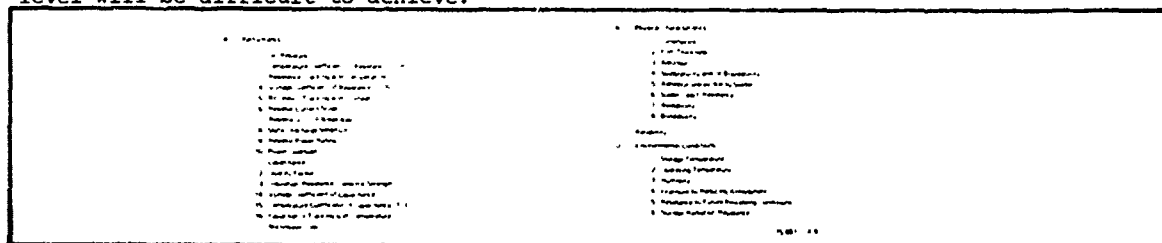


Figure 2. Circuit Requirements

Thick-film network reliability begins with sound design criteria. The thick-film designer must be able to meet his circuit specifications within the manufacturing limits of the thick-film process, which includes the limitations of the materials. Some of the areas where sound design considerations are important include: Minimum conductor spacing; Minimum pad widths; Tolerances on dimensions; Conductor/resistor overlap; Conductor/component overlap; Hole drilling and plating; Resistor tolerances; Minimum resistor width and spacing; Power dissipation; Dielectric overlap.

The thick-film processing specification is a universal specification for all circuits produced at any one facility. The specification generally includes: Reference Documents; Safety Precautions; Documentation Requirements; Equipment to be Used; Operations to be Performed; and Quality Assurance Provisions. The specification is generally written about a process or part of a process. Each thick-film manufacturing facility generates its own process specifications that are applicable to the particular processes and equipment used by that facility.

Obviously, the most directly important areas of the processing specification are descriptions of the equipment used and the operations to be performed. The equipment used by the manufacturing facility is listed, including model numbers and specific options. The environment in which the work is to be performed is also discussed. The discussion of the operations to be performed includes the production sequence for that part of the process, the production options, and the equipment or material parameters which must be controlled.

Another important area of the processing specification is the documentation. Record keeping procedures must be outlined and followed, to include a listing of all the parameters used for each manufacturing lot. A manufacturing log book must be kept which lists, by lot number, the settings actually used and the measurements actually made on the film (such as thickness or average fired sheet resistance).

The third area of major importance in the processing specification is the area of Quality Assurance Provisions. This area lists the important tests and controls which must be imposed upon the processes, such as thickness measurements, electrical measurements, or process parameter measurements, and generally describes the procedure for measurement and the limits or tolerances permitted.

Each manufacturing facility generally develops a series of test pattern screens which are used in paste and substrate evaluations, either for preliminary evaluation of new products or for the standard material qualification testing of new manufacturing lots. These patterns must be designed so as to test all of the properties of the materials as well as variations in the processes. Some examples of useful test patterns could include microwave resonator, microwave meander line, resistor test pattern, conductor test pattern (bondability, solderability, adhesion, etc.), and print resolution test pattern.

Each thick-film manufacturer must follow an inspection specification which must describe the location of each inspection point in the process, and detail the inspections to be performed at those points, referencing standardized inspection methods or detailing new methods, together with the allowable limits. Causes for sample or lot rejection must be discussed, as well as whether or not samples tested may be processed further (nondestructive vs destructive tests). The inspection specification should consist of several levels of reliability, with the highest reliability level receiving the most stringent inspection.

The three major types of inspections used are visual, mechanical (physical) and electrical. Each type of inspection has its own purpose. The visual inspection involves looking at the circuit (or screen, or material) to determine if everything looks as it should; for example, if there are voids or scratches in the print, or if a spot appears on the photo-reduction. The mechanical inspection involves physical measurement, such as dimensions and tolerances. Such measurement can be done with a calibrated reticule eyepiece on a stereo microscope or with high precision, complex measuring equipment. The electrical inspections consist of measurements such as resistance, microwave insertion loss, or voltage breakdown and can be performed before, during, or after environmental

tests. Electrical inspections are generally the most directly related to a network's performance in actual use, but are usually the most expensive to perform. On the other hand, visual inspections are generally the least costly to perform, but have the least relation to actual performance. A tradeoff, then, exists between applicability and cost. It must be emphasized that inspection criteria should be as practical and as closely related to the circuit requirements as possible, since dogmatic and unrelated inspection requirements add to the cost and difficulty of producing a thick-film network without adding to the assurance of reliability. In general, the lower reliability levels involve relaxed inspection criteria or elimination of some inspections. The reliability levels discussed here are designated as Level 1, Level 2, and Level 3, with Level 1 being the highest reliability level of the three, and Level 3 being the lowest. These reliability levels cannot be related to real life failure rates due to lack of acceleration factor information, and, therefore, are qualitative.

Circuit Development and Materials Procurement

The first solid block in Figure 1 to the right of the dotted line is Circuit Development and Materials Procurement. This major processing area is further expanded in detail in Figure 3 showing each of the processing steps and inspection points.

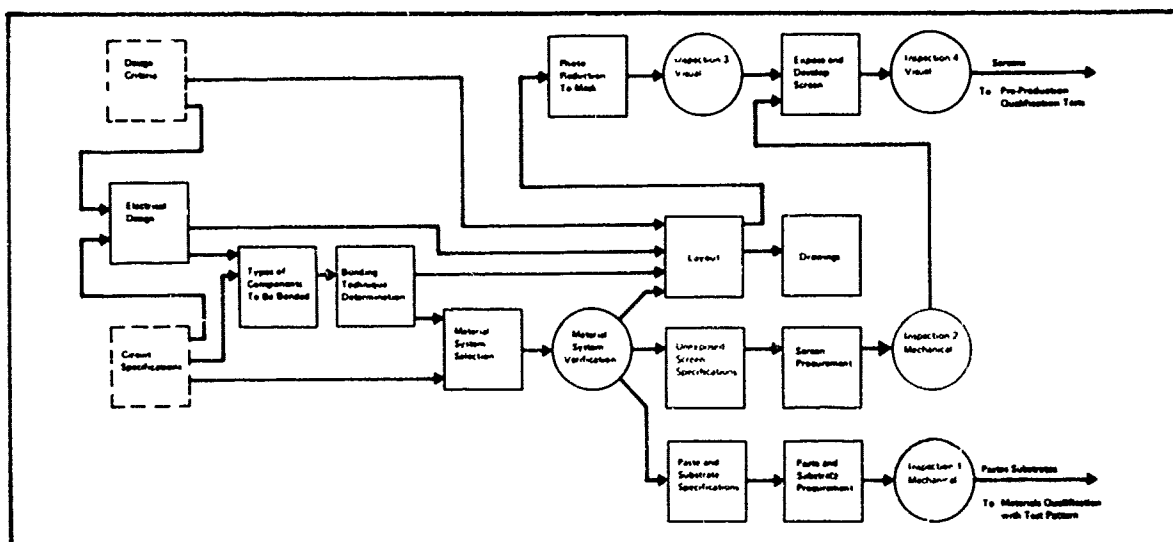


Figure 3. Circuit Development and Materials Procurement

Four symbols are used in this chart and the charts that follow. They are the dotted block, the solid block, the diamond, and the circle. Explanation of the meanings of these symbols is discussed in Figure 4. It should be noted that the output arms of each inspection step are items or lots which have passed the inspection. If an item or lot fails a particular inspection, the result is either item or lot rejection, or process modification, or both. These outputs of the inspection steps are not shown graphically on the flow charts but are discussed in the individual paragraphs about each inspection point.

It should be pointed out that an average manufacturing procedure has been used in the development of these charts. For example, some manufacturing facilities send their 1:1 layout masks to an outside vendor who exposes and develops the screens. Other thick-film network manufacturers buy or make their own screens, apply the emulsion themselves, and expose and develop their own screens. Still others take a middle-of-the-road approach, and buy emulsion-coated screens from an outside vendor and expose and develop them in-house. This is the approach that has been taken in preparing these charts. Slight modification of the processing or inspection steps may be required to adapt this procedure exactly to the manufacturing sequence of a particular facility.

The electrical design must be based on the Thick-Film Design Criteria and the specifications for the particular circuits. Besides meeting all electrical requirements, the designer must remain aware that the circuit will be manufactured by thick-film techniques.

Selection of the types of components to be bonded to the network is based on the circuit specifications and electrical design. Types of components include chip capacitors, chip resistors, beam lead devices, semiconductor chips, and packaged components.

Once the types of components to be bonded have been determined, the bonding techniques must be identified. Bonding techniques include soldering, brazing, thermocompression and ultrasonic wire and chip bonding, back bonding, and epoxy bonding.

Based on circuit specifications and bonding techniques, the thick-film materials to be used must be selected. These materials include the substrate and the conductor, resistor, and dielectric materials. Considerations on which to base this selection include materials compatibility, resistance range, trimming techniques, conductance, TCR, dielectric constant, and substrate hold down technique. These decisions should be made jointly between the design engineer and the thick-film manufacturing facility.

When the materials combination has been chosen, some preliminary verification that the materials will act as expected is needed. This verification may be in the form of data from the materials manufacturer, data from other manufacturers, previous experience, or specific tests, depending on reliability level, as shown in Figure 5a. If the materials combination chosen will not meet the expected requirements, new materials must be selected. If this is not possible, the circuit specifications, electrical design or bonding techniques will have to be modified.

Pastes and substrates may be specified by as little as a manufacturer's part number, but generally, tighter specifications must be imposed. Depending on the paste and requirements involved, it may be necessary to specify viscosity, percent solids content, content of impurities, as well as some physical and electrical parameters when the paste is screened in a particular manner on a particular substrate. Some of these additional parameters are line width and resolution, conductivity, bondability, solderability, adhesion, resistance, TCR, trimability, dielectric constant, and compatibility with other materials used. In such instances, the paste manufacturers should be made aware of the printing, drying, and firing processes to be used, the substrate materials to be used, and any other pastes that will be used.

Substrates may need to be specified by very tight controls on dimensions and tolerances, including length, width, thickness, camber, and deviation from 90° corners. In addition, grain size, surface finish, purity, make-up of impurities, and dielectric constant, as well as specific performance data, may need to be specified in a manner similar to that outlined for paste specifications.

As a caution against over-specification, it should be noted that in general, the tighter the specifications to outside vendors the higher the cost of materials. In addition, some suppliers may not respond to overly tight specifications.

The procurement cycle generally consists of writing a purchase order to buy a particular quantity of the materials according to the specifications discussed in the previous paragraphs. Materials are received by a receiving department and sent to incoming inspection.

In addition to checking part number and quantity, the incoming inspection (Inspection 1) must consist of a physical inspection of the material. The substrates must be checked to see that they meet all the dimensions and tolerances, and that they are not cracked. The pastes must have their viscosities measured and recorded. These examinations should be performed under clean-room conditions, and the degree of examination per reliability level is shown in Figure 5b. If the materials pass this physical inspection, they are then subjected to a qualification test using a standard test pattern, as described below. If the materials fail to pass the mechanical inspection, they shall

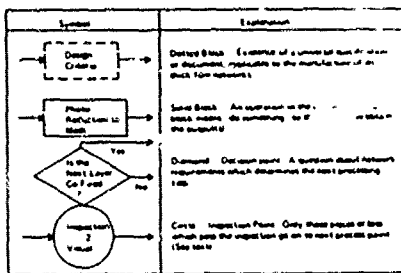


Figure 4. Explanation of Symbols

Inspection	Item	Level 1	Level 2	Level 3
1. Material System Verification	System	Material Qualification with Test Pattern	Process to Mount Experiment	Manufacturer's Data
2. Inspection 1 Mechanical	All Substrate Patches	Part No. & Qty Dimensions, Tolerances, Grains 1000, Grain Size Comparison Viscosity at 3 shear rates, Chemical analysis	Part No. & Qty Dimensions, Tolerances, Grains 33.3 per cent Single point viscosity	Part No. & Qty Dimensions, Tolerances, Grains, 10 percent Single point viscosity
3. Inspection 2 Mechanical	Unexposed Screens	Dimensions & Tolerances under yellow light 50% sample	None	None
4. Inspection 3 Visual	Masks	10x 20x Visual for shorts, gaps, voids, exposure sharpness. Compare and for all critical dimensions	10x 20x Visual for shorts, gaps, voids, exposure sharpness. Compare and for all critical dimensions	10x 20x Visual for shorts, gaps, voids, exposure sharpness. Compare and for all critical dimensions
5. Inspection 4 Visual	Critical Screens	Pattern dimensions with comparison 10x 20x white light to verify complete screen matching and good emulsion adhesion	Pattern dimensions with comparison 10x 20x white light to verify complete screen matching and good emulsion adhesion	Pattern dimensions with comparison 10x 20x white light to verify complete screen matching and good emulsion adhesion

Figure 5. Criteria for Inspections of Figure 3

be returned to the vendor for replacement. A list of the parameters that were "out-of-spec" shall accompany the items returned to the vendor.

Based on the material system to be used, unexposed screens must be specified. Parameters to be specified include length, width, mounting dimensions, mounting orientation, wire mesh type and size, emulsion type, and emulsion thickness. Considerations in choosing the screen parameters include desired line width, line thickness, and particle size of the solids in the paste.

Screens are ordered to the specifications developed above. Except in the case of Level 1 Reliability, screens are not inspected, in order to prevent accidental exposure. Level 1 Inspection (Inspection 2) would be performed under yellow light, and would include 50% sampling checks of the screen dimensions, etc. See Figure 5c.

The circuit layout for the thick-film network is influenced by the design criteria, the materials being used, the bonding techniques, and the electrical design. The layout is generally done at a greatly expanded scale (about 10:1 or 25:1) and is usually cut from stabilene material or made by sticking opaque tape to clear film material. For extremely close tolerances, the layouts must be mechanically generated, such as by use of a coordinatograph or Gyrex or Gerber plotters.

Drawings, when required, are usually generated from the circuit layout. They may be used as assembly aids or inspection guides throughout the process, and must include sufficient information to start production of the network from scratch at some later time.

The layout pattern is photo reduced to 1:1 size of the circuit. It is necessary to carefully control the camera settings (focus, reduction, and exposure), as well as the development process. The mask may be on film or glass.

The mask must be inspected, (Inspection 3) using a 10 to 20 power microscope, to determine that any critical dimensions (gap widths, line widths, line lengths, etc.) are correct, and that all areas are free of scratches and spots which could cause shorts or unwanted gaps. Reduction size should also be checked, as well as overall exposure and edge fuzziness. See Figure 5d. If the mask does not pass this inspection, it may be possible to accurately correct it by hand scraping or touch-up ink. If not, the layout must be photographed again. If this still does not correct the problem, the layout may be at fault and it may need to be changed.

The blank screen is exposed using the mask as prepared above. The exposed screen is then developed in accordance with the manufacturer's directions. Exposure and development must be properly controlled.

The exposed screen is inspected (Inspection 4) according to the information in Figure 5e. Screens which do not pass this inspection must be scrapped and new screens

must be made. Sometimes the layout or photo reduction may be at fault by not taking into account the necessary process-induced deviations. In these cases, the layout or reduction will need to be adjusted.

The circuit pattern screens are used next in the Pre-Production Qualification Test.

MATERIALS QUALIFICATION WITH TEST PATTERN

Once the thick-film materials (pastes and substrates) have been ordered and received, they must be qualified on a lot-by-lot basis. Each new lot of materials (a lot being a batch of material being manufactured by the vendor at one time) must be re-qualified. This is done by screening the paste on the substrate using standard test pattern screens and a standard processing procedure. It must be emphasized that only the particular test pattern screens that are applicable to the circuit in question should be used.

As can be seen in Figure 6, the pastes and substrates which were procured and inspected, as described above, are processed using the test pattern screens and processing specification.

Test patterns are printed, dried, fired, and trimmed in the normal processing manner (see Figures 13 and 15). All inspections within the production and trimming areas are shown in Figures 13 and 15. In addition to recording the processing parameters used, any peculiarities noticed by the operators should also be recorded in the paste qualification log book. Also, a correlation must be made for future reference between wet line width, dried line width and final line width. Several dried but unfired printed substrates should be stored until the materials involved have been completely consumed. These substrates can be used as standards to help identify causes of loss of control of production processes.

Figure 7 details the mechanical inspection criteria (Inspection 5) for the printed, fired, and trimmed (where applicable) test patterns as related to the different reliability levels. The thickness of print should be measured with the equipment listed, and should not vary by more than the percentage indicated from other measurements of the same batch, other batches or lots, manufacturer's recommended thickness, or required thickness. If variation from required thickness occurs, a different screen emulsion thickness must be used, or another printing parameter must be changed. If variations within a batch or between lots occur, another processing parameter may have to be changed. The other dimensions and resolution of the materials/processes must be measured using the equipment listed, and must be within the tolerances listed with respect to the dimensions expected or required, or measured on previous batches or lots. General overall quality should be examined as indicated in the table. Quality must compare favorably with other lots and other pastes of the same type.

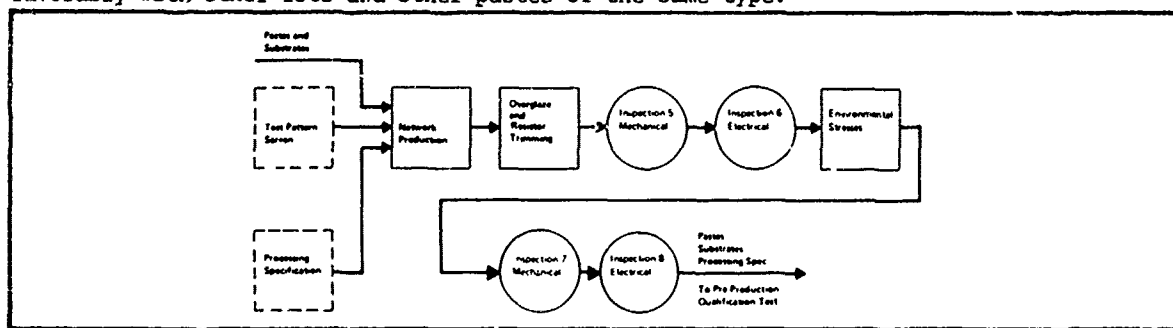


Figure 6. Materials Qualification with Test Pattern

Item	Level 1	Level 2	Level 3
Finish	Surface Preparation = 15%	Preparation or Finish = 20%	Overall or Final Inspection = 20%
Dimensions	Conformity = 1 Mil	Conformity = 2 Mils	Maximum variance = 5 Mils
Order Quantity	25% for properly identified, unmarked, standard components for all types, sizes and quantities, including changes of material type.	50% for properly identified, unmarked, standard, uniformity components, sizes and quantities, including changes of material type.	(Same as for Level 2)
Adhesion	Soldered 10% Bonded 10% Epoxied 10%	Soldered 20% Bonded 20% Epoxied 20%	Soldered 30% Bonded 30% Epoxied 30%
Bondability	Failure to bond = 2%	Failure to bond = 5%	Failure to bond = 10%
Solderability	Solder Pad Failure = 2%	Solder Pad Failure = 5%	Solder Pad Failure = 10%
Dewetting	Required Dips: 100 sec	Required Dips: 20 sec	Required Dips: 10 sec
Leaching	At 1000 psi stress = 20% Deposition	At 1200 psi stress = 100% Deposition	At 1000 psi stress = 100% Deposition

Figure 7. Inspection 5 and 16 Criteria

Adhesion measurements should only be made by the method of component attachment to be used in the finished assembly. For example, where components are to be soldered, measurements of soldered adhesion (using the same solder as will be used in assembly) should be made. Similarly, where thermo-compression bonding is to be used, that type of bonded adhesion should be measured. The percentage listed in the table indicates the maximum acceptable decrease in average adhesion value from the norm. Bondability (ease of bonding) should be measured by the degree of bonding process change necessary to achieve reliable bonds, and the percentage of times that the bond fails to adhere adequately to the bonding pad. Bondability should only be measured, of course, for materials/processing which will be used to produce networks to which components will be bonded. Bond pull tests (wires) or push tests (chips) should be used in the conventional way to determine reliability or strength of bonds. Solderability (solder wetting) should be measured only for materials/processing combinations to which components will be attached by soldering. Solderability should be tested using the particular solder or solders to be used during assembly. Pull testing should be used to see that adequate solder wetting has occurred. "Adequate" is defined as less than the percentage indicated of pads tested exhibiting the failure at the pad/solder interface. Dewetting or scavenging should be tested by subjecting the conductor pads to repeated 5-second dips in the molten solder. Total immersion time to dewetting is the test criteria listed. Leaching should be tested by a soldered pin pull test.⁴

Figure 8 lists the electrical inspection criteria (Inspection 6) by reliability level for each of the circuit elements. The electrical criteria, as with the mechanical criteria, should only be used when applicable to the circuit to be produced.

Substrate dielectric constant should be measured by using a resonator pattern. From the resonant frequency, the relative dielectric constant can be calculated. The dielectric constant should be within the percent indicated of previous measurements or expected results.

The important conductor parameters are conductance, current density capability, and microwave insertion loss. To measure conductance, the resistance of a long length of narrow line should be measured. The resistance must be within the tolerances specified by paste manufacturer and circuit requirements, as well as not varying by more than the percent indicated from previous measurements. The current handling capability of conductors should also be tested by using a long length of narrow line. The line is subjected to a short time current overload of 2-4 times rated or expected value. Maximum change in resistance (conductance) should be as indicated in the table. Microwave insertion loss should be measured using an 8-inch meander line. Insertion loss should be measured, in the frequency range of interest to the particular circuit, or across a wide frequency range if the material is for general use. The insertion loss, in dB, should be less than the value indicated in Figure 8, where frequency (f) is listed in GHz.

Dielectric constant, voltage breakdown, and insulation resistance are the electrical properties of dielectric films which must be verified. Dielectric constant can generally be measured by use of a capacitance test pattern. Capacitance should be within the tolerances shown with respect to previous measurements. Voltage breakdown and insulation resistance should have the safety margins shown in the table.

Resistance is the most obvious property of resistor films which must be measured. All resistors must be trimmable, which means that they must be below desired value by no more than the percentage indicated in Figure 8. If resistors are too high or too low, process adjustment (such as firing speed, firing temperatures, or print thickness) will have to be made. Temperature Coefficient of Resistance (TCR), when required, must be within the range required by the circuit and/or specified by the vendor. It should be noted that changing processing parameters to change after-firing values of resistance can have an effect on TCR. Current noise in resistors should be measured, when required, by standard (ASTM) methods, and should be within the range required or specified. Stability of the resistor under power overload is another important parameter. Overload effect should be measured by applying a 2-1/2 times rated power dissipation overload for 5 seconds. Resistance measurements made 30 minutes after the overload is removed should show a resistance change less than that indicated in Figure 8, relative to pre-overload measurements. Voltage breakdown is measured by applying a short time voltage of 3750 volts per inch of resistor length. Resistor value must not vary by more than the percentage listed in the table relative to initial measurements. Static discharge effect on resistors should be measured, when required, by allowing 5000 volts to charge through a 50 PF capacitor, and then to discharge through the resistor. Change in resistance should be within the percentages indicated in Figure 8. Physical abrasion effect on resistors should be within the tolerances listed. Abrasion can be performed by scratching the length of the resistor three times with the fingernail. Finally, print-to-print reproducibility of the resistor values should be within the percentage listed in Figure 8.

Figure 9 lists the environmental stresses to be performed on the screened test pattern substrates, and the parameters to be measured after each specific stress. Unless otherwise specified, each sample should undergo only one environmental stress; i.e., stresses are not to be cumulative. Measurements of the parameters indicated are to be made by the identical methods as were used under Inspections 5 and 6. Figures 10 and 11 list all acceptable limits of the after stress measurements for the mechanical (Inspection 7) and electrical (Inspection 8) parameters, respectively.

Element	Parameter	Level 1	Level 2	Level 3
Substrate	Dielectric Constant	Resistance $\pm 2\%$	Resistance $\pm 5\%$	Resistance $\pm 7\%$
Conductor Film	Conductance Current Density Maximum Loss	Resistance $\pm 10\%$ $2 \times$ \pm Rated $\Delta R < 0.5\%$ Insulation loss $< 10 \times 10^{-11} \text{ G/cm}^2$ $< 0.25 \text{ dB}$	Resistance $\pm 15\%$ $2 \times$ \pm Rated $\Delta R < 1\%$ Insulation loss $< 10 \times 10^{-11} \text{ G/cm}^2$ $< 0.4 \text{ dB}$	Resistance $\pm 20\%$ $2 \times$ \pm Rated $\Delta R < 1.5\%$ Insulation loss $< 0.10 \times 10^{-11} \text{ G/cm}^2$ $< 0.45 \text{ dB}$
Dielectric Film	Dielectric Constant Voltage Breakdown Insulation Resistance	Capacitance $\pm 10\%$ ≥ 2.5 times that req'd ≥ 2.5 times that req'd	Capacitance $\pm 15\%$ ≥ 2 times that req'd ≥ 2 times that req'd	Capacitance $\pm 20\%$ ≥ 1.5 times that req'd ≥ 1.5 times that req'd
Resistor Film	Resistance TCR Current Noise Power Stability Voltage Breakdown Static Discharge Abrasion Reproducibility	Trimtable $< 20\%$ low Within required range Within required range $2 \times$ \pm Rated $\Delta R < 0.5\%$ 3750 V/in. $\Delta R < 1\%$ 5000 V/50 μF $\Delta R < 1\%$ 3 scratches $\Delta R < 0.2\%$ Untrimmed $\Delta R < 30\%$	Trimtable $< 25\%$ low Within required range Within required range $2 \times$ \pm Rated $\Delta R < 1\%$ $\Delta R < 0.5\%$ 3750 V/in. $\Delta R < 2\%$ 5000 V/50 μF $\Delta R < 5\%$ 3 scratches $\Delta R < 0.25\%$ Untrimmed $\Delta R < 40\%$	Trimtable $< 30\%$ low Within required range Within required range $2 \times$ \pm Rated $\Delta R < 1.5\%$ $\Delta R < 0.75\%$ 3750 V/in. $\Delta R < 3\%$ 5000 V/50 μF $\Delta R < 10\%$ 3 scratches $\Delta R < 0.5\%$ Untrimmed $\Delta R < 50\%$

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Figure 8. Inspection 6 and 15 Criteria

Environmental Stress	Parameter
Temperature Cycling per MIL STD 202D Method 102A Test Condition C	Abrasion Voltage Breakdown Dielectric Constant Dielectric Film Dielectric Loss Dielectric Resistance Dielectric Stability Dielectric Voltage Breakdown
Thermal Shock per MIL STD 883 Method 1011 Condition B	Dielectric Resistance Dielectric Stability Dielectric Voltage Breakdown
Humidity per MIL STD 883 Method 1004.2	Abrasion Conductance Insulation Loss Dielectric Constant Dielectric Film Dielectric Loss Dielectric Resistance Dielectric Stability Dielectric Voltage Breakdown

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Figure 9. Environmental Stresses

Item	Level 1	Level 2	Level 3
Abrasion	$< 10\%$ degradation	$< 20\%$ degradation	$< 30\%$ degradation
Leaching	$< 35\%$ degradation	$< 45\%$ degradation	$< 75\%$ degradation
Cracking Film or Substrate	No evidence at 20h	No evidence at 10h	Insufficiency at 10h

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Figure 10. Inspection 7 Criteria

Item	Level 1	Level 2	Level 3
Conductivity	$\pm 10\%$	$\pm 15\%$	$\pm 20\%$
Insulation Loss	$< 0.10 \times 10^{-11} \text{ G/cm}^2$ $< 0.25 \text{ dB}$	$< 0.10 \times 10^{-11} \text{ G/cm}^2$ $< 0.4 \text{ dB}$	$< 0.10 \times 10^{-11} \text{ G/cm}^2$ $< 0.45 \text{ dB}$
Resistance Stability	$\Delta R < 1\%$	$\Delta R < 1.5\%$	$\Delta R < 2\%$
Dielectric Constant	$\pm 10\%$	$\pm 15\%$	$\pm 20\%$
Dielectric Voltage Breakdown	≥ 2.5 times that req'd	≥ 2 times that req'd	≥ 1.5 times that req'd

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Figure 11. Inspection 8 Criteria

PREPRODUCTION QUALIFICATION TEST

After the pastes, substrates, and processing specification have been approved in the Materials Qualification with Test Pattern, they are combined with the actual circuit screens (from Figure 3) for the Preproduction Qualification Test. Figure 12 is a flow chart for this part of the process.

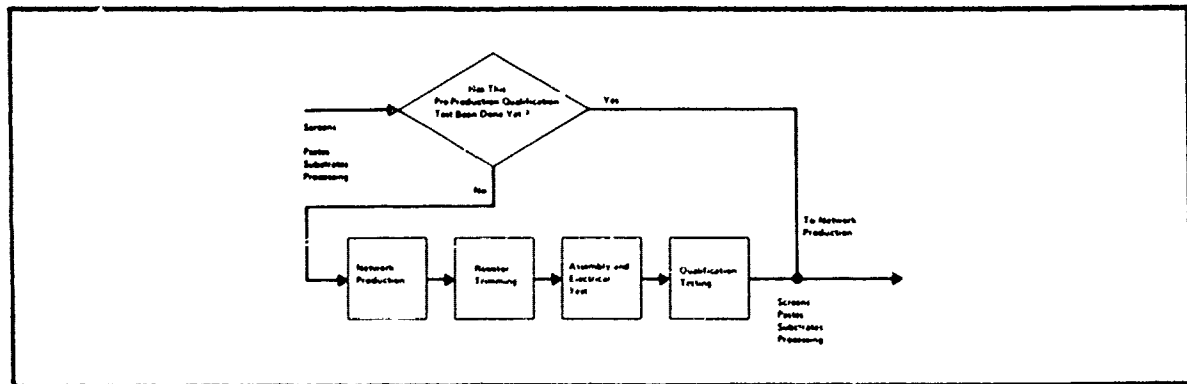


Figure 12. Preproduction Qualification Test

Several important differences exist between this test and the Materials Qualification with Test Pattern. First, this is a test of the circuit being manufactured, so it uses the actual circuit screens. Secondly, it includes component attachment, and possibly even some system integration to be able to properly test the circuit performance. Thirdly, the Preproduction Qualification Test must only be done once for each circuit (regardless of how many different material lots are used).

In summary of this test, a few preproduction networks are manufactured using actual production materials and controls. The completed preproduction networks are then sent to the assembly manufacturer for the purposes of producing preproduction assemblies. The thick-film network is qualified as part of the assembly qualification. The risk is low since the Materials Qualification with Test Pattern will have tested the materials and production processes, leaving only the screen and peculiar circuit characteristics untested prior to the assembly qualification.

The network is printed, trimmed, assembled, and tested electrically. It is then run through the qualification test procedure required of the finished module. This ensures that the finished network will perform in the system as required.

NETWORK PRODUCTION

Following a successful Preproduction Qualification Test, the Network Production sequence, shown in Figure 13, can begin. An average sequence is shown for thick-film network manufacture, which may have to be adapted slightly to fit the production process of a particular manufacturing facility.

The first step in the network production sequence is to print the first layer. The first layer printed is usually a conductor layer. This layer and any subsequent layers, are printed according to the processing specification using the paste specified by the network designer.

The printing process specification must explain how to control the following printer parameters: squeegee speed; squeegee pressure; squeegee hardness; squeegee material and dimensions; screen breakaway distance; and flood bar use. The paste viscosity and room ambient conditions (temperature, humidity, venting) must also be controlled. The values of all these parameters which are recorded in the paste qualification log book must be used.

Figure 14a lists the visual inspection criteria (Inspection 9) immediately after printing. Voids in the wet paste may be touched up by addition of a small amount of

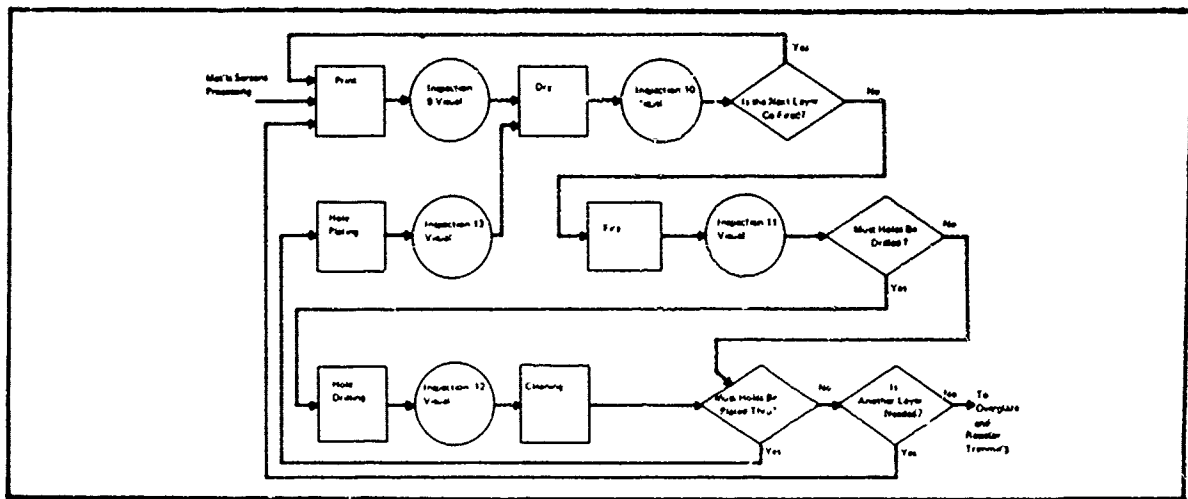


Figure 13. Network Production

paste to the exposed area. Most voids have corresponding screen clogs. Runs can not be touched up; neither can areas where a large portion of the pattern did not print. In these cases, the paste may be washed from the bare substrate or from dried layers with alcohol. Such washed substrates should be dried in air and then may be reused.

The substrates should be air dried after printing in either a belt drier or box oven. Time and temperature are the important parameters to be controlled. Drying too hot will cause sintering to begin; too cool will cause incomplete evaporation of the binder, which may cause blisters or voids during firing. Drying too fast can also cause blistering.

Figure 14b lists the visual inspection criteria (Inspection 10) for the after-drying inspection. Voids, scratches, blisters or runs should be corrected by "erasing" the layer with alcohol and starting over with the printing step. Critical dimensions should be checked and compared with those listed in the paste qualification log book. It should be remembered, however, that the final dimensions may be slightly different due to shrinkage or spreading during firing. Thickness should be measured as indicated and recorded in the production log book.

If the next layer is to be co-fired, it should be printed next. Otherwise, the substrate is fired, either in air or in a controlled atmosphere, in a belt furnace. The important parameters to be controlled include firing profile (time at temperature) and atmosphere, and the values used must be the ones listed in the paste qualification log book.

Figure 14c lists the inspection criteria (Inspection 11) for the post-firing visual inspection. The appearance inspection includes checking for blemishes, blistering, bleed out, excessive porosity, and excessive glass coverage. Critical dimensions should be within the tolerances required by the circuit specifications, and the thickness measurement should be recorded in the production log book.

If holes are required in the substrate, and are not pre-drilled in the blank substrates, they are usually drilled after the firing of the first conductor layer. Holes are generally drilled by means of diamond drill bits, a laser beam, or ultra-sonic techniques.

The drilled substrates are inspected (Inspection 12) according to the criteria of Figure 14d, using a microscope, for correct hole size and location, and for cracks around the holes or through the substrate. Failures here require changes in the drilling apparatus parameters. After drilling, substrates are cleaned to remove excess ceramic particles and diamond dust. Holes and edges are frequently plated through in order to make connection between front and back surfaces of the substrate. This operation may be

performed by hand or by use of special hole-plating screens. The plated holes are visually inspected (Inspection 13) for completeness of the plating. Several plating cycles are sometimes necessary to ensure proper plating.

After the substrates have been dried and fired for the last time, and if no more layers are needed, the networks are ready for the overglaze and resistor trimming portions of the process.

Inspection	Item	Level 1	Level 2	Level 3
a. Inspection 9 Visual	Runs, Voids, and Screen Clogs Dimensions Thickness	Visual 100% 100% of sites Voids may be touched up Conformal thickness 100% 50% Optical	Visual 100% 100% of sites Voids may be touched up Conformal thickness 100% 50% None	Visual 100% 50% of sites Voids may be touched up Conformal thickness 100% 25% None
b. Inspection 10 Visual	Voids, Scratches, Bridges, Runs, Cracks Dimensions Thickness	100% 100% of samples Conformal thickness 100% 20% 50% Performance 2%	100% 50% Conformal thickness 100% 20% 25% Dielectric 2%	100% 25% Conformal thickness 100% 25% Dielectric 1%
c. Inspection 11 Visual	Appearance Dimensions Thickness	100% 100% of samples Conformal thickness 50% Performance 2%	100% 50% 100% of samples Conformal thickness 50% Dielectric 2%	100% 100% Conformal thickness 25% Dielectric 1%
d. Inspection 12 Visual	Runs, Drying	20% 100% of runs	20% 50% of runs	10% 50% of runs
e. Inspection 13 Visual	Plating	20% 100% of runs edges	20% 50% of runs edges	10% 50% of runs edges

Figure 14. Network Production Inspection Criteria

OVERGLAZE AND RESISTOR TRIMMING

The overglaze layer and the resistor trimming cycles are not required of each and every thick-film circuit; however, in most cases one or both cycles are used. (See Figure 15).

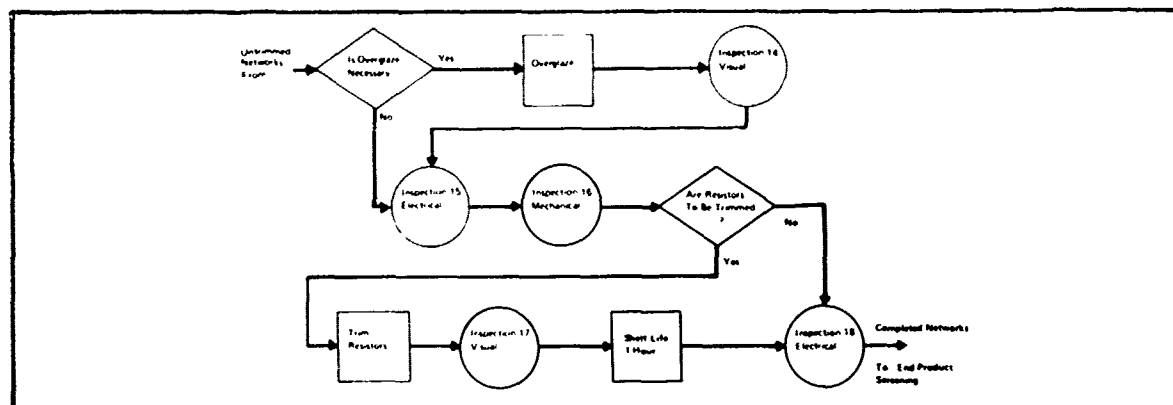


Figure 15. Overglaze and Resistor Trimming

Overglaze may be necessary, after firing the final layer, if resistors are to be abrasively trimmed. The overglaze layer protects the resistor area from overspray during trimming. Care must be taken not to allow overglaze to cover bonding pads or areas which are to be soldered.

Overglaze should be inspected (Inspection 14) according to the criteria listed in Figure 16a, for completeness and for noncontamination of bonding areas. Networks must be electrically tested (Inspection 15), according to the criteria listed in Figure 8, to determine that they are electrically useable. Conductors are tested for conductance, current carrying capability, shorts and opens. Dielectric films are tested for shorts, voltage breakdown, and dielectric constant. Resistance of thick-film resistors must be within trimmable range. In general, a failure in this area indicates that a processing parameter has changed and must be corrected.

Level 1 and Level 2 reliability levels require mechanical inspection (Inspection 16) similar to Inspection 5. The primary parameters to be measured include adhesion,

bondability, solderability, and dewetting. The Level 1 and Level 2 criteria from Figure 7 should be used. Failures here also indicate that a processing parameter has changed and should be corrected.

Resistors are trimmed by several methods. Air abrasive trimming and laser trimming are the most widely used. During abrasive trimming, care must be taken to avoid "sand-blasting" (removal of material from adjacent circuitry) of the protective layer from areas other than those being trimmed, to ground the trimming nozzle to the base plate when trimming resistors which are sensitive to static discharge, and to control ambient humidity. In laser-trimming resistors, a laser power level which is either too low or too high may cause unstable resistance due to material being left in the trim path or cracks propagating through the resistor or substrate material, respectively. The percentage of the resistor width trimmed must be controlled to prevent excessively high current density which may be beyond the power handling capability of the resistor. In addition, if more than one trim cut is used to trim a given resistor, the distance between trim paths must be at least equal to the minimum allowable width of untrimmed resistor material, as specified in Figure 16b. All trimmed resistors must be inspected (Inspection 17) to be sure that the width of untrimmed resistor is within the limits shown in Figure 16b. In addition, abrasive-trimmed substrates must be examined for evidence of "sandblasting". Laser-trimmed resistors must be examined for cracks in the substrate or resistor material, or non-vaporized material (residue) in the trim path. All examinations should be performed using a microscope, as listed in Figure 16b. If the resistor width is reduced by trimming beyond the allowable limits, the last electrical inspection in the production cycle (Inspection 15) must have its lower resistance limit raised. If "sandblasting", non-vaporized material, or cracks are noticed, trimmer parameters must be adjusted.

After a minimum of 1 hour at room ambient conditions after trimming, the electrical tests listed in Figure 16c must be performed (Inspection 18). Resistance of all resistors is measured and recorded. All resistors must be within specified tolerances. TCR will be measured, if required, on a sampling basis as listed. If resistance or TCR values are out of tolerance the trimmer parameters may need adjustment.

END-PRODUCT SCREENING

Hybrid microcircuits are generally screened using procedures outlined in MIL-STD-883. These screening procedures, however, are for completed modules or units, and are not 100% applicable to thick-film networks alone.

Thick film networks which have followed the processing and inspection procedures discussed in this report should be highly reliable (relative to the three reliability levels discussed). Additional screening and testing of the product cannot increase the reliability of the units, but can only increase the confidence of both the manufacturer and customer in the built-in reliability. Accordingly, no end-product screening is being recommended for Level 3 networks. Levels 1 and 2 networks will follow the screening procedure outlined below only as it applies to the particular functions of the specific network.

The screening procedure is basically a three-step process. First, the networks undergo a series of physical and electrical inspections. Secondly, they are subjected to some environmental stresses. And, finally, they undergo the inspections again, with any change in their parameters being noted.

The environmental stresses to be used are listed in Figure 9, along with the parameters to be checked. The allowable limits for change in parameters are listed in Figure 17. The sampling plan to be used shall follow Appendix B of MIL-M-38510A. No sample shall undergo more than one environmental stress. No item which has been environmentally stressed shall be delivered.

Inspection	High	Level 1	Level 2	Level 3
a. Inspect from 18 to 20	One point	20% 100% of substrates	70% 10% of substrates	10% 50% of substrates
b. Inspect from 12 to 14	Watch of Res is normal	Collected resistor 30% + 10% under 100% of resistor + 15% under maximum resistor resistor material	Collected resistor 70% + 70% under 50% of resistor + 15% under maximum resistor resistor material	Collected resistor 10% + 80% under 70% of resistor + 15% under maximum resistor resistor material
c. Inspect from 16 to 18	Sampling Res Material 100%	20% 10% of substrates 20% 50% of test paths 20% 20% of resistors	70% 70% of substrates 70% 20% of test paths 70% 70% of resistors	10% 10% of substrates 10% 10% of test paths 10% 10% of resistors
	Resistor TCR	All Resistor Sample of 2% of substrates	All Resistor Sample of 2% of substrates	All Resistor Sample of 1% of substrates

TA 20

Figure 16. Resistor Trimming Inspection Criteria

Inspection	High	Level 2
a. Inspect from 18 to 20	One point	20% 100% of substrates
b. Inspect from 12 to 14	Watch of Res is normal	Collected resistor 30% + 10% under 100% of resistor + 15% under maximum resistor resistor material
c. Inspect from 16 to 18	Sampling Res Material 100%	20% 10% of substrates 20% 50% of test paths 20% 20% of resistors
	Resistor TCR	All Resistor Sample of 2% of substrates

TA 20

Figure 17. End Product Screening Inspection Criteria

CONCLUSION

The in-process quality control plan discussed above has been developed using the best test methods, controls, and inspection criteria which were available at the time. Some of these methods and criteria, namely tests on solder leaching⁴ and resistor drift⁵, were determined under the same contract which supported development of the quality control plan. The plan is not complete, however, since there are still areas where not enough information is known to adequately define and control the thick-film process.

Work under a second contract with the U.S. Army Electronics Command, Contract DAAB07-75-C-1331, is addressing several of these yet untouched areas: power rating of thick-film resistor materials; effects of furnace profile change on thick-film materials; development of a test plan to determine acceleration factors for thick-film materials; and effects of geometry on resistor stability. In addition, work still needs to be done in the areas of: actually determining the acceleration factors; determining derating curves for power dissipation; importance of viscosity control; measurement of wet print thickness; and reliability and process control for thick-film material systems using non-noble metals.

The quality assurance plan presented here, then, is only the beginning, and more should be added to it as the thick-film technology continues to grow.

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4. Ibid, pp. 98-125 and 191-227.
5. Ibid, pp. 125-144 and 229-277.

THE EFFECTIVE USE OF LOOSE PARTICLE DETECTORS

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INTRODUCTION

Since the advent of the first commercial acoustic type loose particle detectors in 1971 the subject of loose particle detection has received much attention. One reason for this is the simplicity of the acoustical type testers. Devices can be tested at the rate of one per minute with relatively inexpensive equipment, while X-ray or monitored vibration testing are more costly in both time and equipment required. In addition X-ray detection is limited to dense materials and monitored vibration limited to conductive particles.

The problems caused by loose particles in semiconductor devices has been documented in the literature ^{1,2}. Solder ball and gold flake problems were covered extensively in the press and trade journals over 10 years ago; but, unfortunately the problems are still with us. Figure 1 shows a recent field failure caused by a loose solder ball that shorted between a heat sink and the case of a T0-3 can.

Studies run at Singer on over 4000 hybrids show that if no special attention is directed at eliminating loose particles, about 15% of the product will contain loose particles. Over half of these hybrids contain conductive particles large enough to short out some area within the hybrids. It is not surprising then that loose particle failures occur, the surprising thing is that failures caused by loose particles are not a bigger problem.

DESCRIPTION OF TEST

Figure 2 shows the acoustic type equipment used for PIND (Particle Impact Noise Detection) testing. It consists of four major components:

1. A small electromechanical shaker with a piezoelectric transducer mounted on the vibrating platform.
2. Control electronics to allow the shaker to operate over a range of frequencies and amplitudes.
3. Detector electronics that take the output of the transducer and convert it to an audio output through a speaker.
4. An oscilloscope to display the output of the detector electronics package in a visual manner.

The hybrid is mounted on the transducer and then vibrated to excite any loose particles that may have been sealed in the device. In order to improve the efficiency of the test, the device being tested is usually subjected to mechanical shock by tapping the hybrid on several sides. This is done to loosen any particles which may have become trapped for one reason or another. The moving particle generates noise which is detected by the transducer, amplified by the electronics and displayed visually on an oscilloscope and audibly through a speaker.

PROPOSED MILITARY TEST METHOD

A proposed method (2020 of Mil-Std-883) for loose particle detection is now out for review and comment by industry. This document describes the apparatus, procedure and criteria for failure. Appendix A contains the proposed draft.

The proposed test method is basically sound and should be updated, approved and released as soon as possible. The following changes are recommended for inclusion in the update.

1. The tip material of the proposed shock tool should be specified so that it is hard enough to generate sufficient impact to dislodge trapped particles but not hard enough to damage the case material of the device being tested. Actually much of the industry now uses an 1/4" diameter nylon rod about 6" long.
2. The use of double face tape to hold down the device should be avoided if no limit is placed on the number of parts tested before new tape is used.
3. The addition of a bake cycle just before each test or retest should be instituted to disperse electrostatic charges. This will be discussed in more detail later in a section on special techniques.
4. Either mounting attitude (cover up or cover down) should be specified, or a statement added that the device can be mounted in any attitude.
5. If more than 15% of the parts fail, then the loose particle in the failed devices should be recovered and analyzed so that a sensible decision can be made on the rest of the lot. For example, if small gold flakes are found, the rest of the lot would also be suspect.

Another item that must be considered when evaluating the effectiveness of PIND testing is the conflict with pre-cap visual requirements. It is generally conceded that the PIND test limit of particle detection is in the one to three mil area. A quick review of the present version of Mil-Std-883, Class B pre-cap visual inspection revealed some startling facts. There are 16 paragraphs that allow spacing of less than 3 mils (5 in the present 2010.2 and 11 in 2017) between adjacent conducting paths. Twelve of these allow spacings of .3 mil or less. Only one paragraph out of the 16 involves an item that would be aided by chip glassivation. Unless the loopholes for close spacing (1 mil or less) are eliminated, the effectiveness of PIND testing will be diminished. There are two other paragraphs in 2010.2 that bear on the particle problems. The first is paragraph 3.2.3C which allows cracks of under 5 mils if they are not heading toward an active area. This defines a crack which could easily generate a large silicon chip. This paragraph should be amended if particle free parts are required. The other paragraph bearing directly on the loose particle problem is paragraph 3(g) 4. This defines an attached particle as one that cannot be dislodged by a 20psig air blast. We have attempted to dislodge known loose particles with greater than 20psig and have found some particles which would not break loose. In every case a "sticky-pick" (stick with scotch tape wrapped around it) easily removed the loose particle. This general area of loose particle removal needs investigation. For example, if the particles are being held by static electricity, would a liquid work better than the airblast, or would a high temperature soak prior to the airblast be beneficial in reducing the electrostatic attraction?

PARTICLE RECOVERY AND ANALYSIS

In order to investigate the loose particle problem in detail a simple method was developed to extract, measure and chemically analyze the loose particles. The covers of hybrids that fail the PIND test are pierced with a polished stainless steel awl. This results in a hole about 25 mils in diameter as shown in Figure 3. The hole is covered with a clean piece of scotch tape and the hybrid returned to the PIND tester. The test is run in 30 second intervals until the hybrid no longer exhibits an indication of loose particles. Fresh tape is put over the hole after each 30 second run. The tape over the hole is cut (as can be seen in Figure 3) and then carefully peeled off using tweezers.

The tape with the trapped particles is placed on double faced tape that is mounted to a SEM (Scanning Electron Microscope) specimen stub. Figure 4 shows the tape with some particle attached. The SEM specimen stub must be coated with a thin film of evaporated carbon. This prevents charging of the tape when placed in the SEM and still allows elemental X-ray analysis using energy dispersive techniques. Figure 5, 6, 7, 8 and 9 show some of the types of material removed from hybrids.

All PIND test failures to date that have been subjected to the removal technique described above, have yielded particles, 1 mil or greater in size. As a further check of both the PIND test and our ability to remove particles, five modules that had passed the PIND test were subjected to the standard process of part removal and evaluation. In no case was there a particle found that was greater than 1 mil, in fact three of the hybrids were found to be completely free of loose particles. Having developed confidence in the PIND test and our ability to remove the loose particles a method of improving the yield of particle free hybrids was undertaken. To get a better feel for the particle shapes and sizes, SEM photographs were taken of all of the particles removed. In using the photographs to make measurements, consideration must be given to the fact that for particle analyses the tilt angle of the specimen in the SEM was established at 60° . With a 60° tilt the vertical dimensions on the photograph must be multiplied by 2.

The particles were analyzed using EDAX (Energy Dispersive Analysis of X-rays). This equipment allows qualitative elemental analysis of all elements with atomic numbers of 11 (sodium) or greater. The details of energy dispersive X-ray analysis can be found in a publication coordinated by Russ³. For this discussion it is only necessary to understand the output of the equipment. A spectrum is presented for viewing, using a video display. The energies at which peaks occur in the spectrum are readily identified with the elements that produced the X-rays. This then gives an elemental analysis of the particle being investigated. Figure 10 shows a photograph of the display tube after an analysis of a loose particle of gold-silicon eutectic. The spectrum shows two major peaks around 2,000 (electron volts) and two lesser peaks above 8000 ev, the major peak to the left and the two lesser peaks are all indicative of gold. The other major peak confirms the presence of silicon.

The EDAX equipment allows an expanded look of any segment of the spectrum. This allows isolation of a peak down to a 20 ev (electron volt) channel. Figure 11 shows an expanded view of the lower range of the X-ray analysis shown in Figure 10. Figure 12 shows an analysis of 1% silicon gold lead wire. Note: the silicon peak is still present but at a much lower level than the gold-silicon eutectic of Figure 10.

Figure 13 shows the analysis of a particle of teflon. The EDAX has two memories so that two specimens can be analyzed and compared. The dots indicate the peaks of the information stored in Memory B while the solid area (actually closely spaced bars) indicate the information stored in Memory A. In the case of the analyses shown in Figure 13 both memories contain the same information showing that there is no significant difference between the analysis stored in Memory A and that stored in Memory B. Memory A contained information on the teflon particles and Memory B contained information on the area next to the particle or, in effect, the surrounding background noise. From this it can be concluded that no elements heavier than neon (atomic number 10) are present in the particle.

The combination of SEM and EDAX in one piece of equipment results in a powerful tool for analyzing loose particles.

CASE HISTORIES

Several of the lots having over 50% of the hybrids containing loose particles were analyzed. When the analyses were completed the individual vendors were contacted to see if the source of the particles could be determined. This investigation resulted in uncovering the following process related problems:

1. Laser cutting of the substrates produced nodules of fused alumina that broke loose during thermal cycling.
2. Fiberglass bristles from a brush used to apply protective coating to a power hybrid were discovered.
3. A wire bonding capillary was found to have chlorine contamination.
4. Teflon fibers from a cleaning solvent tank were introduced into hybrids because a millipore filter was left out of the system.
5. Properly cleaned packages were contaminated by placing them in dirty containers after the final cleaning operation.
6. Excessive scrubbing when attaching semiconductor die produced gold-silicon eutectic flakes.
7. Hybrids held upside down on a shaker head to remove particles actually were found to have an increased loose particle count. A magnetic chuck that attracted small charged particles was used to hold the hybrids.
8. Solder balls were found that had been formed during the package sealing operation.

The dramatic effect of correcting a process can be shown by a case history. The PIND rejects on a hybrid had suddenly risen to over 40% on eight successive lots. The line was stopped until the problem could be resolved. Particles from several hybrids of the eight lots were removed and analyzed. This resulted in uncovering the offending process. Figure 14 shows the change in PIND rejects before and after the corrective action.

REPAIR OF PIND REJECTS

The question arose as to the deposition of hybrids that were acceptable in every respect except for loose particles. A delidding operation to remove the particles would entail a complete recycling of the part through all of the screening tests required of a new hybrid (from pre-cap through burn-in). A method of repair was developed where only a minimum amount of retesting would be required. The basic method involves the removal of particles by the method described above while the parts are in a moisture controlled dry nitrogen atmosphere. After the particles have been removed the hole is sealed with a small solder preform. Since the entire operation is performed in the same atmosphere as is the hybrid, and since the part

does not see any environments in excess of that for which it was designed. The only testing required would be a hermeticity test to check the solder sealing of the hole. Appendix B outlines the step by step procedure for repairing PIND test failures.

PROBLEMS AND SPECIAL TECHNIQUES

Because the EDAX system does not detect elements below sodium, the analysis of aluminum (from wire bond chip metalizations) and alumina (substrate material) will both look alike on the X-ray display monitor. Therefore other techniques must be employed to determine the differences. Both the optical microscope and the SEM pictures are useful in making the determination. McCrone and Dilly⁴ have published a four volume work which is also useful in analyzing small particles.

The key to good results using the PIND tester is in training the operator. By giving the operator feedback from the particle analysis, confidence is rapidly developed in the operator and the special techniques necessary for reproducible testing.

A useful technique that has been developed is the baking of hybrids for one half hour at 85°C just prior to testing, retesting or particle removal. This disperses the electrostatic charges that tend to hold the small particles in place. Several parts known to have loose particles in them suddenly no longer failed when PIND tested. After a bake cycle the hybrids again were rejected by the PIND test. Another example of the usefulness of the bake step was discovered during early attempts to repair PIND rejects using the method described previously. Before the bake step prior to particle removal was instituted, about 10% of the repaired parts failed PIND test again. After the bake cycle was instituted almost no repaired parts failed the PIND test. Baking hybrids has also been useful in resolving differences in PIND test results at two different locations. The drier location always had fewer PIND failures.

Care must be taken when punching the hole in the lid of a hybrids so that the particles can be removed. Both the shape of the tool and the location of the hole are important. The location is determined by looking at the layout of the hybrid and finding a location where there are no high parts or bonding wires. The cover should be thinned to between three and five mils in the area where the hole is to be punched. The tool for punching the hole must be controlled. It must be inspected periodically to assure that the tip has not been dulled by previous use. The hole can be inspected using a microscope having vertical illumination. This method can also be used to ascertain if any damage has been caused by excessive punch penetration.

When analyzing the particles captured on tape a minor problem arose. When the tape was exposed to the SEM environment it would shrink and cause the carbon coating to crack. This resulted in isolated islands that would charge up and make the particle analysis difficult. Figure 15 shows a sample of the charging effects caused by the drying out of the tape. One way to eliminate shrinking after carbon coating is to bake out the tape just prior to coating.

CONCLUSIONS

PIND testing is a cost effective method of improving hybrid reliability. It can be used to screen out a large portion of the potential particle failures. The greatest value of PIND testing however, results from isolating and analyzing the loose particles. This procedure has a twofold beneficial effect. First, confidence and proficiency is gained by verifying the results of PIND testing. Second, and more important, is the reliability improvement possible by finding and eliminating the source of the particle contamination.

ACKNOWLEDGEMENT

Acknowledgement is due to Wilson Reilly and Gladys Courter for valuable suggestions and performing the thousands of tests necessary for the success of this program.

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4. W.C.McCrone and J.G.Delly "The Particle Atlas-Edtion Two" Ann Arbor: Ann Arbor Science Publishers, Inc.



Figure 1. Loose Particles
Induced Field Failure

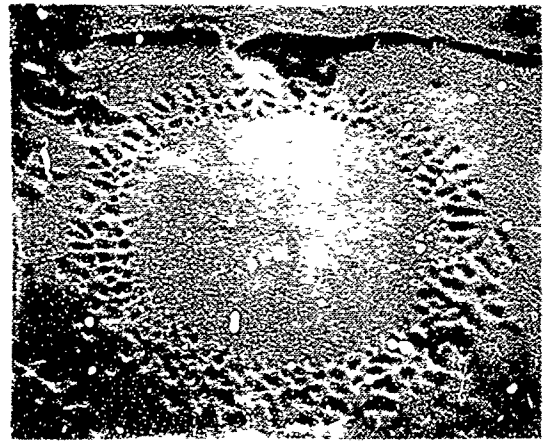


Figure 4. Tape With Captured
Particle Attached

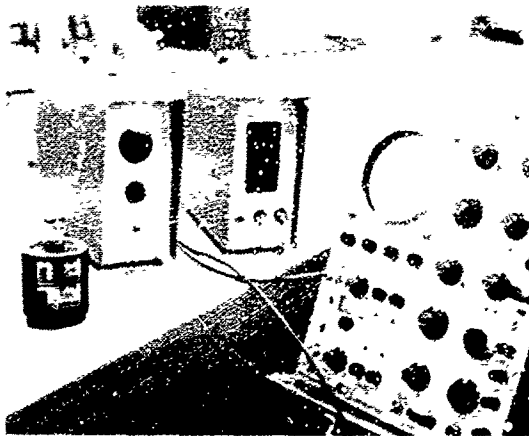


Figure 2. Loose Particle
Test Equipment

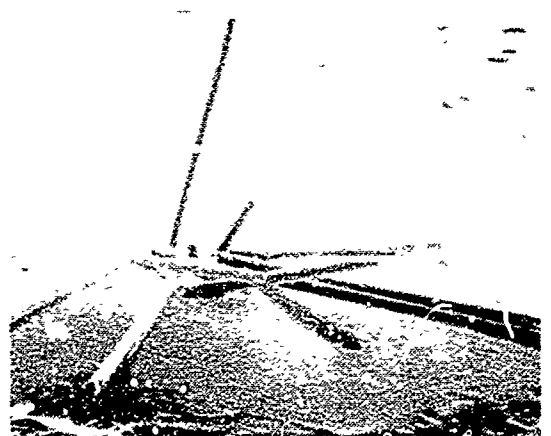


Figure 5. Fiberglass Bristles
Removed From Hybrid

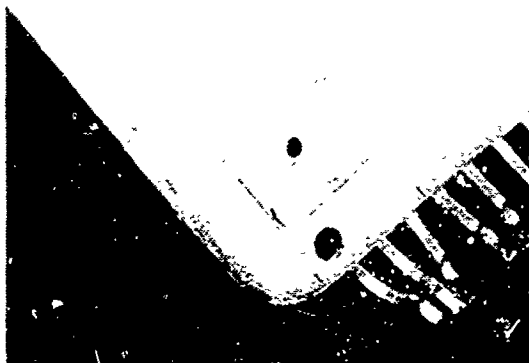


Figure 3. Hole Punched In
Cover For Loose Particle
Removal



Figure 6. Alumina Particles
Caused by Laser Scribing



Figure 7. Table Salt Crystal

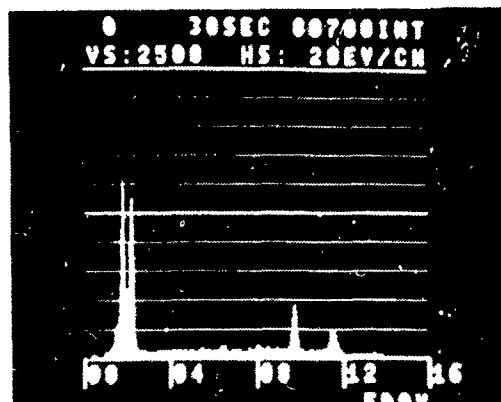


Figure 10. Dispersive X-Ray Analysis of Gold Silicon Eutectic



Figure 8. 90 Mil Long Gold Silicon Eutectic

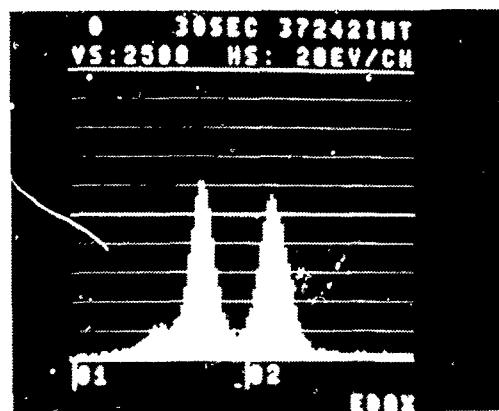


Figure 11. Expanded Lower End of Figure 10

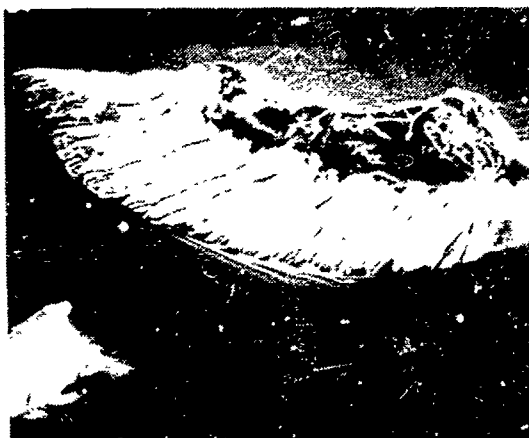


Figure 9. Gold/Kovar

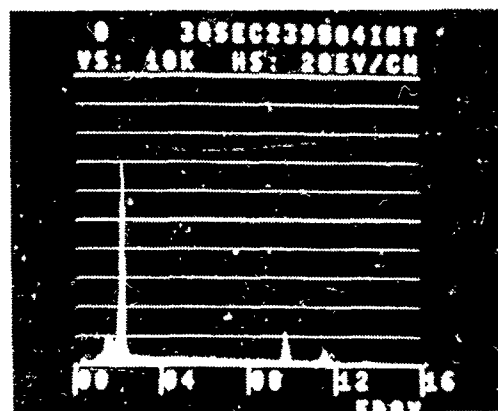


Figure 12. X-Ray Analysis of Gold Bonding Wire

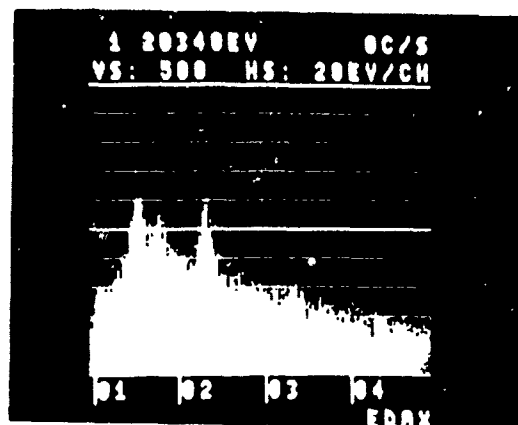


Figure 13. X-Ray Analysis of Teflon

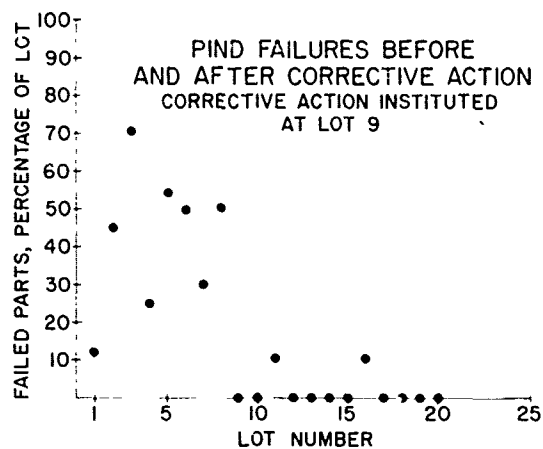


Figure 14. Effect of Particle Analysis on Yield



Figure 15. Result of Not Pre-Baking Tape Before Carbon Coating

APPENDIX A

DRAFT OF PROPOSED TEST METHOD 2020/20XX OF MIL-STD-883

PARTICLE IMPACT ACOUSTICAL NOISE TEST

1. **PURPOSE:** The purpose of this test is to detect loose particles or component parts inside the cavity of microelectronic and semiconductor devices. It provides a non destructive means of detecting those devices containing particles which have a sufficient effective mass upon impact with the case to excite the transducer. The practical limit of the test is particles of 0.4 microgram effective mass or greater, although smaller particles may be detected under certain conditions.
2. **APPARATUS:** The apparatus required for the particle impact noise test shall consist of the following:
 - 2.1 A vibrator capable of providing the specified G force at the specified frequency. The vibrator should be a small, low force-pound rated type with very low inherent noise. Armature rub, oscillator or amplifier noise can create noise levels which obscure noise bursts caused by particle movement.
 - 2.2 A noise detection system of sufficient capability (see typical noise values) consisting of a piezoelectric transducer (Dunegan Model S-140B or equivalent), an amplifier-filter (Dunegan Model LPD or equivalent), an oscilloscope, and headphones (a soundproof enclosure may be used instead of headphones).
 - 2.3 A shock tool capable of imparting shock pulses of the specified G level to the device under test. (A number 820 Densco Condensaire dental amalgam condenser or equivalent).
 - 2.4 Attachment medium to secure the devices firmly to the transducer. (Permicer P 50 double face tape, Dow Corning C-2-0982 bouncing putty or Dunegan AC-WS Couplant and Automation Industries, Inc., Heavy Viscosity Water Soluble Multipurpose Ultrasonic Couplant # 50A9084, are suitable for this purpose).
3. **PROCEDURE:** During use, the noise detection system operation shall be verified at least once each working shift by mounting a device, which contains a spherical particle of known mass (between 1.4 and 11 micrograms) on the transducer and observing the noise output while vibrating at the specified conditions. The device shall be of the same or similar case type as those being tested. In addition, the system may also be verified using a particle free device to demonstrate the absence of false signals. Typical noise values range from about 50 to 300 (peak to peak) millivolts per microgram of particle weight depending upon the device case.

The device to be tested shall be subjected to three (3) preconditioning shocks of $200 \pm 100G$ peak using the shock tool described in 2.3 in the Y_1 or Y_2 axis prior to mounting for test to assure that any potential internal particles are unrestrained. Immediately after these three shocks, the device shall be mounted directly to the transducer using materials which conform to the case irregularities (clamps should be avoided since they provide a possible source of false signals). The transducer and device shall be vibrated along the X or Z axis with a vibration force of $8 \pm 2G$ peak at a frequency of 60 ± 5 hertz. While the device is being vibrated and within a time period of five (5) seconds maximum the impact shock tool of 2.3 shall be used to apply a minimum of three (3) shock blows to the device case in the same manner as specified for the preconditioning shock blows.

During the five (5) second period and a three (3) second period immediately following the last shock blow and while the device is still being vibrated, audio and oscilloscope monitoring for noise bursts caused by loose particles impacting the device case shall be conducted.

- 3.1 Failure Criteria: Any noise burst exclusive of background noise except those caused by the shock blows during the monitoring periods shall be cause for rejection of the device.
- 3.2 Reference Condition: In the event of doubt of interpretation of noise bursts resulting in a device being classified as a failure, the test shall be repeated five times on the questionable device. If no additional noise bursts occur during the additional test periods, the device shall be considered acceptable.
4. SUMMARY: The following details shall be specified in the applicable procurement document:
- (a) Test conditions (see 3) if other than specified.

APPENDIX B

Repair Procedure for PIND Test Failures

1. Using hybrid layout locate the best location to punch hole(preferably not diagonally opposite the dot indicating Pin 1).
2. Determine thickness of cover and mill a 60 mil blind hole where the lid is to be punctured. This operation should leave 3 to 5 mils of cover thickness. Thoroughly clean the hybrids.
3. Load a dry box (20ppm max.water content with the following equipment:
 - a.hole puncher
 - b.PIND test shaker
 - c.tool to tap hybrids on shaker
 - d.adhesive to attach hybrid to shaker
 - e.solder preforms
 - f.soldering iron
 - g.tape to capture particles
 - h.cleaned hybrids with blind holes
 - i.hot plate
4. Heat hybrid on a hot plate for a minimum of 30 minutes at 85°C.Remove and cool to room temperature.
- 5.Punch hole in hybrid (20 to 30 mil diameter) in the 60 mil blind hole
- 6.Place tape over hole
- 7.Mount hybrid on shaker,tape side up, with water soluble adhesive
- 8.Carry out standard PIND test until all particles have been removed. Note: In some cases it may be necessary to replace tape and test a second time. One reason for this is the tape gets so loaded with particles no more can stick
- 9.Return hybrid to hot plate for 5 minutes
- 10.Insert solder preform in hole
- 11.Quickly seal hole with a hot soldering iron
- 12.Retest part to see that all particles have been removed
- 13.Remove hybrids from dry box and clean off water soluble adhesive
- 14.Run hybrids through appropriate screening tests

APPLICATION OF TAPE CHIP CARRIER TECHNOLOGY TO HYBRID MICROCIRCUITS

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INTRODUCTION

Several previous papers^{1,2} have been published which discuss the Tape Chip Carrier (TCC) or Tape Automated Bonding (TAB) technology which is now moving into commercial production. In this paper, the authors intend to review the TAB technology and describe progress towards its adaption to high production programs for hybrid microcircuits. Approximately ten years ago the tape concept for handling and bonding integrated circuits (ICs) was introduced by General Electric with the Minimod process. This process has evolved into the present technology used for IC packaging^{3,4} and hybrid fabrication. Progress has been such that TAB bonders are now available from several vendors which enable IC manufacturers to handle and bond devices at the rate of several thousand per hour.

Figure 1 shows a pictorial presentation of the essential assembly steps for the fabrication of hybrids with the tape technique. The major steps in the process are listed below.

- | | |
|-------------------------------|-----------------------------|
| 1. Wafer Metallization | 5. Inner Lead Bonding (ILB) |
| 2. Substrate Manufacturing | 6. Outer Lead Bonding (OLB) |
| 3. Tape/Carrier Manufacturing | 7. Die Testing |
| 4. Die Separation | 8. Rework |

During the course of this paper these topic areas will be explained.

The technology described herein can be highly automated and readily adaptable to process control.

1. Wafer Metallization at Chip Connection Pads (Bumping)

A major advantage of the Tape Automated Bonding technology which is not shared with beam lead technology becomes apparent when viewed from the standpoint of availability. With only minor exceptions, IC wafers of any type, from any vendor, are compatible with the TAB process. The following paragraphs describe the procedure for metallizing IC wafers so that they may be used in

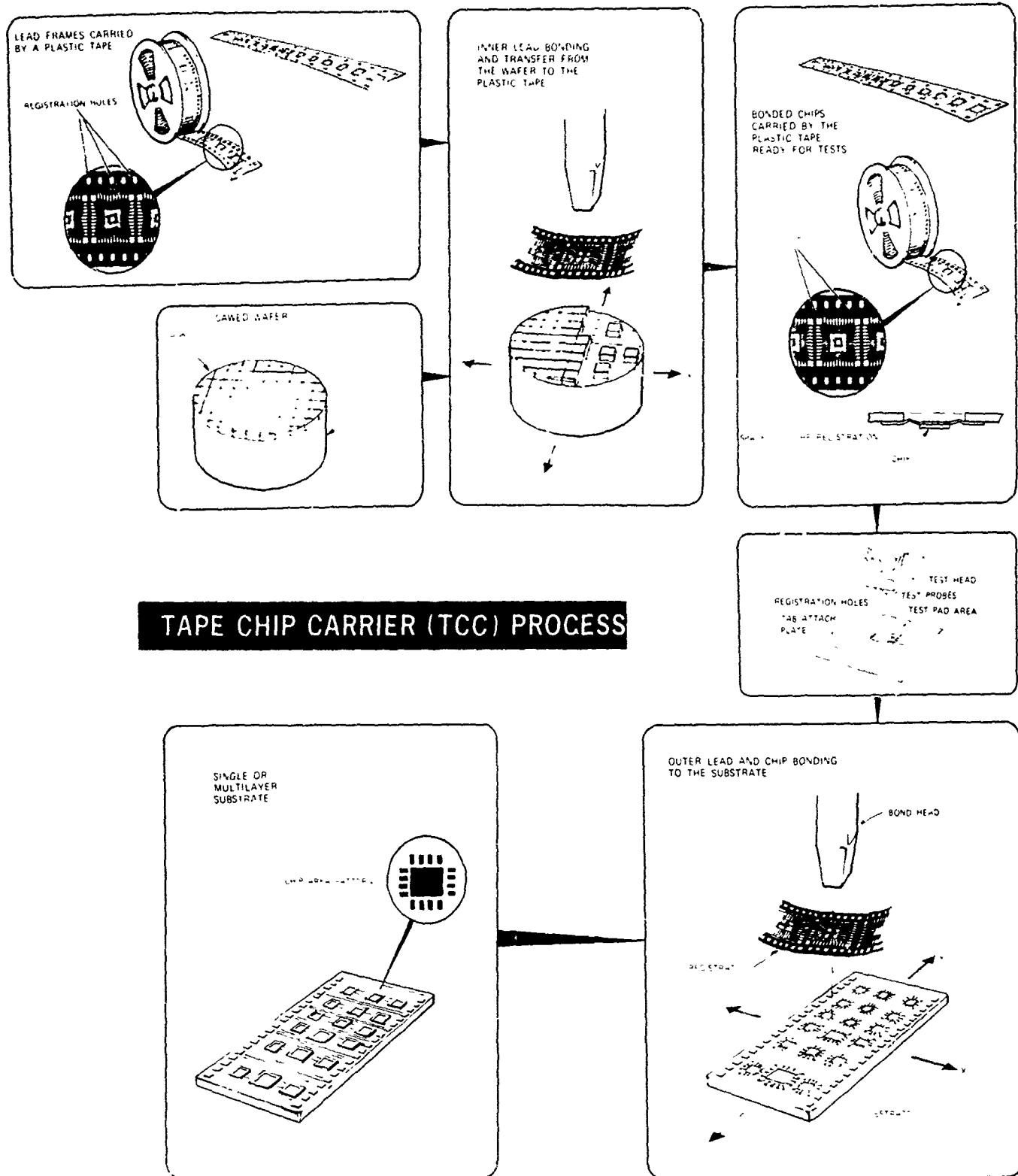


FIGURE 1. TAPE AUTOMATED BONDING PROCESS

conjunction with TAB. This process is known as "bumping" and the purpose of the bumps is to provide interconnection metallization between the lead frame on tape and the integrated circuit bonding pads.

Illustrated in Figure 2 is a typical metallization procedure for gold bump fabrication. Figure 2 depicts a wafer as it arrives from the vendor. Solvent cleaning (if necessary) and mild etching may be used to remove the first few monolayers of metallization in order to reduce contamination and increase adhesion.

The next step consists of depositing two or three thin layers of appropriate metals over the entire wafer. The purpose of these layers is to provide good adhesion to both the aluminum pad and to the passivation layer. But the work function (ϕ_w) of the first layer must closely match that of the aluminum bonding pad. This is essential if the junction formed is to be an Ohmic rather than a Schottky barrier. These metallization layers must furthermore act as diffusion barriers to prevent the formation of intermetallics which could cause a bump to lift off at a later time. Presently, shear strength tests on gold bumps are in the range of 60-100 grams. In addition, it should be mentioned that the main advantage of this metallization scheme is its high resistance to corrosion, and storage stability at moderately high temperatures (for example, 350°C). At this point, a thin layer of gold is deposited over the wafer. This is necessary to eliminate contamination of the contact/barrier layers when the wafers are handled.

In preparation for building up the gold bumps by electroplating, photoresist is applied. This may be done by the standard technique of spinning a liquid photoresist or laminating solid photoresist films onto the wafer, drying, exposing, and developing.

Upon developing the photoresist, the wafers are electroplated with gold to a bump height, generally greater than 0.5 mils. After stripping away the photoresist, the layer of gold is removed with a suitable gold etchant. Note that the etchant will also remove an equivalent amount of gold from the bump. Then the wafer may be placed into other etchants to remove the contact/barrier layers. Figure 3 shows a typical finished gold bump.

A parameter extremely critical to this process is contact resistance of the bumps. Measurements have been made using a four-point probe to determine the contact resistance of the gold bumps on IC wafers. The results indicated resistance in the milliohm range.

Bumps usually consist of a ductile material (gold or copper) to allow for slight deformations in the bumps during bonding. By using a material which has this property, variations in bump height will not reduce the effectiveness of the bonding device. As an example, consider thermocompression as the mechanism for

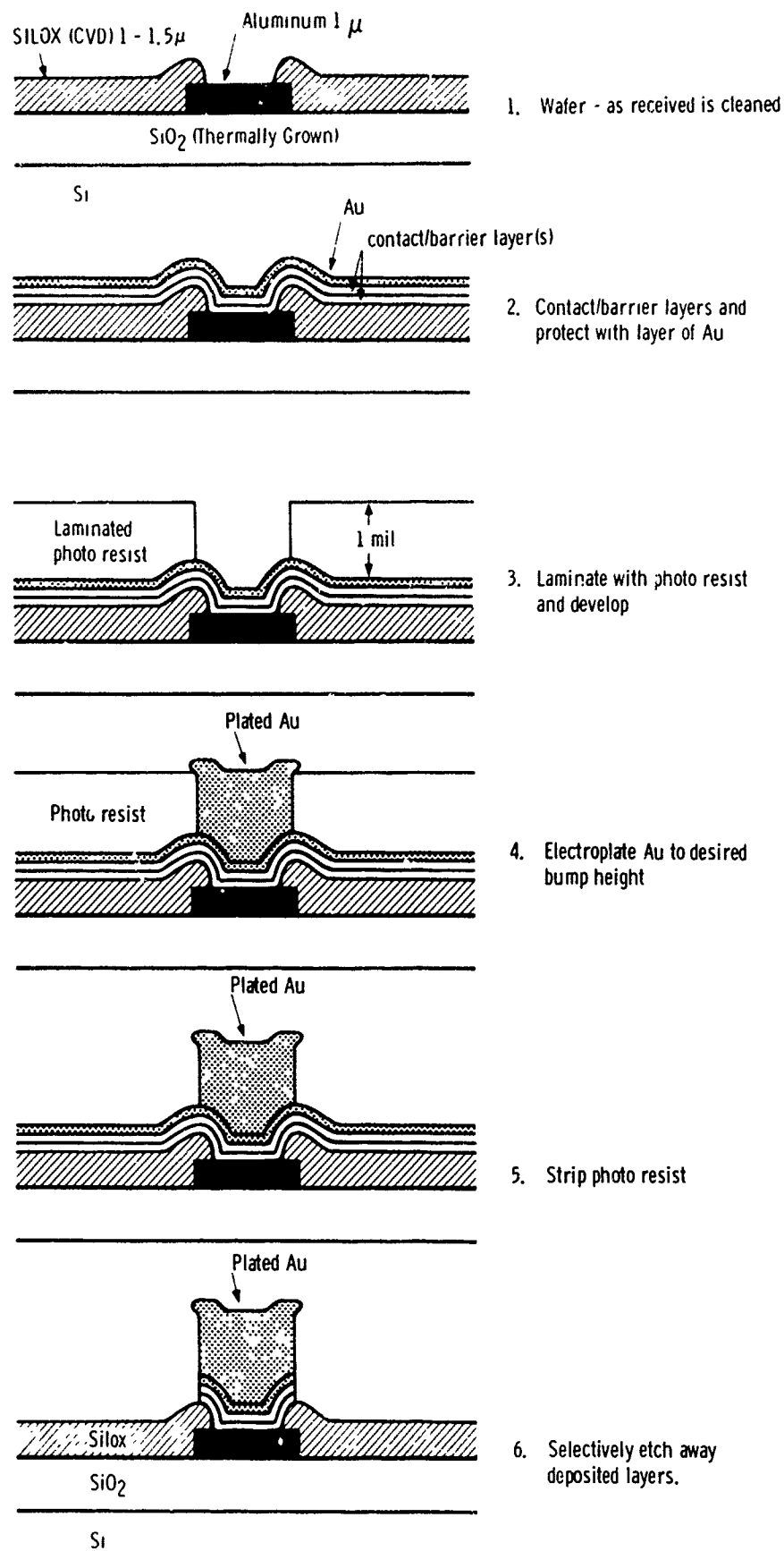


FIGURE 2. METALLIZATION PROCESS FOR BUMPING WAFERS

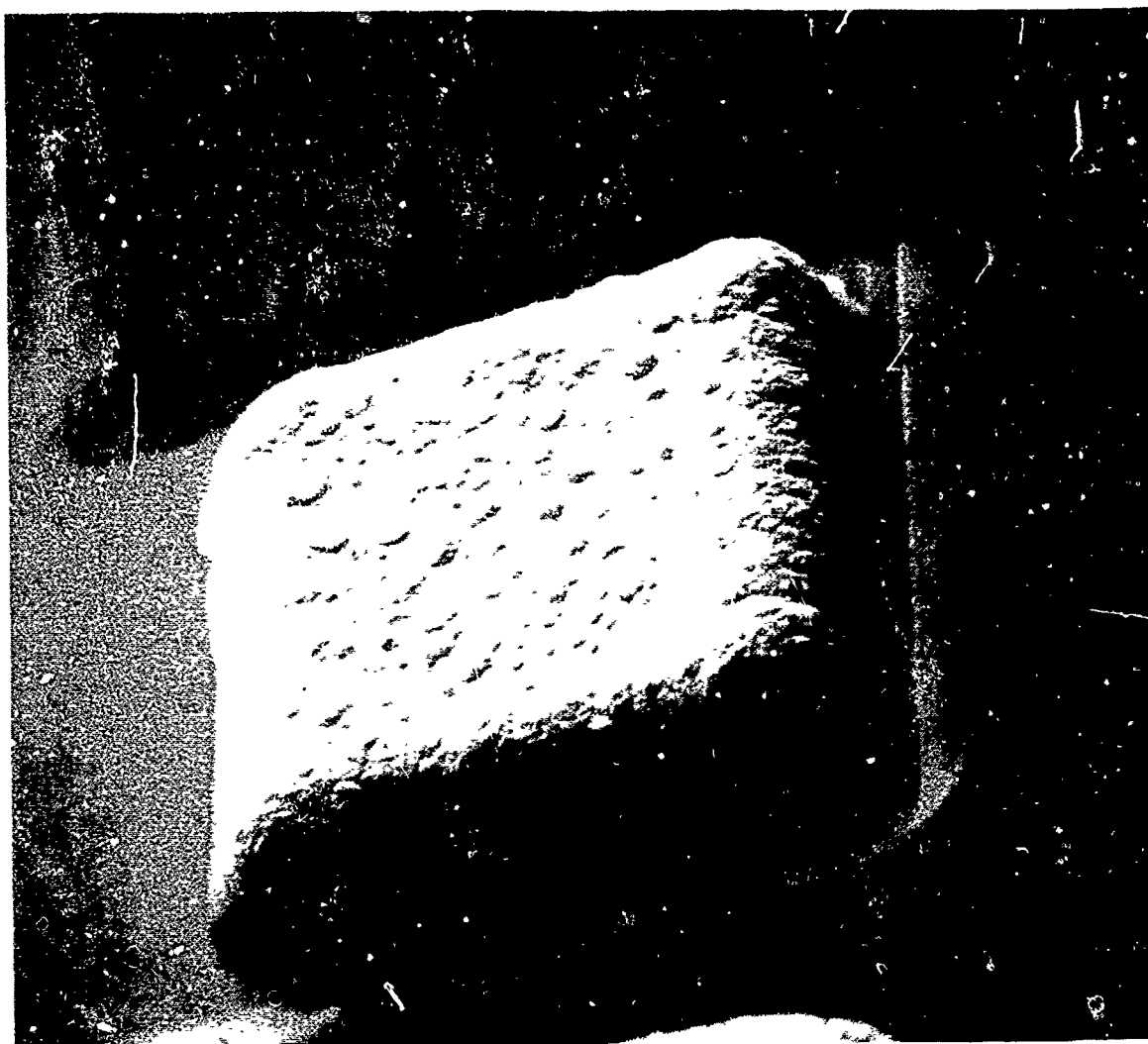


FIGURE 3. SEM PHOTO OF AN ELECTROPLATED GOLD BUMP

inner lead bonding. During the bonding process, taller bumps will be somewhat deformed (in addition to the deformation of lead frame tips) to the level of the short bumps. Another advantage to using gold as the bump material is that soldering (using an Au-Sn eutectic) can be an alternate method to thermocompression as an inner lead bonding mechanism.

2. Substrate Manufacturing

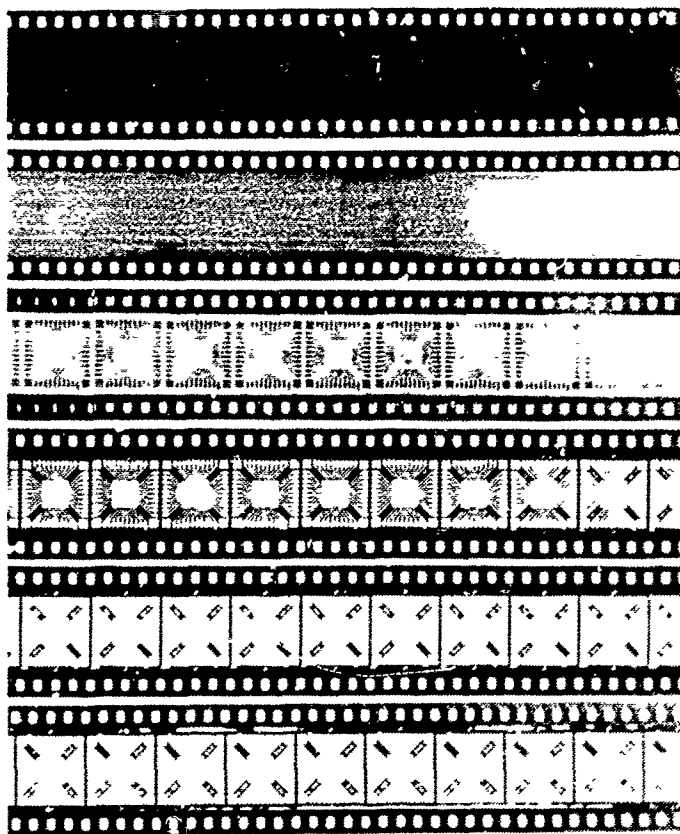
Significant increases in the demand for hybrid microcircuits has advanced the use of thick and thin films on ceramics in hybrid fabrication. Several reasons are responsible for the popularity of these films: quick turnaround, ease of fabrication, low cost, ruggedness and high reliability. By utilizing conventional film technology, interconnections for resistors, capacitors, discrete passive components, and TAB semiconductor devices can be provided. Consideration for the materials selected must include compatibility with solder mounting or thermocompression bonding of the outer lead bonds and the attachment method for the back of the chip. Critical parameters for the interconnect materials are resistance, intermetallic properties, diffusion rates, and the ability to withstand compressional forces without cracking. Inks supplied by du Pont, EMCA, etc. for thick film applications are available and have satisfactory performance characteristics.

3. Tape/Carrier Manufacturing

This section will review the various aspects of the technology as it relates to carriers and methods for obtaining the required lead and carrier patterns. A representative plastic carrier and metallurgical approach is shown in Figure 4. This figure illustrates one of the fabrication sequences used at Honeywell.

Tape width shown is 35 mm. Dimensional tolerances of the sprocket holes are critical to the successful implementation of the automatic inner lead bonding and pattern definition processes. A tight tolerance in the 15 μ m range between reference sprocket holes must be met.¹ The defining of the lead patterns is accomplished by precision exposure equipment.

There are two different methods available for producing patterns in the carrier and the carrier metallization. The first involves applying photoresist on a composite of carrier and carrier metallization. Composites of this type are formed by casting liquid polyimides onto copper foils and then curing the polyimide at high temperature. After photoresist has been applied and baked, it is exposed to interconnect and window/sprocket patterns. Development of the photoresist protects certain land areas and opens others to attack by selective etchants. Final pattern definition is then obtained by spray etching techniques. This method works especially well with thin composites.



--1.2 MIL Copper Foil

--Kapton Film Carrier

--Top View of copper foil laminated to Kapton Film Carrier (35mm).
Not shown is the prepunch die placement opening that is on tape.

--Photoresist pattern which defines leads and test pads.

--Etched Lead Frame Pattern

--Tin Plated Lead Frame

--Chips Mounted to Carrier

FIGURE 4. A REPRESENTATIVE PLASTIC CARRIER AND METALLIZATION

The other method for patterning the tape is essentially as shown in Figure 4. In this process a prepunched film carrier is laminated to a foil. Next, the interconnect pattern is produced by applying photoresist, exposing the photoresist to a metallization pattern, developing the photoresist and then spray etching for forming the metal leads. This technique has been sufficiently defined so that reel-to-reel processing is now possible.

The plastic carrier material selected must have suitable dimensional stability and the capability to withstand short term thermal excursions necessary for soldering and thermocompression bonding. One material which is known to satisfy this description is polyimide. The most common format for this tape is 35 mm. It is also available in 8, 16, and 70 mm sizes. Alternate materials that are now being considered to replace polyimide are polyester and Exxon's PBA (polyparabanic acid) film. Prime motivation for the development of the alternate materials is that the present costs for polyimide are relatively high. The ability of these alternate materials to withstand the temperature excursions and handling in the hybrid configuration is still being demonstrated. Manufacturers involved in carrier materials and formats are IMI, 3M, AMP, Honeywell and du Pont. Conventional thicknesses for the polyimide carriers are 0.5, 1, 2, 3, and 5 mil.

Copper is used universally as tape metallization because the lamination processes for copper to plastic carriers have been known for several years, it is readily etched and has good electrical conductivity. This combination of material is identical to that involved in flex cable circuitry.

Two types of copper are available-- electro deposited and rolled-annealed. The copper is classified as 1/2, 1 or 2 ounce with the 1 ounce being the most common. According to C. Burns of National Semiconductor, the use of rolled, annealed, copper foil is preferred because it has greater ductibility. This reduces the possibility of microfracture-formation when the inner lead bond is made and the leads are formed in preparation for outer lead bonding. Another advantage of the rolled annealed material is that it has a more uniform surface for plating of metals such as gold and tin. Also in pattern generation, which involves etching; the more uniform surface produces cleaner lines since preferential etching along grain boundaries is minimized. A disadvantage of annealed copper may be additional droop in the unsupported section of the frame.

Before the bonding of the copper metallization to the gold bump takes place additional platings are usually applied to the copper. The additional metal coating (generally gold or tin) is applied to enhance the bond interface on the die and provide compatible metallizations for outer lead bonding. At the bumped die pad, the gold or tin plated copper lead frame is bonded with heat and pressure. On the substrate the bonding is accomplished by thermocompression bonding or solder reflow. Tin plated copper leads are used for the solder operations and gold plated copper for thermocompression bonding.

4. Die Separation

The conventional method of scribing wafers (usually done with a laser or mechanical scribe) is not appropriate for TAB because upon separation, die position and orientation is lost. However, recently, saws with diamond impregnated blades have been developed which provide a kerf width of 1.5 mils. With the advent of such saws, a method of die separation compatible with TAB technology has been developed. This involves mounting a wafer on a pedestal (mounting block) with a heat-release adhesive, then sawing through the wafer and partially through the pedestal. Using this technique, die orientation is preserved and dice may be released one by one by the heat of the bonding tool as they are bonded to the metal fingers attached to the tape. Proprietary pedestal material and heat sensitive adhesive have been developed which provide excellent bonding yields. Although the pedestal requirements are strict, the task of successful die separation is most strongly dependent on the saw which is used. Factors to be considered are kerf width and edge chipping. The saw blade used for die separation must rotate at 20-40K rpm; in general, the faster the better. Also, blade dressing on a daily basis and effective blade cooling are required. When these requirements are met, fast and efficient die separation is achieved.

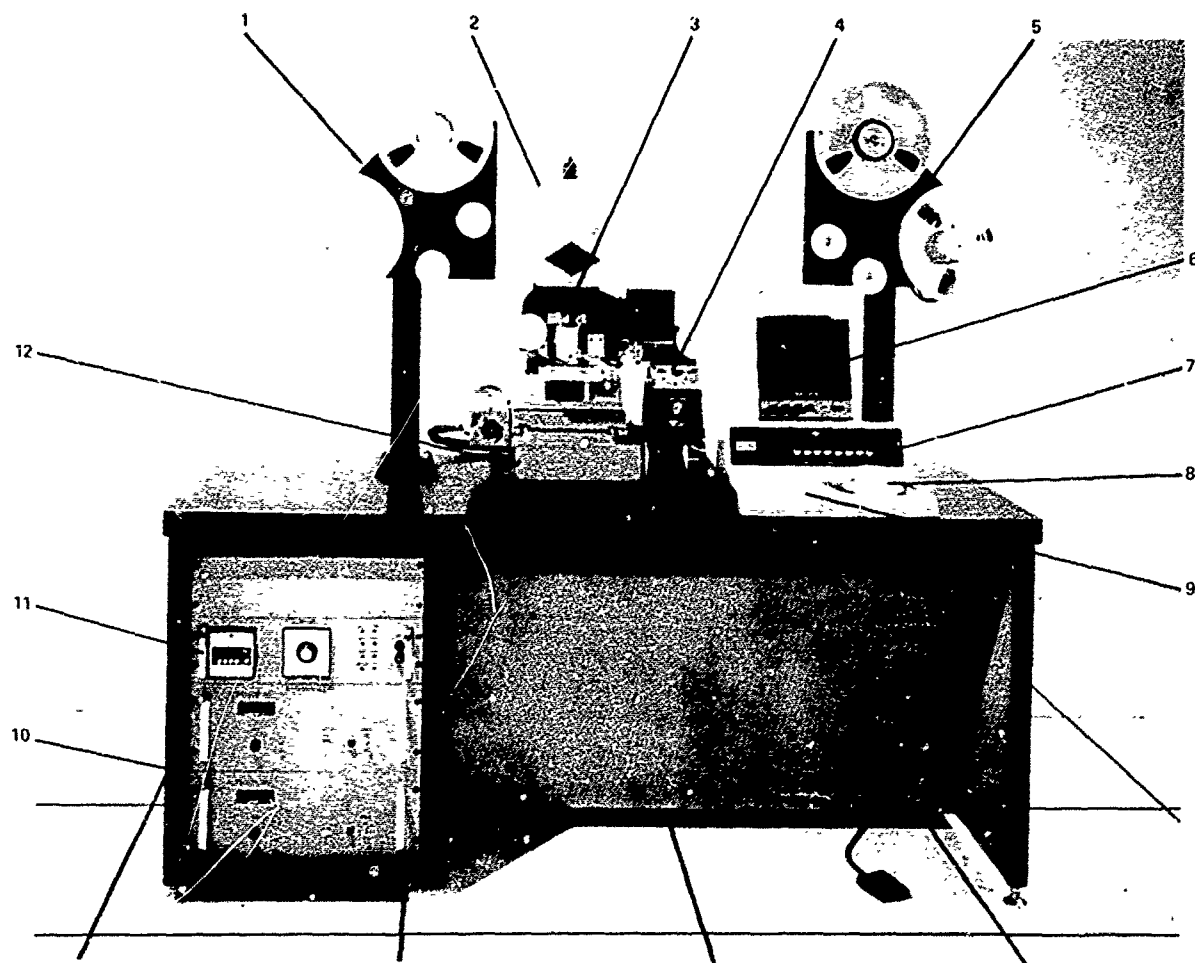
5. Inner Lead Bonding (ILB)

As clarification it should be mentioned that currently developed Inner Lead Bond systems do not require a bond of the chip to the plastic carrier. The chip is suspended by the lead frame at the joint to the chip bump. These bonds have sufficient mechanical integrity to jointly hold the chip in place over the cutout in the polyimide film. Additional mechanical protection is provided by the use of plastic separator tapes on the tape reel.

Considerable progress had been made in the Inner Lead Bonding (ILB) technique such that third generation production machines are now available. Highly automated ILB machines are available from a number of sources, such as the Jade Corporation (Figure 5), International Micro Industries and Honeywell Bull. All these machines perform the bonding operation in approximately the same fashion. That is, a simultaneous thermocompression gang bond of all lead frame fingers to the respective bumps on the chip.

Equipment and Operation (Typical to Jade Bonder)

The Inner Lead Bonder provides high speed (1500-2000 devices/hour) operator assisted attachment of the inner leads or interconnects on tape to semiconductor devices (IC or transistor chips). During the bonding operation the tape passes from a source reel into the bond area, a device is attached, and the tape is collected onto an output reel. Devices are mounted on the previously discussed pedestal in an ordered array (the sawed semiconductor wafer). The periodic spacing of these devices is utilized to mechanize the feeding and alignment of the device prior to bonding. The bonding



1. Tape de-reel system.
2. Bonder head and CCTV Camera.
3. Micro-Video objective.
4. Micromanipulator assembly
5. Tape re-reel system.
6. CCTV Monitor
7. Control Console
8. Micromanipulator control
9. Die plate control buttons
10. X-Y table control
11. Control panel, — Timer & Temperature controller
12. X-Y table

FIGURE 5. JADE INNER LEAD BONDER

takes place directly on the wafer. Automatic indexing of the tape is also provided; however the dimensional stability of the tape may not be sufficient to assure proper registration with the accurately positioned devices so provision is made for operator assisted final alignment of the tape.

A complete operational cycle in the run (normal) mode of operation consists of the four steps shown in Figure 6. The machine can also be operated in the set-up mode for such operations as tape loading, wafer loading, etc. The automatic pick and feed functions are provided by operator actions. An example of an IC bonded to the metal fingers is shown in Figure 7.

6. Outer Lead Bonding (OLB)

Outer Lead Bonding (OLB) is the key operation for successful implementation of the TAB program. Figure 8 shows the OLB sequence for the product fabricated at Honeywell Bull. The first photograph is a bonding site on multilayer substrate. Prior to die placement and bonding the substrate is coated via screen printing techniques with solder paste and thermally conductive epoxy. Next the device is excised from the tape and positioned onto the bonding site. Bonding of all the leads is done simultaneously. The other technique for attachment of the leads is thermocompression bonding. This operation is similar to that of reflow with one exception; that is, the joint is formed at higher temperatures and pressures.

Chip to Substrate Bonding

Chip attach may be performed with a number of different joining agents. The simplest approach is conductive or nonconductive epoxy. The type selected depends on the chip and its electrical application. Solder attach is also feasible and depends on the exact design of the bonding head and the thermal characteristics of the substrate. For solder attach the substrate temperature will have to be higher than if epoxy were used and additional heat must be applied during the press-down time by the bonding tool.

Lead Forming

Another important aspect of the entire joining process is the form that the lead has between the inner and outer bond. The form selected for the loop or path must be such that it imparts minimum stresses on the joints. One approach to the forming of leads is shown in Figure 9. In this technique an arc is selected for the interconnect path. This approach has the advantages of adding additional clearance to the exit of the lead from the chip and gradual transistion to the bonding foot for OLB.

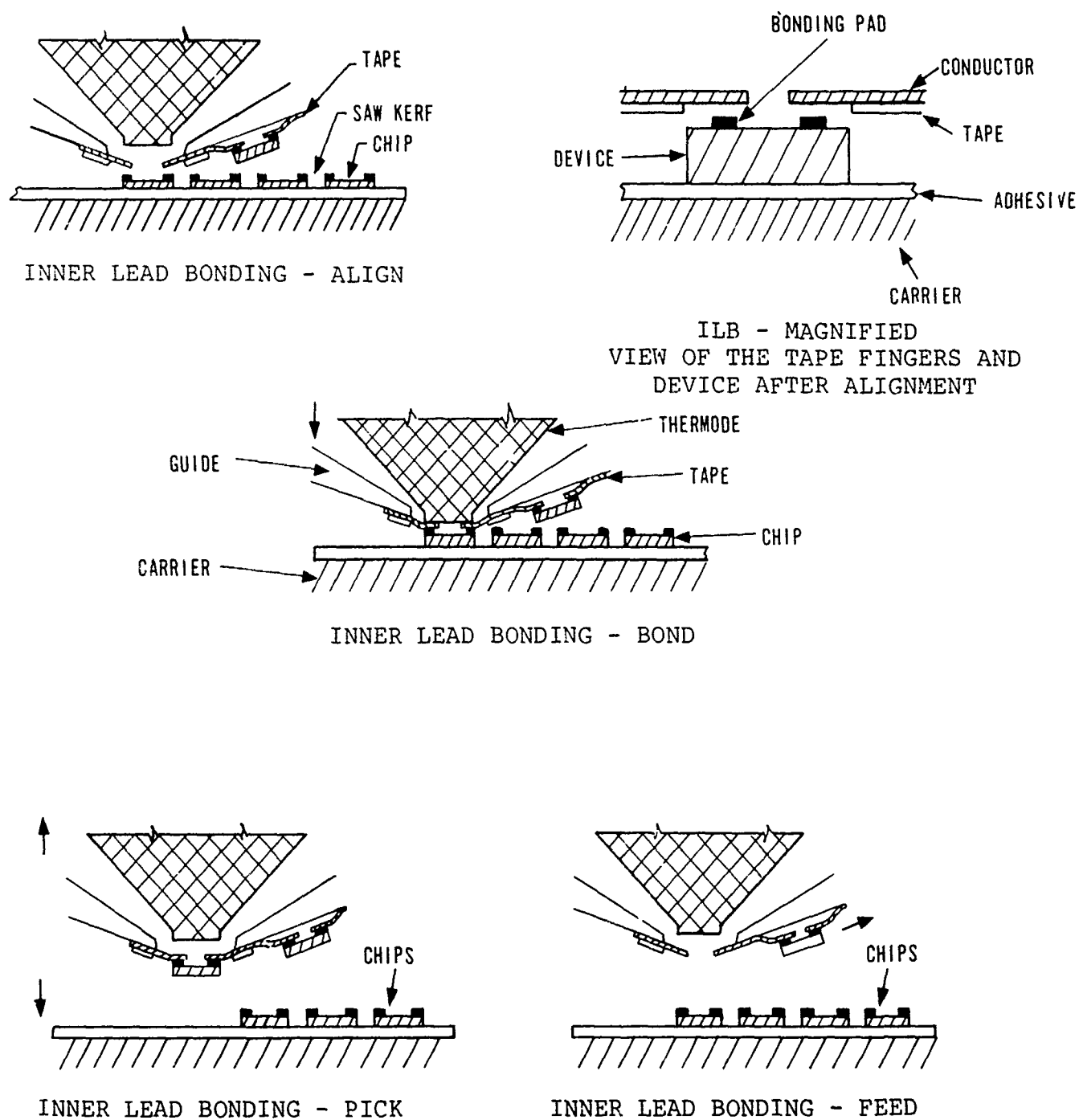


FIGURE 6. STEPS FOR INNER LEAD BONDING

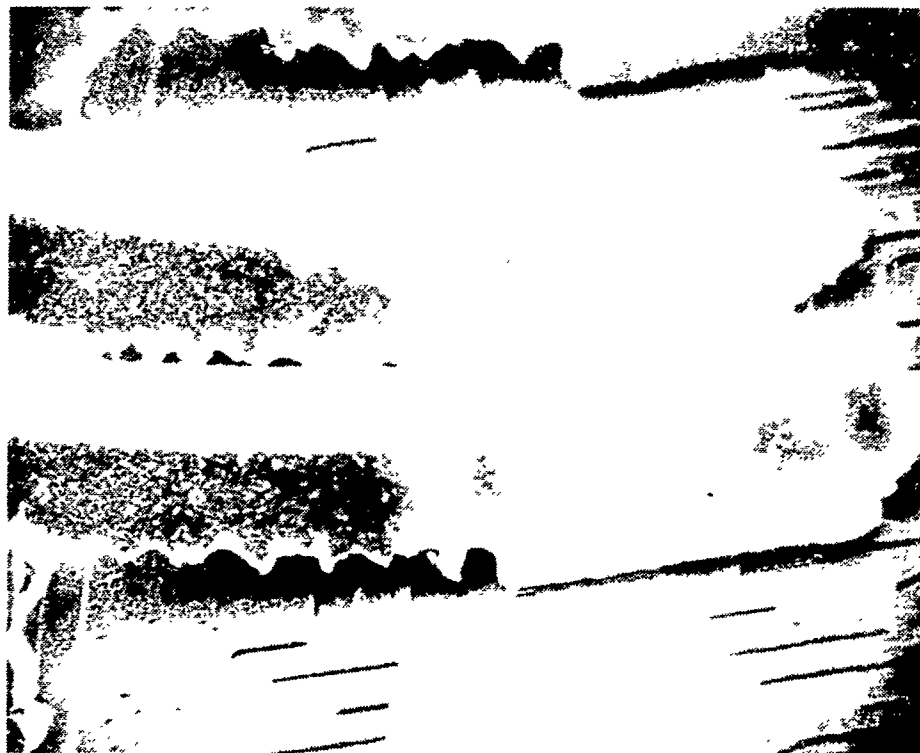


FIGURE 7 . SCANNING ELECTRON MICROGRAPH OF LEADS BONDED
TO BUMP ON CHIP

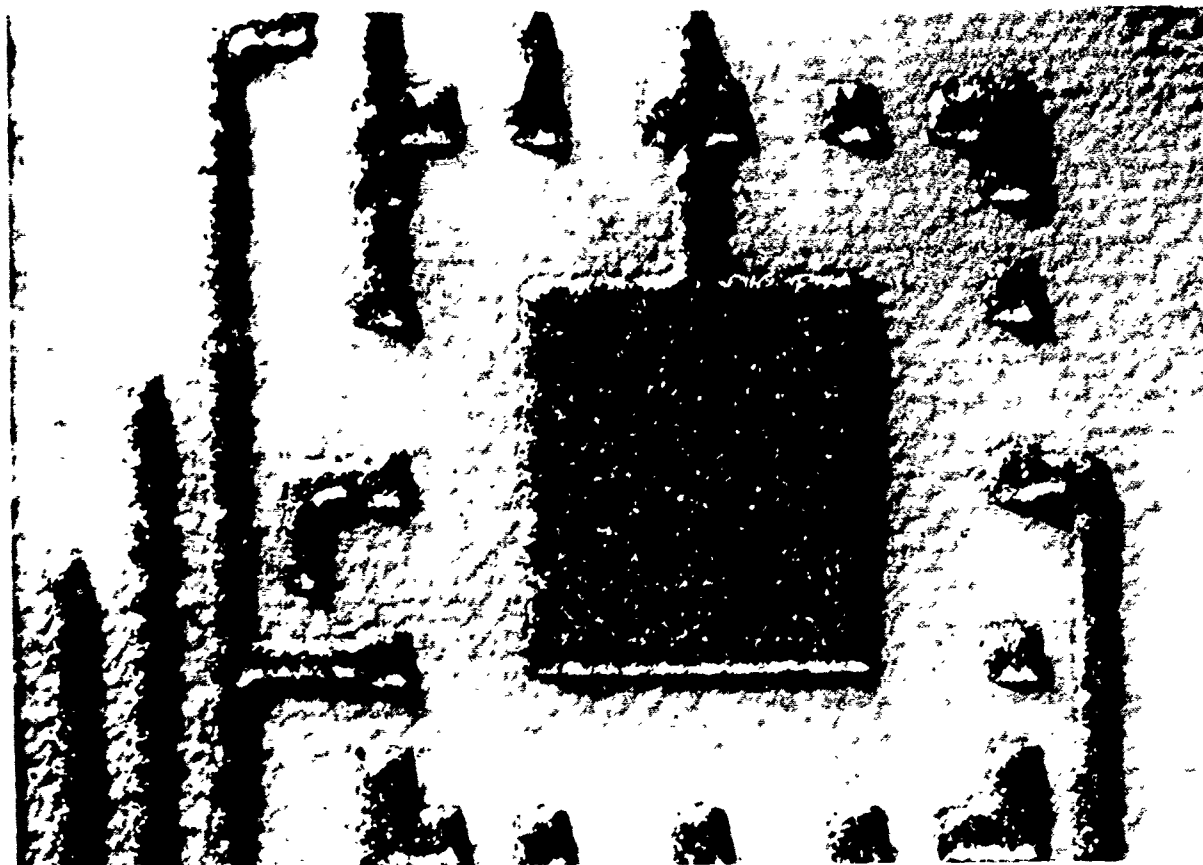


FIGURE 8a. BONDING SITE ON SUBSTRATE FOR LEADS AND CHIPS

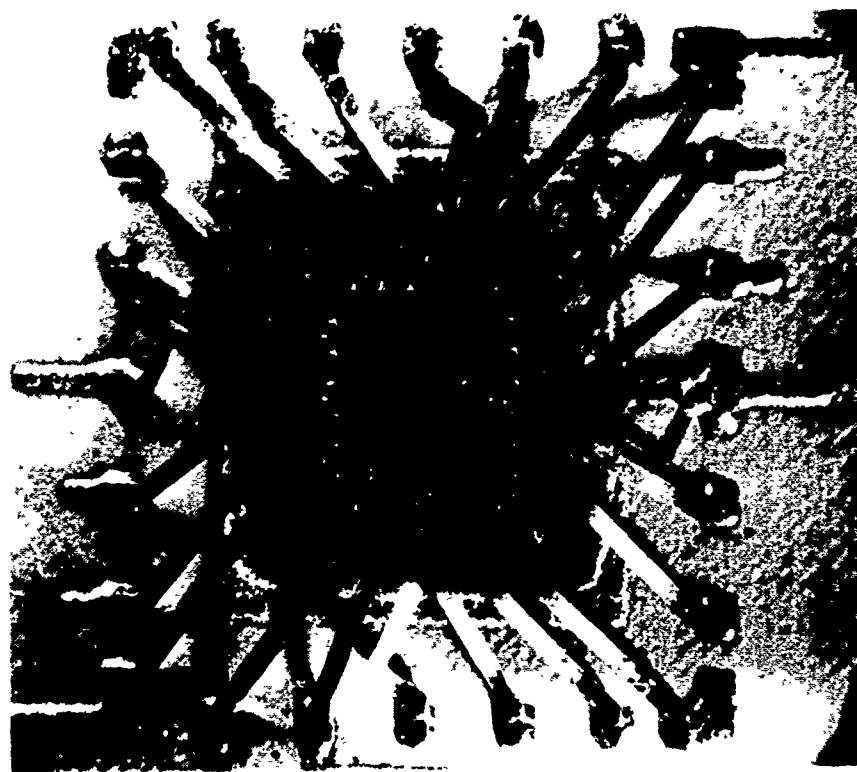


FIGURE 8b. EXAMPLE OF A CHIP BONDED TO THE SUBSTRATE



FIGURE 9. SCANNING ELECTRON MICROGRAPH OF LEADS SHOWING
TRAJECTORY AND STRESS RELIEF

7. Electrical Testing

Parametric Testing

A high speed parametric testing system which does three basic functions sequentially has been designed for automated testing of chips on tape. The first function, removal of shorting wires between leads which were needed for electroplating, can be accomplished by punching a hole in the tape. Step two consists of a mechanical locating system which pushes the tape up against stationery probe fingers, the output of which is connected to an automatic tester. The output of the test is then stored in a memory and when the device gets further downstream on the test head, a third operation occurs, which is the excising of bad devices. A subsequent mechanism senses the presence or absence of the device.

Coding

The inner lead bonder may contain a tape coding system which can punch a hole in the edge of the tape indicating that the device has been tested bad or good. Devices can also be coded so as to separate them into certain categories, providing a simplified means of identification on a preliminary basis. The codes on the tape can be read at a later date on the outer lead bonder which either accepts or rejects the device or uses it in a categorized fashion.

8. Rework Methodology

Basically, all assemblies made with TAB technology are considered repairable. Possible failure mechanisms include:

- Die mortality during final screening
- Misregistration of outer/inner lead bonds
- Ineffective chip attach
- Failure of one or more inner or outer lead bonds.

If a failure occurs in a thermocompression bonded device, its repair could be effected as follows. First the leads are cut to isolate the device from the electrical contact pads on the substrate. Then the device is pried or microchiseled free of the substrate. (Note: laser sectioning may be necessary to remove large chips.) Next, the bonding pads on the substrate are restored by removing old bond "feet" using a microshaving machine to remove all excess metallization and return the conductor pad to its original height. A new device is then epoxied or soldered in place and its leads thermocompression bonded to the old pads. Rework of solder bonded leads is relatively simple as the leads can be reflowed and the defective device removed or replaced.

CONCLUSION

The authors have attempted to cover a new and emerging technology in one paper and have therefore been forced to present only highlights of the process steps. As this technology advances and is accepted by more and more of the electronics manufacturing community it is anticipated that papers on TAB will become as common as those on wire bonding and die attach.

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3. "Beam Tape Automated Assembly of DIPs", C. Burns, A. Keizer and M. Toner, NEPCON/WEST 1975.
4. "Automated Beam Tape Microinterconnection Equipment", A. Keizer 25th Electronic Components Conference, IEEE, 1975.

A 'UNIVERSAL' TAPE CHIP CARRIER FOR MILITARY HYBRID PACKAGING

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ABSTRACT

A Tape Chip Carrier approach specifically designed for use in military-grade hybrid microcircuits is currently under development. This utilizes bonding "bumps" or projections on the tape leads rather than on the semiconductor device. While drawing upon technology developed for high-volume, low-cost (plastic DIP) integrated circuits, it has the unique advantage of compatibility with virtually all conventional IC chips, requiring no special wafer metallization. Because of this feature a number of problems are avoided including: (1) additional wafer fabrication costs and yield loss, (2) non-availability of specially metallized IC's, and (3) extensive reliability proofing of the different bonding metallurgies occasioned by various vendor-unique wafer-bumping processes. It allows the hybrid microcircuit fabricator the option of in-house conversion of conventional chips, with all the multiple-sourcing and other advantages presently enjoyed, to the tape format without reliance on outside sources of suitably tape-mounted chips. The resulting Tape Chip Carrier provides the anticipated advantages of testability, reduced chip damage during assembly, and reduced costs and operator dependence.

This paper discusses methods of fabricating polyimide-based Tape Chip Carrier materials with integrally formed bonding "bumps" or projections at the tip of each bonding lead or finger. The potential advantages of the general approach are shown and specific examples of such tapes made by alternate methods are displayed by micrograph and SEMgraph. Results of preliminary inner lead bonding experiments with such tape are shown, together with present and proposed techniques and equipment. A complementary activity using similar technology has resulted in a multilayer polyimide substrate with metallized bonding pads on the surface rather than plated through holes. This has led to investigation of alternate methods of outer lead bonding to both this substrate as well as conventional ceramic thick and thin film substrates.

INTRODUCTION

The value of the Tape Chip Carrier in semiconductor integrated circuit (IC) fabrication has been established by the recent conversion to this approach of the low-cost mass-produced plastic dual inline package (DIP) product lines in at least four major semiconductor houses. Manual wire bonding and die attach labor costs are eliminated and interconnection integrity and reliability enhanced (ref. 1, 2, 3, 4), leading to lower overall costs and better product.

The prospect of applying this technology to hybrid microcircuits is most attractive. The relatively short history of the hybrid has included many attempts to eliminate wire bonding. The greater complexity of more sophisticated hybrids increases cost, rework, and reliability problems which are accentuated by the chip's receiving no testing between wafer probe and hybrid functional test. Production-oriented techniques for large-scale testing of bare chips prior to die attach/wire bond are

not generally available. In spite of these shortcomings and the time and effort expended on wire bonds and their alternatives, the average military hybrid microcircuit producer, needing a variety of chips and lacking a captive IC line, still makes chip-and-wire-hybrids.

HYBRID REQUIREMENTS

Whatever became of alternatives such as beam-leads and flip-chips? In spite of their basic promise and attractiveness, a lack of availability, along with some unique problems (ref. 5,6) has prevented general usage. There are some notable exceptions: large-scale use of both flip-chips and beam-leads in communications or electronic data processing equipment and the commitment of sophisticated military systems to beam-lead hybrids. Successful use of such devices in large-scale hybrid production has virtually dictated a limitation of device types, the commitment of considerable capital, and often a captive IC line. Where such factors permit these approaches can be cost-effective and deliver a reliable product. For most military hybrid microcircuit producers they are unusable.

With the mixed history of special format devices, some hesitation by hybrid microcircuit fabricators in approaching the Tape Chip Carrier might be expected. While this is not uncommon, there are at least two very encouraging aspects to this technology. First it is coming from the opposite end of the industry spectrum. It is being spawned of necessity to satisfy the demands of a mass market rather than to develop special-purpose high-reliability military devices. Thus the technology is likely to develop and grow with more and more devices and device types committed to it. Secondly it offers ready pre-testing of the chip prior to bonding onto a substrate, something not generally accomplished with beam-leads or flip-chips. At the present time only one international EDP equipment manufacturer (ref. 7, 8) appears to be in a position to make immediate use of the Tape Chip Carrier in hybrids, but the basic attraction has accelerated interest and development work in many organizations.

Fundamental to the formation of a good tape semiconductor (inner lead) bond is some type of bump or projection which provides both the physical mass needed for good bonding and separation of the lead off the device surface. By far the most common method of producing this bonding bump is as a "standard" variant of the wafer metallization. This has a number of implications:

- Some type of special wafer metallization — quite different from the conventional — is required.
- Standardization of wafer metallization materials, thicknesses, etc., among different vendors, is extremely difficult because of proprietary processing variations, relative patent positions, etc.
- Matching such wafers to a tape suitably designed for hybrid microcircuit fabrication is by no means a trivial task. Not all present tapes allow device testing prior to substrate (outer lead) bonding. The lack of uniformity and standardization among the various wafer bumps is more than matched by the bewildering variety of existing tape sizes, formats, and metallurgies.

- Assuming suitably taped devices eventually become available, their different metallurgies and inner lead bonding processes may require imposition of temperature ladders, complicating hybrid fabrication and repair processes.
- Use of the Tape Chip Carrier format implies that all devices required for a given hybrid should be available (and even second sourced) in that format. Mixing conventional and special format chips in the same hybrid has often proved inefficient.
- The per-chip cost of specially metallized devices is usually higher.

It appears nearly certain that Tape Chip Carrier use for discrete IC production will increase both in units produced and numbers of producers. With its cost and reliability advantages, the technology will find its way into hybrids. It will probably find first use in those areas of commercial, high-grade electronics which readily lend themselves to automated processing, e.g., computer circuitry or communications gear. The military hybrid producer, with his usually smaller production runs and his need for greater chip variety, may be left somewhat out of the mainstream of this development. Uncertain of his ability to buy sufficient suitably taped devices, he will likely remain reluctant to repeat the experience with other special-format chips.

Eventually, given the size of the overall hybrid microcircuit market, it seems probable that some source of taped devices allowing pretesting and substrate bonding with a reasonable degree of standardization will become available. There may someday be a 'taping' house geared to the requirements of the hybrid industry. However, there is the distinct danger of the type of situation — users don't commit because of lack of availability, producers don't increase production because of lack of market — that has hampered beam-leads in particular.

One alternative is to purchase standard aluminized wafers and specially metallize (and perhaps passivate) them in-house or through some outside service organization. Besides the questions of numbers and costs of photomasks, possible contamination, IC metallization variables, handling and logistical problems, and ultimate product reliability, this might well leave each producer with a unique materials system and tape format, increasing costs and defeating standardization.

BUMPED TAPE — AN ALTERNATIVE

In order to utilize the basic technology in as expeditious a manner as possible, we have pursued alternative approaches. Considering the extensive availability of standard aluminized (together with some gold-metallized) IC chips and wafers, we concentrated considerable effort on placing the bonding projection or bump on the tape lead rather than on the device. A number of characteristics are required of such a tape:

- Complete testability, DC, AC and functional, of the chip mounted on the tape.

- Tape metallurgy and bonding techniques that are compatible with conventional aluminized or gold-metallized semiconductor IC chips.
- Tape fabrication methods which provide yields and costs attractive to hybrid production.

There are other desirable features:

- Compatibility with thermocompression inner lead bonding. This might simplify reliability considerations and would reduce subsequent temperature ladder problems.
- The ability to excise the chip and attached leads from the tape carrier during or immediately after outer lead bonding without the need for expensive tooling for each die size or family of sizes.
- The option of bonding the device face-up onto the substrate with all bonds visible for inspection.
- The option of eliminating all organic material from the device itself once outer lead bonding is accomplished. This exacts some penalty on edge-short protection and may ultimately prove unnecessary as other organic materials may remain within the hybrid package. However such materials do require strict pre-seal cleaning, drying, and outgassing procedures (ref. 9)

BUMPED TAPE - FIRST RESULTS

General Dynamics has taken several alternate approaches to the fabrication of bumped tape meeting these requirements and most of the desirable features. Both in-house tape processing and cooperative efforts with outside vendors have been undertaken. As a result a number of sample tapes have been produced and used in initial bonding studies.

At the present time all work is being carried out with gold-over-nickel-over-copper bumps bonded by steady-state heated tool thermocompression bonding onto aluminized IC chips. In the immediate future similar bonding onto gold-metallized chips will be conducted, a more attractive situation. In spite of the well-known problems involving gold and aluminum, it offers a single well-studied material system in contrast to the myriad of vendor-unique metallurgical systems currently used for inner-lead bonding. The use of thermocompression-bonded gold-plated copper leads for the outer lead bonding is attractive for most hybrid substrates and has extensive background (ref. 10, 11). Specification of nickel barrier thickness, gold plating thickness, and bump size and shape is a part of our present study, as is the role of the copper and nickel in bond formation and reliability. Although this approach may be only an interim one, until such time as suitably taped chips are generally available, the expected increase in availability of gold-metallized devices may make it more generally attractive.

An in-house development program has been pursued for the last 18 months to establish our capability to fabricate tape and the feasibility of forming integral bonding bumps on the ends of tape leads. Both "bumpless" tape (Figure 1) and bumped

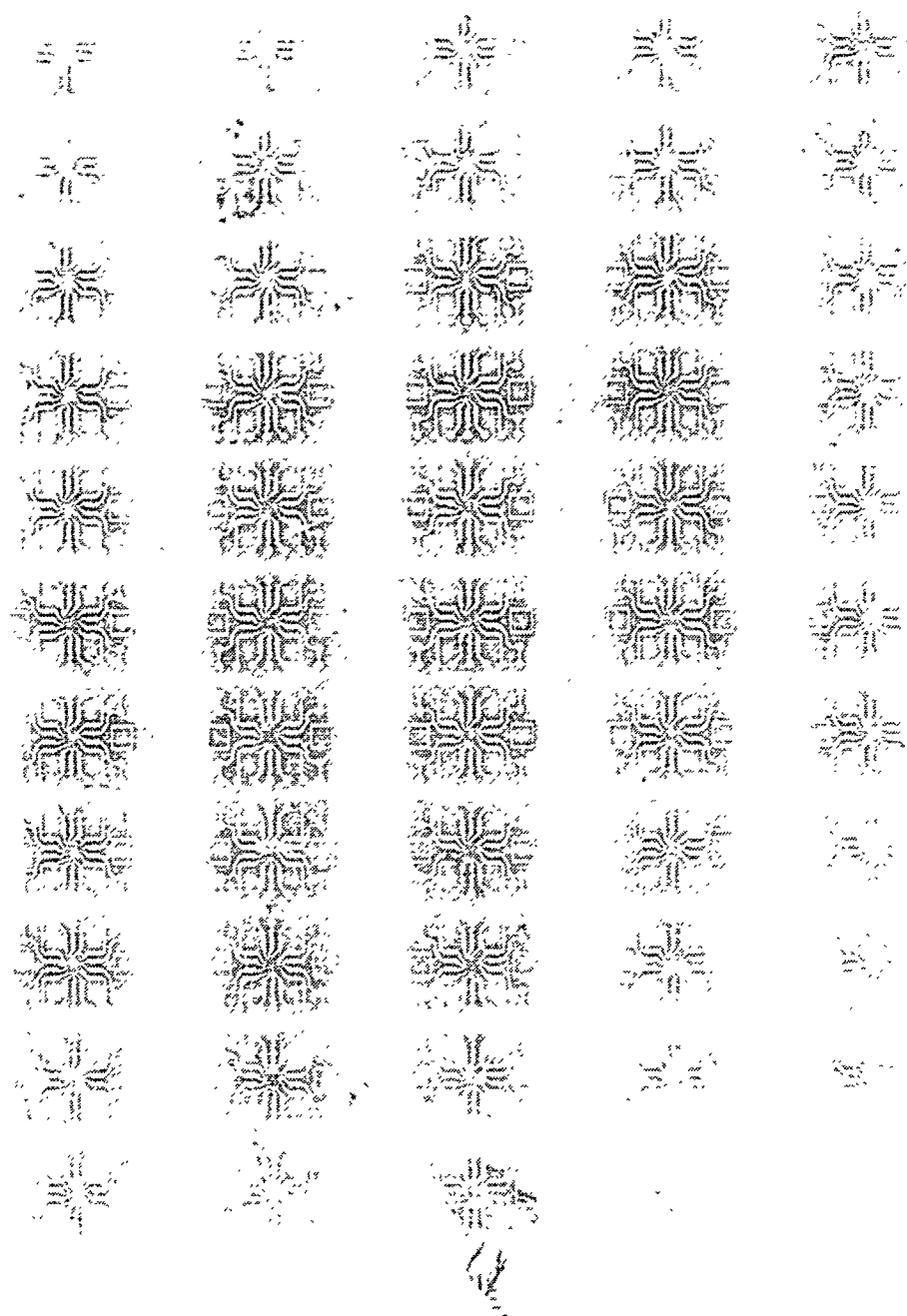


Figure 1. Conventional Tape — General Dynamics.

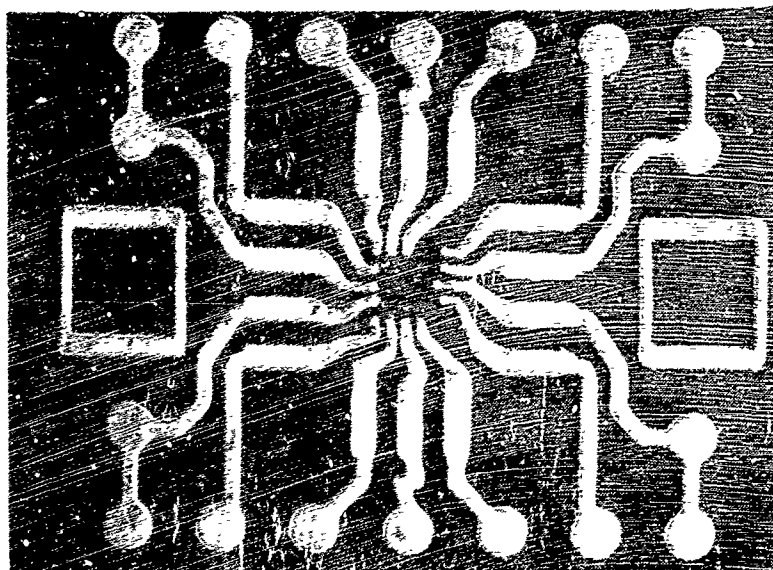


Figure 2. Selectively Plated Bumped Tape - General Dynamics.

tape (Figure 2) has been made. Contrary to conventional wisdom at the time, producing such tape was found to be a relatively straightforward extension of fine-line flex circuit fabrication, well within the capabilities of many organizations, and should present few availability problems. To verify this a number of cooperative programs were started with outside vendors possessing related capability.

A type of bumped tape, produced as a best first effort by the 3M Corp. is shown in Figure 3 and Figure 4. While this particular sample is all-metal and thus not testable, it can be converted to a polyimide laminate with electrically isolated leads. That form of the tape is now being developed. This particular sample, formed of rolled-annealed copper and plated with gold over nickel, exhibits excellent definition of the approximately $80\text{ }\mu\text{m}$ ($0.003''$) diameter bonding projections (Figure 5) and excellent overall plating coverage (Figures 6 & 7). Overetching leading to excessive thinning of the lead adjacent to the bump was overcome in later attempts. Producing such tape, particularly in the all-metal format, is considered routine by 3M who also believes it may offer considerable advantage over the conventional two or three layer copper laminated polyimide tape now being used for commercial DIP production. Bumped all-metal tape can be made at least as cheaply and eliminates the need for additional wafer processing. Such a development would greatly accelerate the bumped tape concept.

Initial inner-lead bonding attempts with this tape have proved most encouraging. While we are now taking delivery of a Jade Mark IV JEMS/LAB gang-bonder, our first attempts utilized simple modifications to a conventional wire bonder, and experiments were limited to single-point bonding of individual tape leads to individual device bonding pads. Bond time, pressure, tool configuration, and tool temperature were varied with the chip on a room temperature stage, simulating conditions

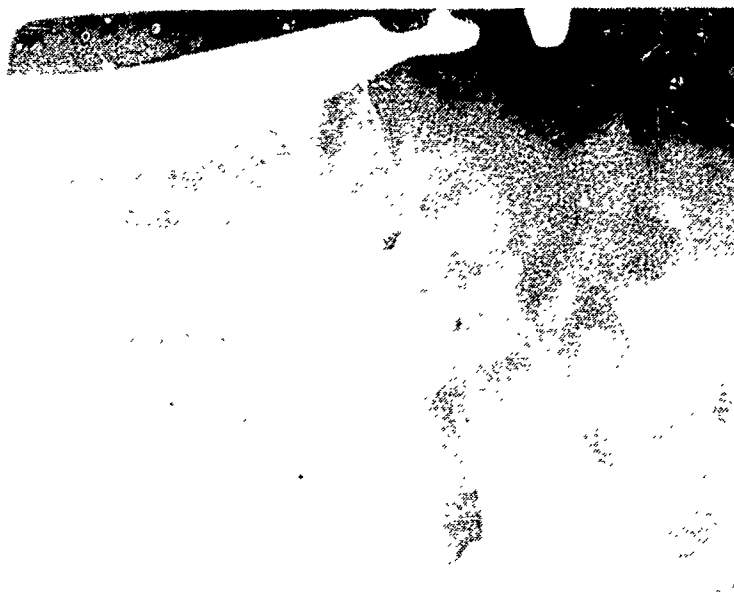


Figure 3. Bumped All-Metal Tape - 3M.



Figure 4. Bumped All-Metal Tape - 3M.



Figure 5. Single Bonding Projection - 3M Tape.

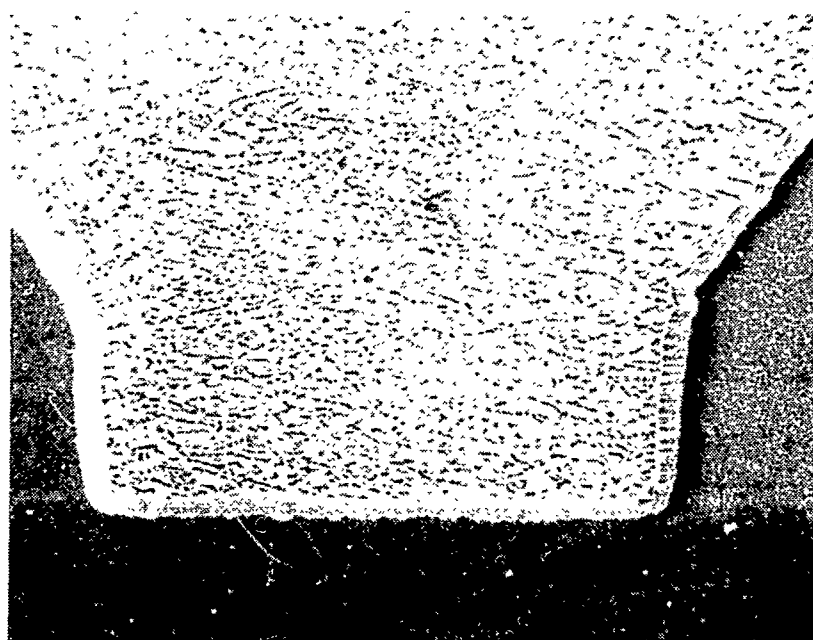


Figure 6. Cross-Section of Single Bonding Projection - 3M Tape.

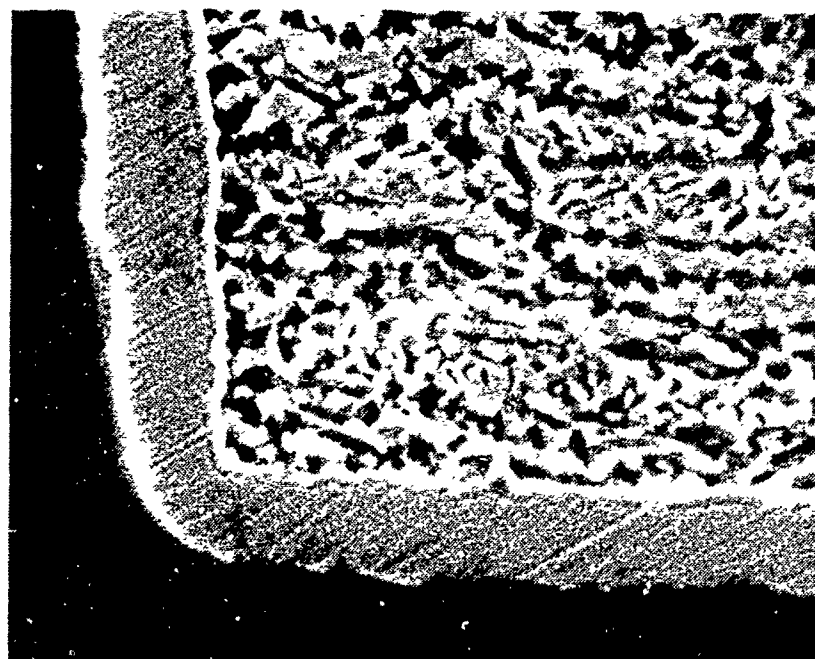


Figure 7. Detail of Figure 6 Showing Excellent Plating Coverage.

on the gang bonder. Simple fixturing was used for tape/chip alignment with individual (electrical reject) chips affixed by a modified thermoplastic wafer mounting cement.

Results of the earliest experiments using this tape showed an underbonding condition which was corrected by increasing bond interface temperature. The resultant gold-aluminum bond, while by no means optimized, is mechanically robust allowing routine handling and simulated testing. Meaningful mechanical strength measurements were compromised by the overetched and weakened tape and by the variability inherent in these early bonding experiments (Figure 8).

The excellent edge-shorting protection afforded by this design is easily visible in cross-sections (Figures 9a and 9b).

In considering the edge shorting problem, as well as alternate methods of making bumped tape, the idea logically evolved to achieve shorting protection by using the polyimide portion of the tape. One method, starting with a copperclad polyimide sheet, is to etch holes through the polyimide and plate copper through the holes to form the bumps. Later etching and plating steps can then form the lead pattern in the laminated copper and coat the bumps with the desired metallurgy. Similar bonding bumps are formed at the opposite ends of each lead for inner and outer lead bonding. The polyimide carrier film covers the entire lead on the chip side between these two bumps, thus providing complete shorting protection from the chip edge or adjacent substrate metallization.

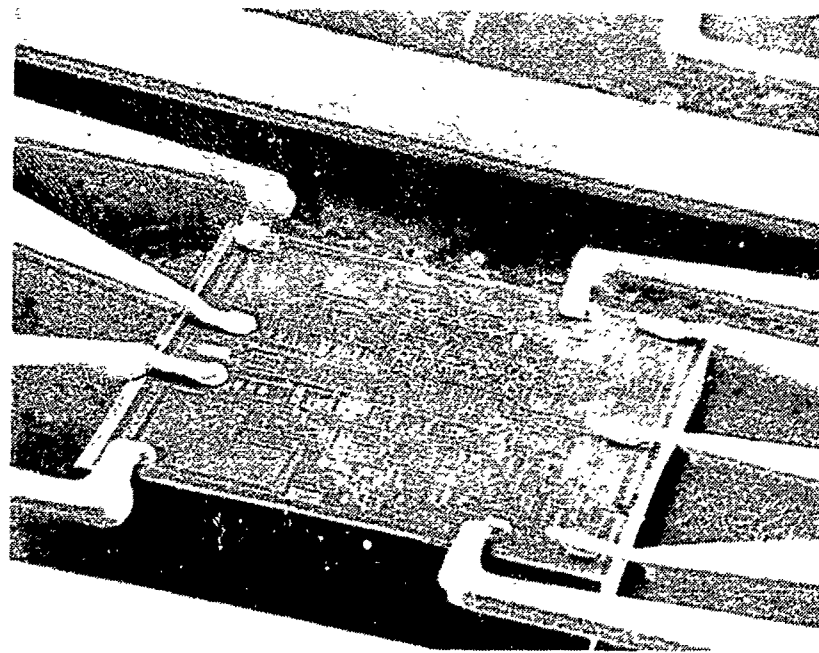
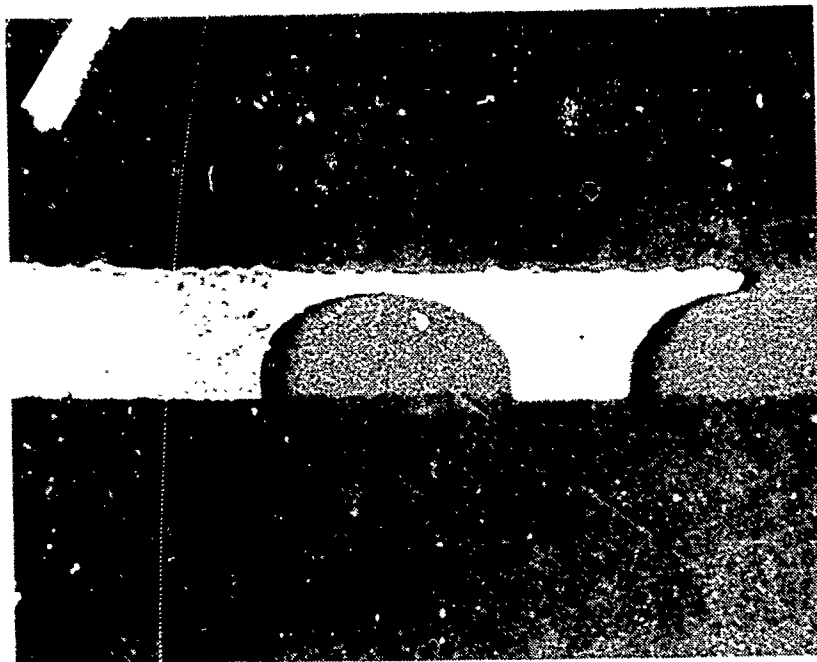


Figure 8. NSC 747 Bonded to 3M Tape Using Single-Point Technique.

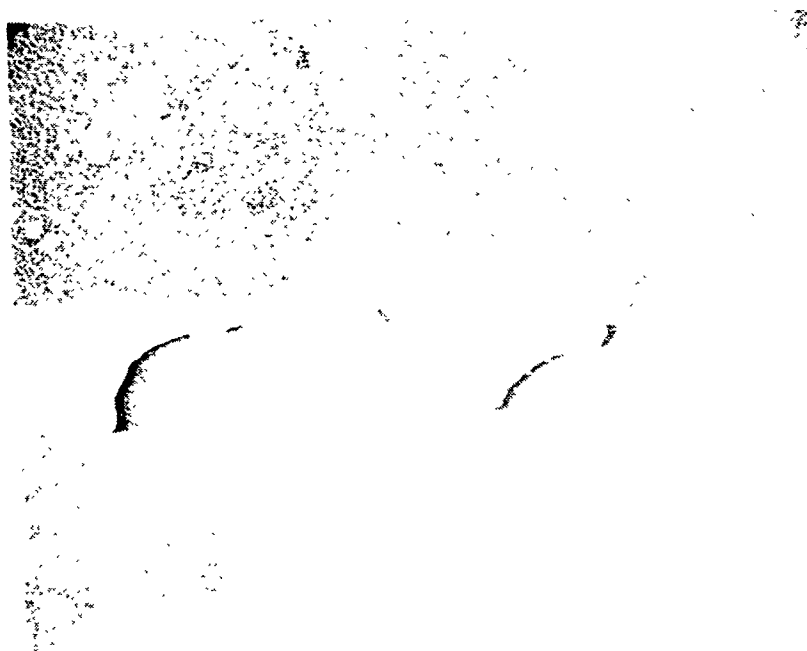
Following this approach, Chem-Aero, Inc., executed some initial tests with artwork which, while optimized for another process, was inadequate for this one. Because of this and some first-attempt processing difficulties, only a few samples became available. Figure 10 shows the configuration of the inner lead bonding bump which extends up from the surface of the film by perhaps $20\text{ }\mu\text{m}$ ($0.0008''$). Undercutting during the polyimide etch is evident, and the gold-plating thickness was inadequate. However, initial single-point bonding attempts were partially successful, frustrated mainly by the small physical size of the tape samples. Further work is planned.

Another approach to bumped tape was pursued by the Pactel Corp. In this case the tape, together with the integral bonding bumps for inner and outer lead bonding, is built up by an additive process. As before the polyimide covers each lead between the two bumps, affording the same type of shorting protection. All copper in this system is electrodeposited, and various bonding metallurgies are available at the bumps. A number of sample batches of tape, with thousands of frames each, has been fabricated with several artwork and process iterations. Although this is the first time to our knowledge that tape of this type has been made, and while the entire process is still experimental, initial results are most encouraging.

In its most recent configuration, Figures 11 and 12, this tape displays a unique concept which we call the "pop-out" bonding platelet. This is the small area of polyimide in the center of the tape frame which contains the lead pattern with connected inner and outer lead bonding bumps. Upon moderate pressure with a crude metal or rubber "punch" or by bending the tape in a controlled tight radius, this platelet "pops out" of the tape (Figure 13). In use the tape would be inner lead bonded to the chips, the platelet remaining in the tape. After chip pretesting or



(a) BEFORE



(b) AFTER

Figure 9. Cross-Section of Typical Lead of 3M Tape Before and After Inner Lead Bonding. Note Clearance From Chip Edge.



Figure 10. Inner Lead Bonding Bump — Chem-Aero.

other preconditioning, the outer lead bonds are formed, leaving the platelet with attached chip mechanically and electrically connected to the substrate. The tape is now withdrawn, easily extracting the platelet/chip combination which remains in place on the substrate.

The inner lead bonding bumps, Figures 14a, 14b, and 15 extend above the polyimide film by at least $10\text{ }\mu\text{m}$ ($0.0004''$) and have more than adequate gold for bonding (approximately $6\text{ }\mu\text{m}$ ($0.00025''$)) on their surface. Single-point bonding experiments with this tape have been only marginally successful thus far, apparently due to the heat-sinking of the small heated bonding tool to the greater amount of polyimide material immediately adjacent to the leads and bumps. Samples are now undergoing gang-bonding evaluation where the more massive thermode should supply sufficient heat for proper bond formation.

AN ALTERNATIVE SUBSTRATE

An interesting corollary of this technology is the fabrication by Pactel of sophisticated multilayer substrates. An example is shown in Figures 16 and 17 which illustrates a four-layer multilayer replacement for a similar thick-film multilayer. As shown, these substrates are batch fabricated for reduced costs. Minimum lines and spacings are less than those common with larger thick-film multilayers without

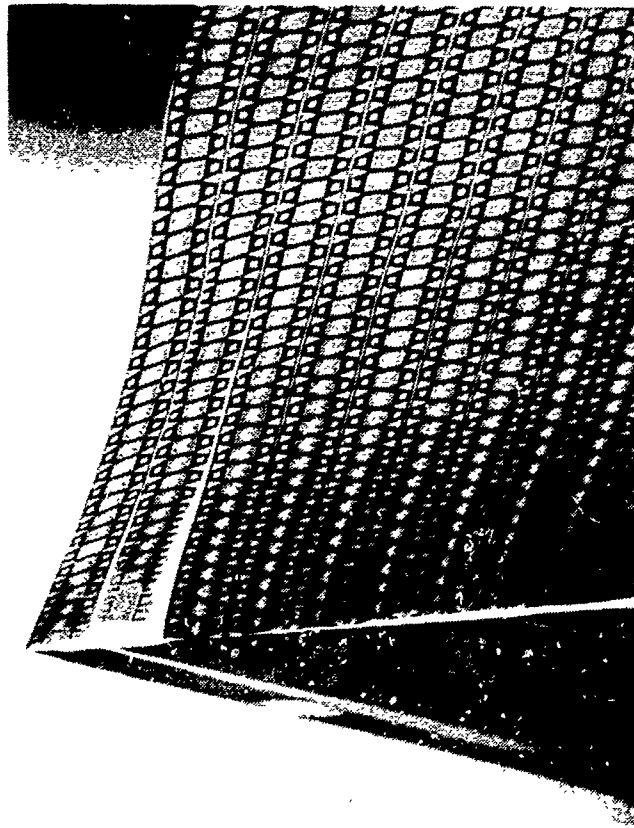


Figure 11. Tape Array Showing Slit Ends - Pactel.

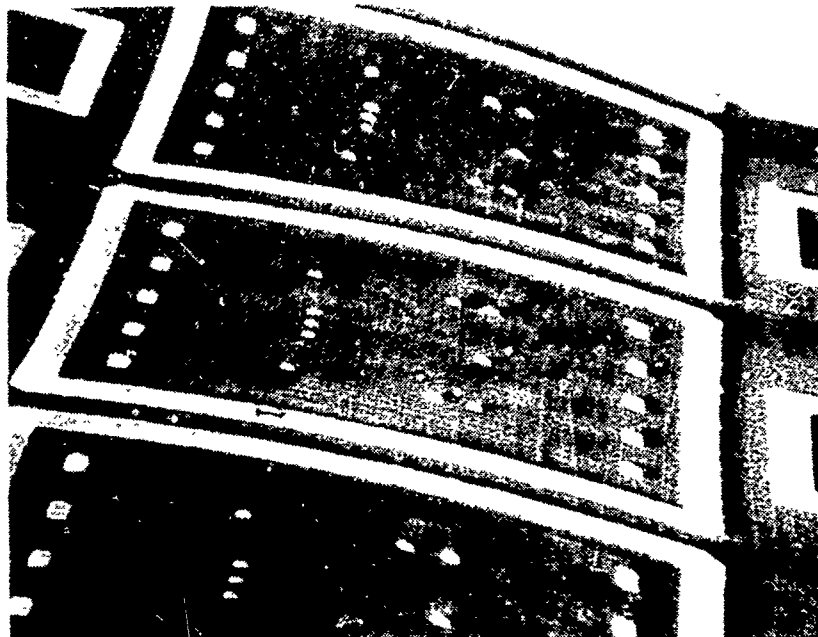


Figure 12. "Pop-Out" Tape Showing Bonding Bumps - Pactel.

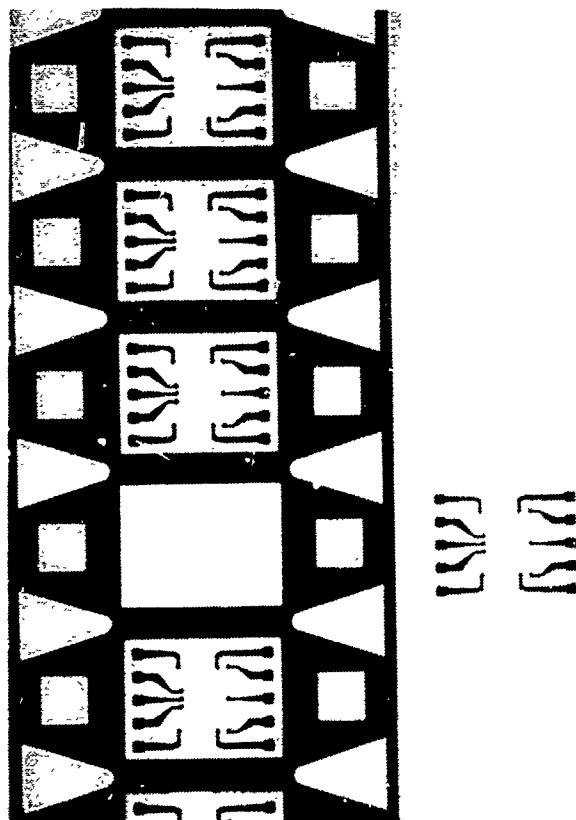
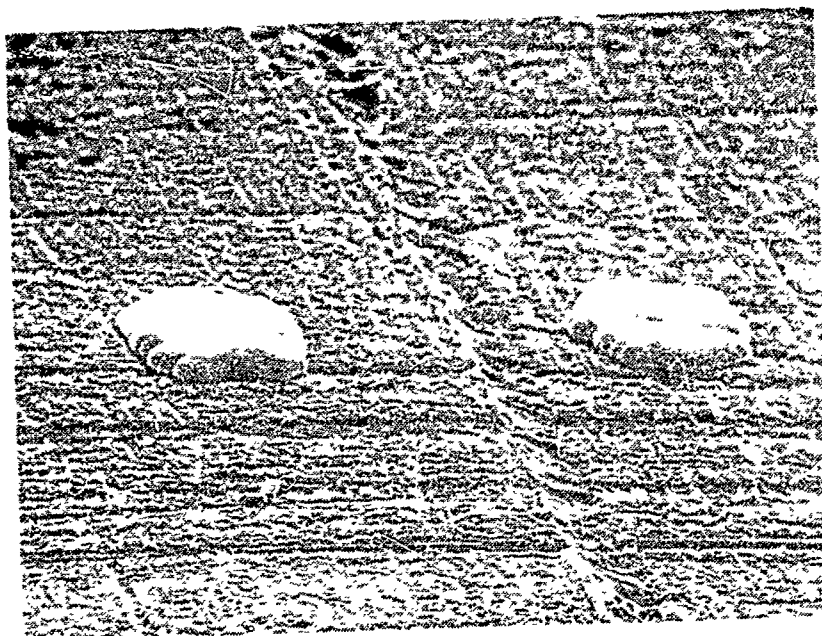


Figure 13. "Pop-Out" Tape With Separated Bonding Platelet — Pactel.

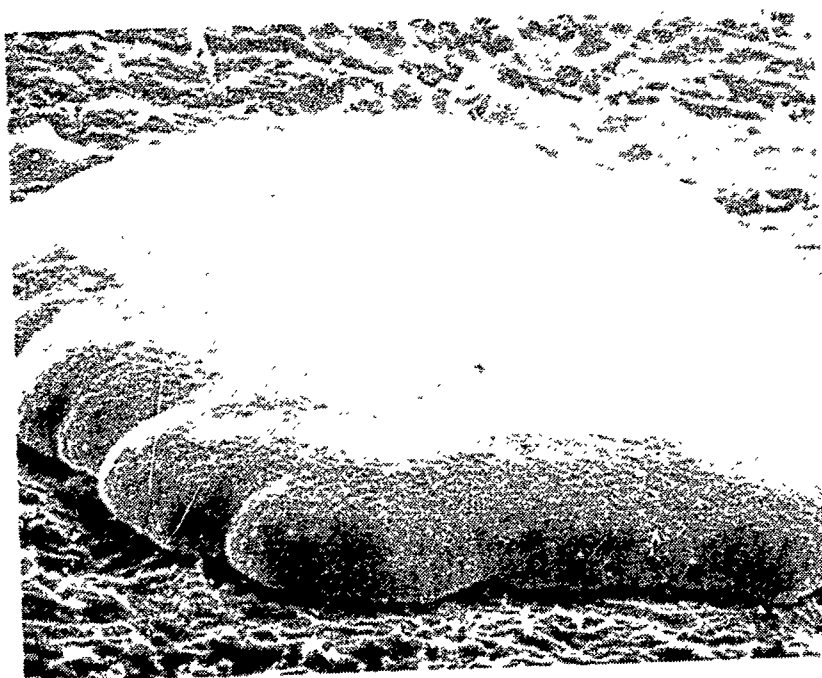
undue sacrifice of conductivity as all buried layers are pure copper. Surface metallurgies allowing ultrasonic or thermocompression bonding or a choice of soldering operations are readily achievable. Although the circuitry can remain flexible, similar to the tape, it may also be laminated to a variety of backing or stiffening materials such as aluminum, copper, kovar, or ceramic. These can provide integral mechanical, thermal, and electrical functions such as heat sinking or electrical shielding.

CONCLUSIONS

In summary, we have established the feasibility of fabricating tape, by at least three different methods, for Tape Chip Carrier applications with the bonding projections integrally formed on the tape leads. Such a tape can be successfully bonded to aluminized IC's. This approach is viewed as being complementary rather than necessarily competitive to the bumped chip technique. Ultimately the semiconductor houses, or other agencies, will probably make available to hybrid users some suitable form of taped chips. In the interim there is a great need for flexibility of approach, particularly for the non-chip-producing military systems house, in order to make significant use of this packaging style in the near future and to maintain a capability to stay up with this rapidly evolving technology. Experience has shown that it is not cost effective to become locked into processes and equipment too early in an area of rapid technological growth.



(a)



(b)

Figure 14. Details of Inner Lead Bonding Bumps - Pactel.

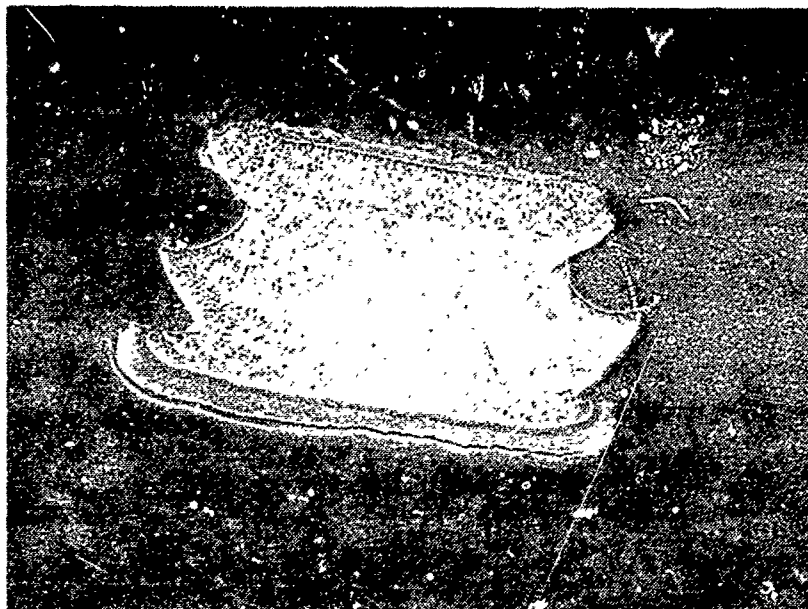


Figure 15. Cross-Section of Inner Lead Bonding Bumps — Pactel.

The polyimide substrate which is an alternative to thick-film multilayers, while useful for conventional assembly methods, is quite complementary to the gang-bonding of tape carried chips. With its cost advantages, surface flatness, fine-line capability, ruggedness, and tremendous variety of available forms, it provides avenues of packaging design heretofore unavailable.

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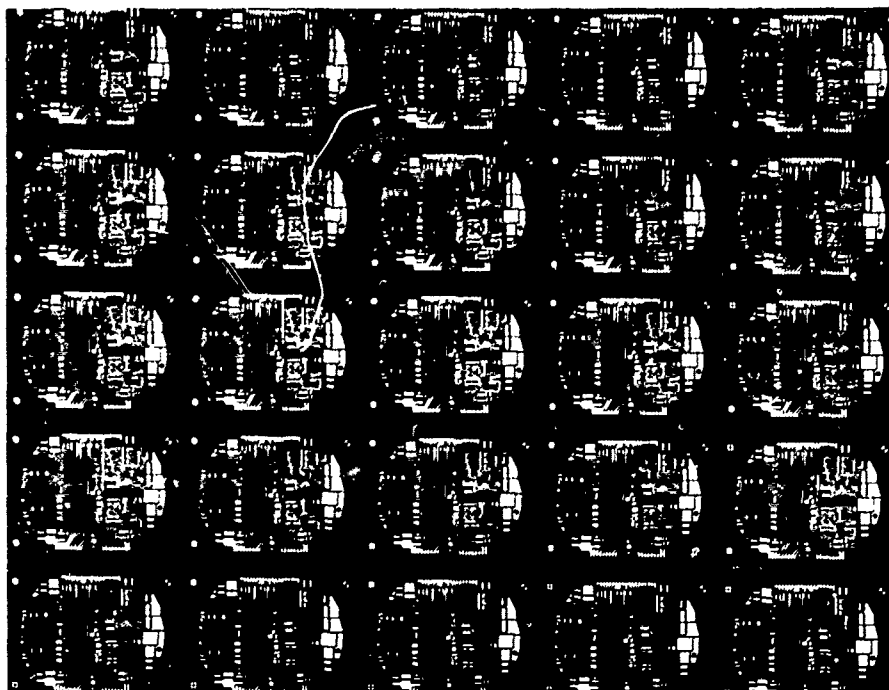


Figure 16. Array of Multilayer Polyimide Substrates — Pactel.

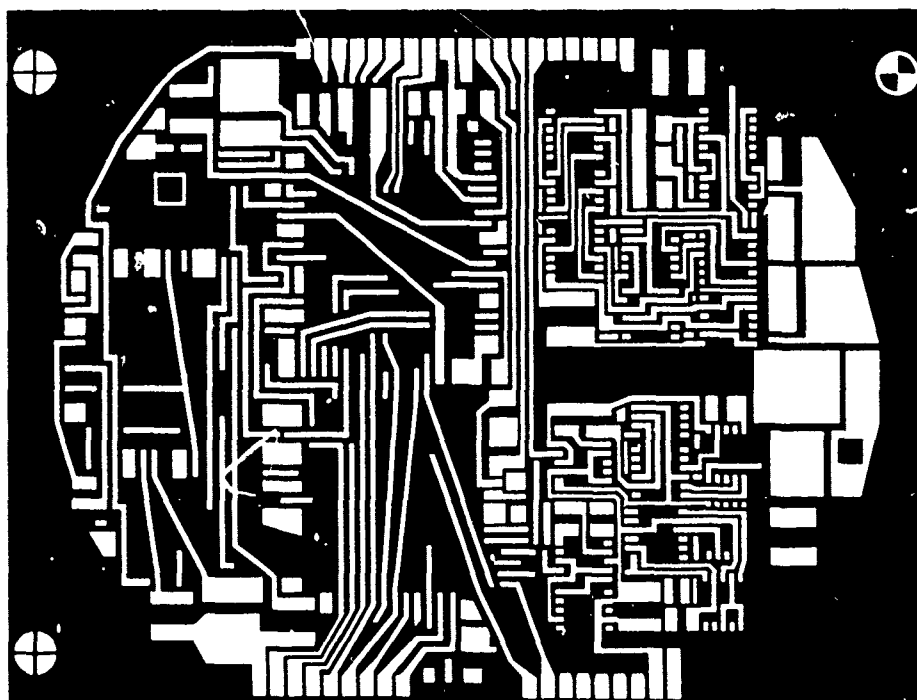


Figure 17. Polyimide Multilayer Substrate — Pactel.

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THE AUTOMATION OF CERAMIC MICROCIRCUITS FABRICATION

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ABSTRACT

Hybrid technology has existed and been used in military electronics for over two decades. However, the full economic advantage available has not yet been realized as these hybrids have been fabricated by slow manual techniques. A versatile hybrid automation concept capable of producing the wide range of hybrid circuits required in military electronics is needed to achieve the potential cost savings.

INTRODUCTION

During the past two years, ECOM has supported a program which has successfully demonstrated a highly automated and versatile concept for the fabrication of ceramic microcircuits. These techniques were developed using as a vehicle a fuze circuit developed at Harry Diamond Laboratories. The concept has wide applications and can be used to fabricate any circuit whose length and width are less than four inches. This paper will discuss the application of this concept and the proposed fully automated line in the manufacture of hybrids used in equipments developed under ECOM sponsorship.

The demonstrations conducted during this program verified that this concept can

- reduce manpower requirements by approximately 9:1
- increase yield and significantly reduce rework through improved reproducibility of machines
- greatly increase reliability and substantially reduce need for manual inspection

This paper consists of three main sections. A discussion of the demonstrations conducted in the ECOM program just concluded. Then a detailed discussion describing a proposed fully automated line capable of producing over 600 ceramic microcircuits per hour. In conclusion, data is presented on the economic aspects of this automation.

The three major hybrid operations, thick-film printing, chip placement and wire bonding are described in detail. For each of these operations, the generic production rate is developed and the actual production rate of the subject circuits for the manual and automated methods tabulated in concise form.

ECOM CONTRACT

To fulfill the requirements of the recently completed ECOM contract, RCA demonstrated a production rate of 125 circuits/hour for all operations required to fabricate the XM-734 fuze amplifier hybrid. Only the three major operations - thick-film printing, chip placement and wire bonding will be discussed in detail.

Automatic Thick-Film Printing

The printer complex (Figure 1) used in this demonstration consisted of a magazine loaded printer, automatic ejector, synchronized collocator-belt and conveyORIZED dryer. Using this complex, material handling is reduced to magazine loading operations, and one operator can print 750 substrates per hour. This operator loads the magazine in the autoloader, inspects and does other tasks as required. The magazine capacity is 400 to 450 substrates for 45 minutes of work (figure 2). A logic system controls the loading and transfer of the substrates from the loader to the printer platen (Figure 3). This fluidic/pneumatic logic system is compatible with the control system of the printer. A vacuum pickup arm reaches down through the base of the printer table to engage the uppermost substrate. The arm lifts the substrate out of the

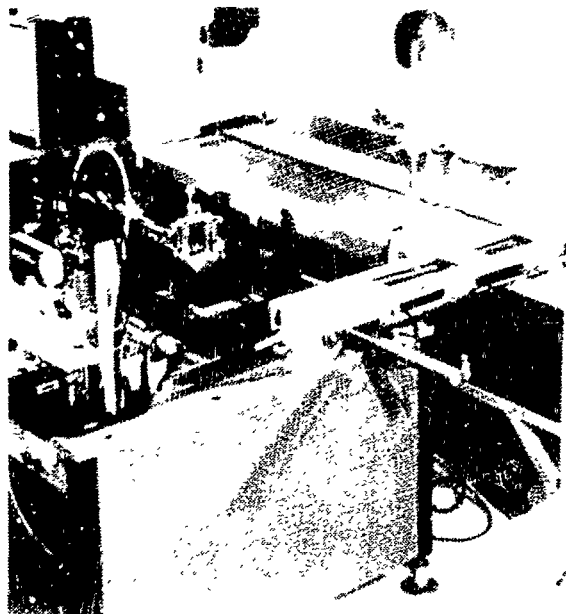


Figure 1. PRINTER COMPLEX



Figure 2. SUBSTRATE MAGAZINE

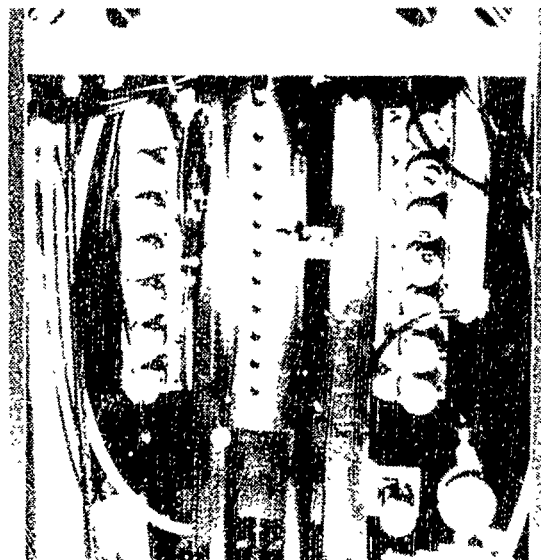


Figure 3. AUTOLOADER LOGIC

magazine while the platen is in the printing position. As the platen returns from the printing to the loading position, the substrate is transferred by the printer ejector to an intermediate position and then to the collocator belt.

This belt moves in synchronous increments as dictated by the production rate of the printer. When the printed substrates reach the end of the collocator-belt tunnel, they are transferred to the dryer belt in a preselected count (such as four abreast) to use the full capability of the drying furnace. Then the substrates move through the inspection station, prior to the drying oven cycle (Figure 4).

One of the important numerous features of this equipment is the camber sensor which inhibits the printing of substrates whose topology limits good line definition. This inhibition allows faulty substrates to be removed after the first pass and so eliminates unproductive subsequent processing.

Capacitor and semiconductor chip attachment was performed using an automated equipment called a Chip-Assembly-Robot (Figure 5). This equipment can accurately locate 1400 active or passive chips per hour. Programming is accomplished by manually stepping the machine to the desired locations and storing the locations simultaneously

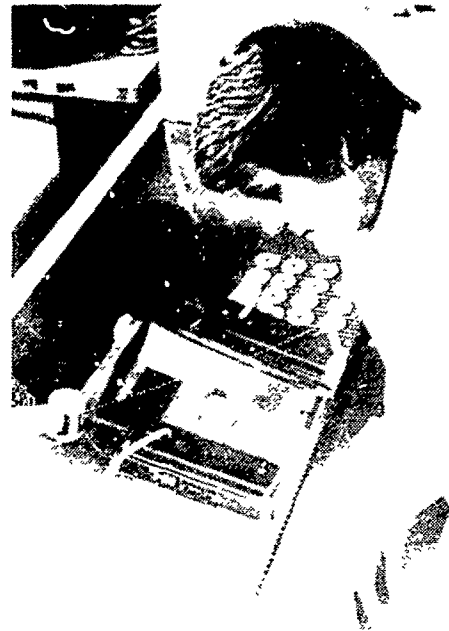


Figure 4. SUBSTRATE INSPECTION

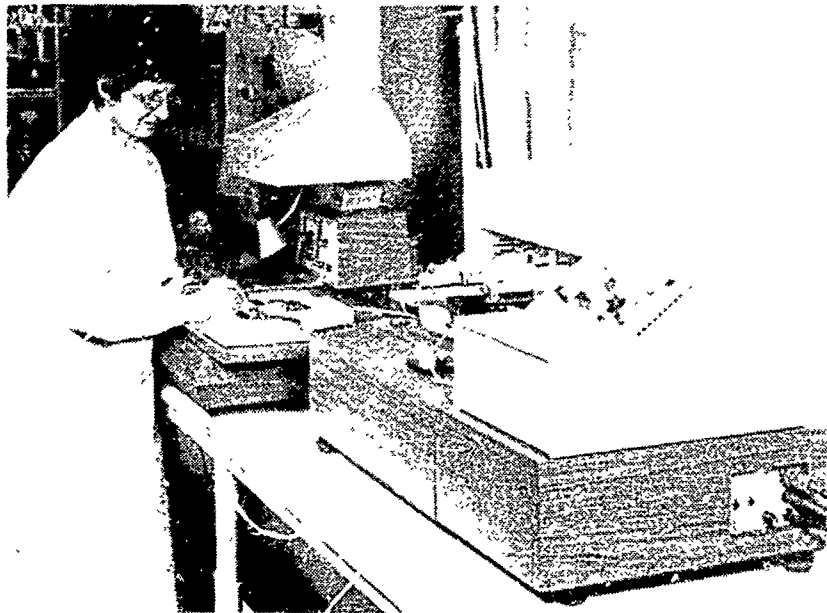


Figure 5. CHIP-ASSEMBLY-ROBOT

in the equipment's memory and on a magnetic tape cassette. The equipment operates automatically from its internal memory and the cassette used to store programs for future use. The X and Y of both the pick-up positions and the locate positions are programmable. In addition, this equipment permits the programming of angular placement of the component. Rotation is performed as the component is being transferred from the pickup to locate positions. The line operator only has to load and unload the four substrates and activate the start button.

A linear vibratory feeder (Figure 6) moves the parallel rows of chips to a reference position for pickup with the vacuum chuck. After a chip is picked up, the other chips in its row move forward so that another chip is in the referenced position. Held in an easily removable slotted tray, the chips may be loaded manually, or they may be loaded automatically from a separate vibratory bowl feeder. In general, maximum manufacturing rates are achieved by populating substrates sequentially, thereby minimizing table transfer time. This operation is repeated for each successive row of active or passive chips until all chips are placed on the four substrates. In the demonstration run, 180 capacitor sets per hour were placed on ceramic substrates for the XM-734 multi-option fuze.

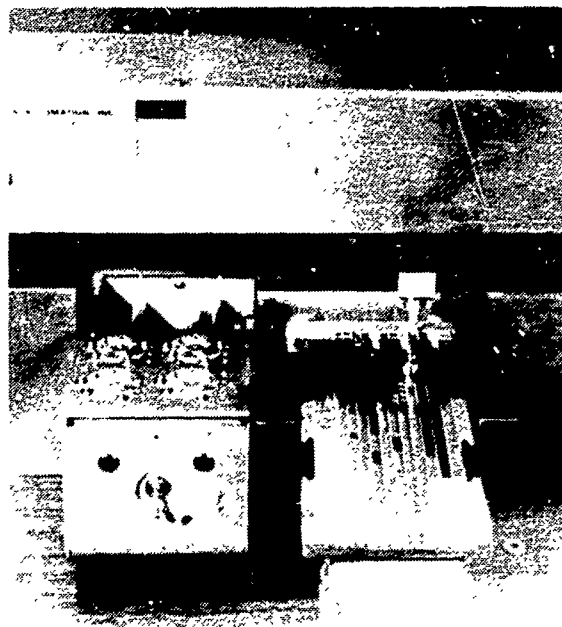


Figure 6. LINEAR VIBRATORY FEEDER

Wire bonding was demonstrated with an automatic wire bonder as shown in Figure 7. The machine bonding rate of this equipment is 3000 wires per hour. This bonder is a modified version of a commercially available thermal compression bonder.

Instead of a hard-wired ROM board, a Central Processing Unit (CPU), Figure 8, is used to store the operating program. The CPU not only provides more flexibility, it also provides much more capability. The dual-in-line magazine load and unload system was replaced by a numerically controlled X-Y table which, upon command from the CPU, moves the table from chip to chip. Finally, an ultrasonic head was added to replace the thermal compression bonding capability since TC bonding would impose serious limitations in ceramic microcircuit assembly.

To program the pad locations, the digitized information is converted by the use of a "canned program" from a standard Telex computer terminal to a CPU source tape and from this tape into the CPU.

Once the automated wire bonder is set up and programmed, the operator picks up the substrate and places it on the station. Automatically, the

equipment snuggler accurately registers the substrate by securely fastening it against a set of stops. Then the first chip is displayed on the video monitor. The operator aligns the lower left pad on this chip to a set of alignment lines on the video screen and depresses a button. All microelectronic connections are automatically wire bonded. Then the X-Y table brings the next chip into view on the monitor screen and at the work station. The sequences are repeated for all chips on the substrate. The operator then removes the wire-bonded substrate and replaces it with an unbonded substrate.

The speed of the system depends on (1) bond dwell time, (2) length of wire and chip location runs, (3) alignment time, (4) the accuracy of the die location and (5) the arrangement of the pad geometry. During the demonstration conducted, XM-734 ceramic microcircuits were wire bonded at a rate of forty (40) per hour. This rate included all loading and unloading of the substrates. With auto load and unload, one (1) operator would efficiently control three (3) automated bonders for a rate greater than 125 per hour.



Figure 7.
OPERATOR ALIGNING
CHIP ON
MULTI-CHIP AUTOMATIC
WIRE-BONDER



Figure 8.
LOADING PAPER TAPE
PROGRAM INTO
AUTO-BONDER
CENTRAL PROCESSING
UNIT (CPU)

Proposed High Volume Production Line

The techniques demonstrated in this contract have established the feasibility of a fully automated production line for the high volume manufacture of ceramic microcircuits. The proposed production line could be used as the base for the production of any military ceramic microcircuits.

The main features of the proposed production line are:

- . STANDARD SUBSTRATE SIZE - 4" x 4" for all circuits

The substrate size would be standard; the same automated handling equipment could be used for any circuit.

- . MULTIPLE-IMAGE PRINTING

The size, configuration, or both for a circuit would be made unique through laser scoring. Multiple-image printing would be used if the size of the circuit permits, thereby substantially increasing the circuit printing rate.

- . MAGAZINE HANDLING THROUGHOUT

All work transfer would take place from and to magazines. The operator would never directly handle any work in process. The operator would move only the magazines with batches of work.

- . LASER TRIMMING

For such a production line, laser trimming would obviously be used as it is over ten times faster than its abrasive counterpart.

- . AUTOMATIC ACCURATE WORK TRANSFER FROM STATION-TO-STATION

Work in process is automatically transferred from magazines to indexing conveyors. These conveyors automatically and accurately would move the work to and through the required operations.

- . PROGRAMMABLE AUTOMATIC WIRE BONDING

Programmable automatic wire bonders would reduce the time of microinterconnections.

- . MAGNETIC TAPE PROBE & DI-TAPE ATTACH

Semiconductor chips would be prepared for automatic assembly by probing the wafers. Chips transferred by category on adhesive-backed plastic strip similar to 8-mm movie film. The data required to subsequently sort by type would be stored on magnetic tape.

- . MAGAZINE STORAGE AT ALL MAJOR OPERATIONS

Work in process would be stored in magazines for effective lot and inventory control. This storage would allow easy correction of work-flow imbalance caused by occasional, unavoidable, random equipment downtime.

- . MODULAR CONSTRUCTION

Due to its modular nature, the line could be readjusted readily to produce a very wide range of hybrid circuits.

The proposed production line consists of four (4) main sections - substrate fabrication, passive component attachment, active component attachment, and wirebonding.

Substrate Fabrication

The automation of the substrate fabrication is rather obvious. Adding automatic unloading to the system demonstrated and described and laser trimming would establish a fully-automated substrate fabrication capability. The operators would only have to load and unload the magazines to their respective equipments.

Using multiple-image substrates substantially increases the manufacturing capacity. Two (2) of the ECOM ceramic microcircuits are presently being produced with multiple-image substrates. The Relay Driver uses a sixteen (16) image substrate, two (2) inches square and the Digital Stimulus Buffer, a five (5) image substrate, also two (2) inches square. The GVS-5 ceramic microcircuits are larger, more complex and are produced using single substrates. Using the standard substrate size of the proposed concept, these circuits would all be produced using a substrate whose outside dimensions would be four (4) inches square. With these standardized substrates, only the screens would have to be changed to produce any of these circuits with this printing/firing complex.

In Figure 9 are shown the resulting configurations for these five ECOM circuits. Any required holes would be punched out in the "green state", but to minimize breakage in handling, the laser-scored lines between circuits should be generated just before the circuits are separated. This four-inch configuration is planned for all the automated assembly described in this paper.

The salient features of this substrate fabrication concept are:

- . Standardized Substrate Size (4" X 4") - limited by printing definition.
- . Multiple-Image Printing - limited by size of substrate
- . Magazine Load and Unload.

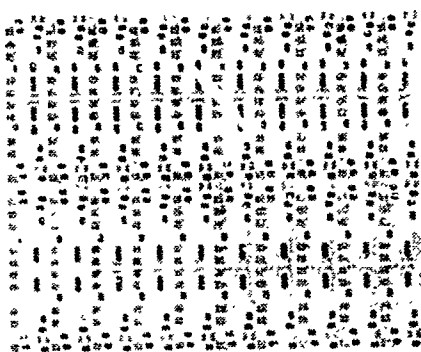
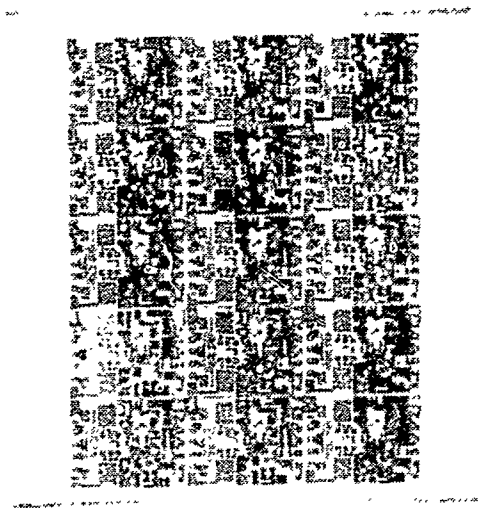
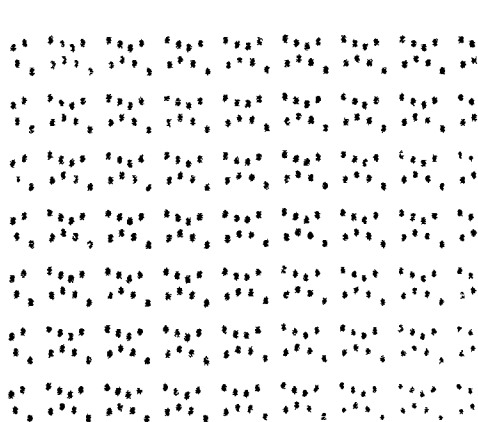
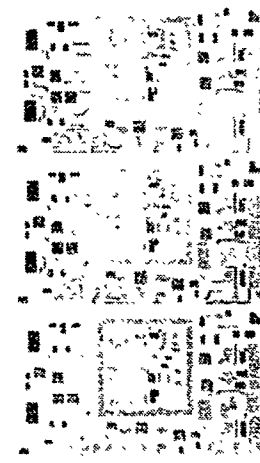
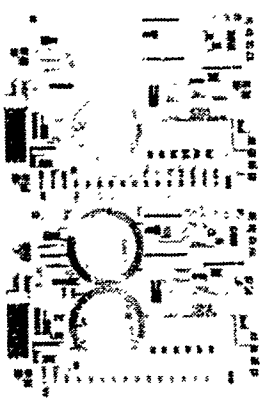
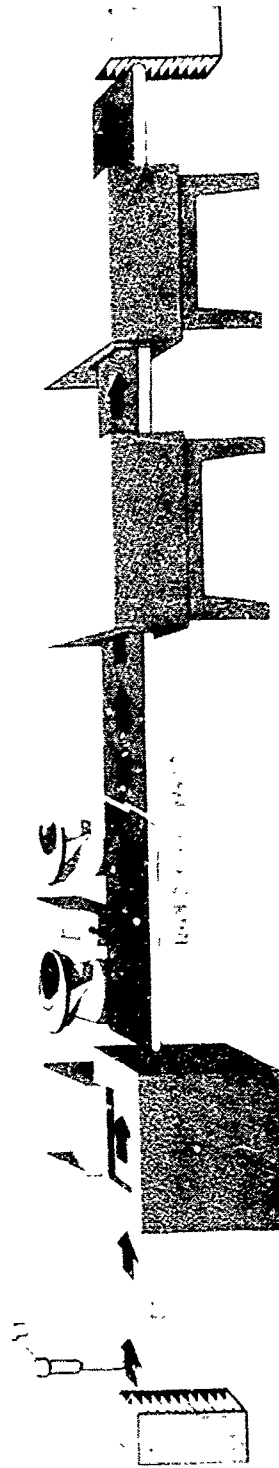


FIGURE 1 - MULTI-IMAGE SUBSTRATE

- TOP ROW - EQUATE
 LEFT - RELAY DRIVES
 MID - MEASUREMENTS BUFFER
 RIGHT - DIGITAL STIMULUS REF
 BOTTOM ROW - APPLIED



Passive Component Attach Module (PCAM)



Active Component Attach Module (ACAM)

Auto-Bonding System

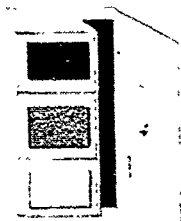
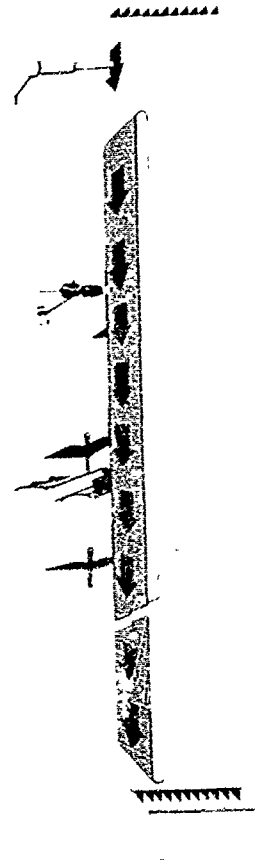
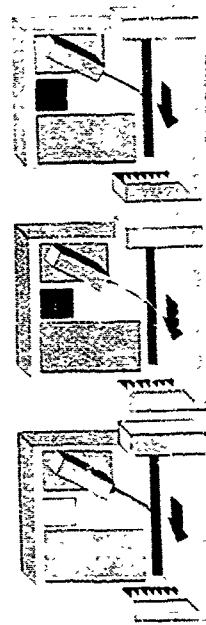


FIGURE 10. ARTIST'S CONCEPT - AUTOMATED HYBRID ASSEMBLY

- . Laser Trimming
- . No special tools or fixtures required to manufacture a wide range of circuits

Automated Assembly

Figure 10 is an artist's concept of the heart of the proposed production line the automated assembly. This section includes a passive component attachment module (PCAM), an active component attachment module (ACAM) and an automatic wire bonding system. The fact that this figure is an artist's concept should not delude the reader to construe that this production line is but a dream. Although this line is not established, all of its elements can be procured from a minimum of two (2) vendors.

Passive Component Attachment Module (PCAM)

An indexing conveyor or a Walking Beam Indexer transfers the substrates from the input to the output, stopping accurately at each station. This conveyor is mounted on an incrementing X-Y table which indexes all substrates in sequence from the first circuit to the last circuit on each substrate.

As in all previous operations, substrates are stored in magazines. At the output end, as components have been attached, substrates no longer can be stacked one on another, and a different type of magazine must be used from this point on. The magazine planned is similar to that shown in Figure 11, except designed for 4-inch square substrates and spaced one-fourth inch apart.

An auto-load screen printer prints solder paste at the first operation. This printer applies the paste to all circuits on the substrate, then transfers it to the indexing conveyor while the X-Y table is in its first location.

The passive components, chip capacitors, impact switch, etc., are attached to the substrates using vibratory bowl feeds and automatic pick-and-place stations. A conveyor furnace is used to reflow the solder paste. The work is then moved to a conveyor spray clean for flux removal, and then returned to magazines automatically

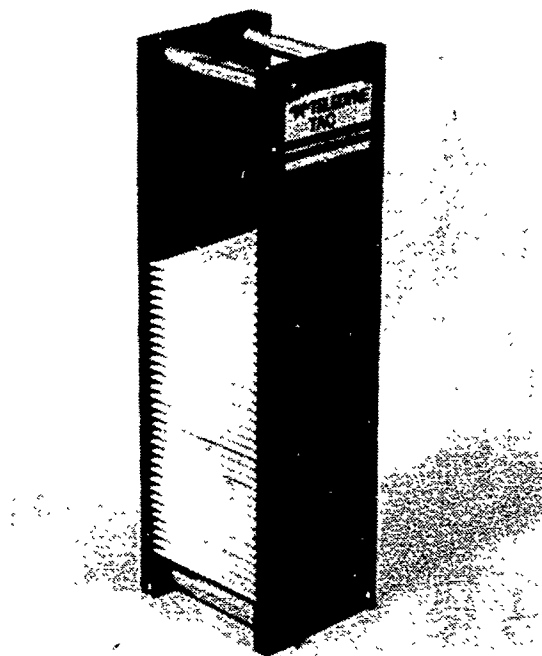


Figure 11. PARTITIONED MAGAZINE

The set-up of this module consists of:

- . Setting up proper screen for solder dispensing.
- . Introducing the proper increment in the X-Y table, i.e., center-to-center spacing of all circuits in the 4-inch square substrate.
- . Adjustment of pick-and-place station for appropriate component and location.
- . Bulk loading of the proper components into the bowl feeds.

The operator then only has to keep loading or unloading magazines. Substrates are transferred from the input magazine onto the indexing conveyor which moves the substrate along the line.

Active Component Attach Module (ACAM)

This module is very similar to the PCAM. The printer is replaced by a multi-nozzle epoxy dispenser and the vibratory bowl feeders are replaced by chip attachment stations (CAS). The use of epoxy eliminates the need for the spray flux removal station. Batch-curing of the epoxy while the work is in the magazine replaces conveyorized reflow.

The semiconductor chips are attached to the reels of the CAS's using a commercially available system. Using this concept:

- . semiconductor wafers are partially sawed but kept intact
- . The wafers are then affixed to a mylar membrane on a metal frame and the individual chips separated while maintaining physical location
- . using a probe-magnetic tape recorder system, the wafers are probed and the data for each chip stored on a magnetic-tape cassette
- . finally, another equipment accurately transfers the semiconductor chips from the mylar-wafer assembly onto adhesive-backed indexing tape. The magnetic tape cassette is used to transfer only the chips meeting the desired requirements onto the indexing tape.

At the ACAM, the tape is indexed to accurately locate the probed chips for pickup by a pick-and-place module. This is a common pick-and-place module, identical to that used to pick-and-place passive components but with a smaller vacuum pencil to accommodate the smaller semiconductor chips.

The production rate of these modules is governed by the time required for pick-and-place and the transfer of the substrate from station-to-station. The transfer from circuit-to-circuit within a substrate is concurrent with the return of the pick-and-place arm, thus does not add to the operation time. The pick-and-place cycle time is approximately 2 seconds, the substrate transfer time is approximately 3 seconds, and the X-Y table movement occurs in

parallel with the return of the pickup arm. Therefore the rate per hour is given by the following equation:

$$\text{Assembly Rate (ccts/hr)} = \frac{3600}{2 + 3/N_C}$$

where: N_C is the number of circuits per substrate

This relationship is relatively insensitive to the number of circuits per substrate. The substrate for the GVS-5 Range Counter contains only 2 circuits and thus its rate would be the lowest - 1028 ccts/hr. On the other hand, the EQUATE Relay Driver with its 56 circuits per substrate could be produced at a rate of 1753 ccts/hr.

All of these components, indexing conveyor, X-Y table, magazine load and unload, printer, etc., are available from many of the known hybrid and semiconductor manufacturing equipment vendors.

Wire Bonding System

The most time-consuming and, therefore, costliest operation in the manufacture of hybrids is wire bonding. Full automation greatly reduces this cost. In the proposed production line, a wire bonding system will consist of three wire bonders and loaders/unloaders coupled to a common console so that one operator can effectively keep all three bonders operating. The work is automatically transferred from the magazine to the work station, and each chip is sequentially displayed on the appropriate video monitor. The operator only has to finally align the displayed chip and activate the bonder to automatically make all bonds on the aligned chip. While two bonders are operating, the operator aligns the chips on the third. A second operator loads and unloads magazines and can readily maintain a group of modules. One module can produce 150 XM-734 hybrid microcircuits per hour.

A more detailed description of the operation of this module is listed below:

- (1) Magazines are loaded to each bonder (if several modules are in use, an operator could be assigned to feed all bonders).
- (2) Substrates are automatically transferred to the bond station and chip #1 of circuit #1 is presented on the television monitor of bonder #1.
- (3) The operator performs final alignment of this chip, then turns over the wire bonding to the machine.
- (4) The operator then repeats step 3 for bonders #2 and #3.
- (5) After a chip is bonded, the machine automatically moves to locate the next chip into bonding location and television view. The operator then repeats Steps (3) and (4).

- (6) After the bonding on a substrate is completed, the substrate is automatically transferred to an empty magazine and a new substrate to the bond station.

The rate of such a module is dependent on number of wires per circuit (W_c), number of chips requiring alignment per circuit (C_c) (chips with large bonding pads do not require alignment), number of circuits per substrate (C_s), the substrate transfer time magazine-to-bond station (T_{mb}), bond station to magazine (T_{bm}), total distance chip-to-chip in one circuit in inches (D_c), the table travel speed (S_t), the chip alignment time (T_a), wire bond time (T_b), and the number of bonders controlled by one operator (N_b).

The approximate number of circuits an operator can produce per hour with this type of module is given by the following equation:

$$\text{Rate (ccts/hr)} \approx \frac{N_b \times 3600 \text{ (sec/hour)}}{\frac{T_{mb} + T_{bm} + \frac{D_c}{S_t} + T_a C_c + T_b W_c}{C_s}}$$

The typical labor and machine time for these elements are listed below:

T_{mb} - Transfer time magazine-to-bond station - 2 sec.

T_{bm} - Transfer time bond station-to-magazine - 2 sec.

S_t - Table travel speed - 2 inches/sec.

T_a - Ave. chip alignment - sec.

T_b - Wire bond time - 1 sec.

By inserting these values in the above equation, the wire bond rate equation, in circuits per hour, reduces to,

$$\text{Rate (ccts/hr)} = \frac{(3 \times 3600)}{\frac{4}{C_s} + D_c + 2C_c + W_c}$$

The circuit variables and bond rate for the EQUATE and GVS-5 wire bonded circuits are listed in Table I.

TABLE I. AUTO WIRE BONDING VARIABLES & RATES

	Circuit Variables				Wire Bond Rate
	D _C	C _S	C _C	W _C	
<u>EQUATE</u>					
Relay Driver	1.2	56	9	62	134
Measurements Buffer	2.5	9	10	40	174
<u>GVS-5</u>					
Video Amplifier	3.5	3	15	50	130
Range Counter	1.5	2	6	98	95

The automatic wire bonder demonstrated in the ECOM contract was the first automated bonder capable of bonding multichips as required for the manufacture of ceramic microcircuits. This bonder was procured in 1974 and since then, many equipment manufacturers have announced and are marketing multi-chip automated wire bonders.

In Figure 12 is shown a two-station complex of a more recent vintage computer-controlled automatic wire bonder. This bonder can be programmed to bond up to 600 wires on any number of chips. It is programmed by bonding one circuit while inserting the bond positions in the CPU memory. This is a very similar concept as is used in the Chip Robot. Programs can be stored on paper tape or floppy disc.

Figure 13 shows the control panel. This control panel is used for recalling existing programs, loading programs from tape or disc, generating programs, bond repair and even for self diagnosis of the electronics of this system. This supplier has developed and will provide on a floppy disc a self-diagnostic program which will identify the system failure down to board level. The malfunctioning board can be replaced and operation quickly restored.

These bonders are shown with microscopes for alignment. However, for an automated system, three bonders would be coupled with automatic load and unload and TV monitors used for alignment.

AUTOMATIC WIRE BONDING IS HERE TO STAY AND WILL BE USED MORE AND MORE TO REDUCE LABOR COST.



Figure 12. DUAL AUTO-WIRE BONDER COMPLEX

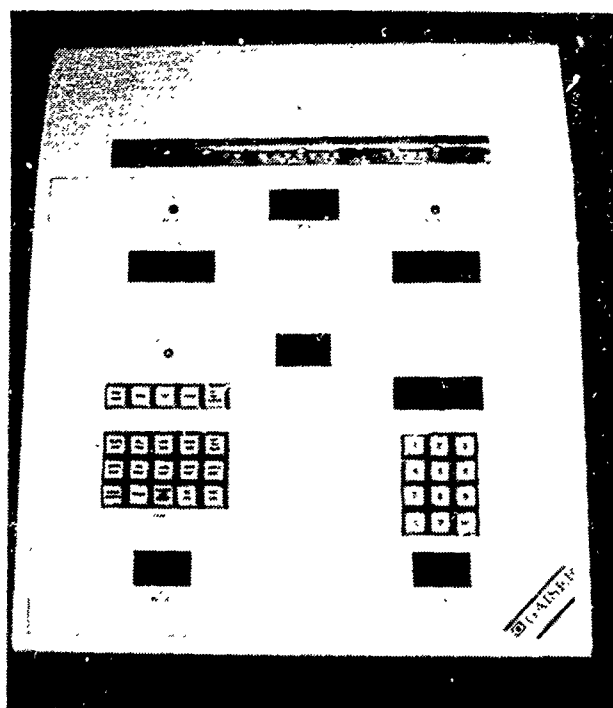


Figure 13. AUTO-BONDER CONTROL PANEL

Economics of Automation

Now let us look at the savings afforded by the automation of these three major ceramic microcircuit fabrication operations. The output for manual and automated fabrication for each of these major operations and for the ECOM circuits are listed in Table II. The output is in shippable units per labor hour.

TABLE II. MANUAL vs AUTOMATIC CERAMIC MICROCIRCUIT ASSEMBLY

Operation	Approx. Output/Labor Hours								Approx. Added Capitalization* (\$K)
	Manual				Automatic				
	RD	MB	VA	EC	RD	MB	VA	RC	
Substrate Fabrication	25	5	3.3	4	200	80	40	33	(36)
Component Attach	11	5	2.2	4.5	350	125	80	111	460
Wire Bond	4.3	3.3	2.7	1.7	43	27	23	19	(20)
Total **	2.7	1.4	.9	.95	32	17	12	11	404

* Equal mix of circuits

**Labor hours for the sum of all three (3) operations

These figures were computed using current yields. It is expected that with automation would come improvement in yields as well as rate, but this factor is not included in these computations. As can be seen readily, automation increases the output of these three major operations by approximately 11 to 1.

To gain a better appreciation of this automation, let us convert to savings in dollars per circuit. To perform these operations on the average circuit requires .67 hour of labor with manual equipment, and only .06 hour with automatic equipment. A reasonable average hourly rate range including overhead, G&A and profit, is \$6.00 to \$25.00. Therefore, a savings of \$3.66 to \$15.25 per circuit. This will represent many millions in savings per year as inevitably more and more ceramic microcircuits will be used by the military.

SUMMARY

This contract has demonstrated that automated techniques can replace human-dependent operations by more predictable and much faster machine repeatable processes. This will greatly reduce the cost of ceramic microcircuits through the reduction of the required labor resulting from automation and higher yields made possible by machine reproducible processing.

Manufacturers of computers and automotive electronics have long recognized the value of automatically assembled ceramic microcircuits and use automated lines to produce enormous quantities for their use. These are dedicated production lines, producing a very large volume of fixed configuration.

Most military needs do not require the high volume necessary to justify dedicated lines of this type. Because of the versatility of the concept presented in this paper, the establishment of such a line would make available the benefits of automation for the manufacture of military ceramic microcircuits. Its availability would foster accelerated application of ceramic microcircuits for military use by lowering their costs.

ACKNOWLEDGMENTS

Space does not permit acknowledging all individuals who contributed to this study and concept, but we must at least acknowledge the organizations who contributed significantly. Beginning, naturally, with our parent organizations, ECOM and RCA-ASD who respectively supported and accomplished this contract (DAAB 05-73-C-2039). We must also acknowledge Harry Diamond Laboratories for technical guidance, Teledyne-Tac, AMI, GCA, Gaiser and Dixon who supplied some of the demonstration equipment and contributed substantially in defining the automation concept.

BEAM LEAD DEVICE PROCESSING IMPROVEMENTS

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ABSTRACT

Motorola combines the advantages of beam lead sealed-junction technology with the yield enhancement and silicon real estate advantages of a master mask technology to produce a state-of-the-art family of 54LS IC's.

Refinements have been made to the titanium-platinum-gold beam lead metallization system such as a modified sealed junction, sputter etching and chemically vapor deposited glass passivation over the surface of the die.

Handling and testing of beam lead chips has long presented problems; Motorola has participated in the development of beam lead chip carriers in support of the C-4 program. Plans are being made to expand these capabilities to the standard products required on ECOM's Manufacturing Methods and Technology program.

INTRODUCTION

The Federal High Reliability Products group of Motorola is presently developing beam lead devices in support of four programs: (1) Manufacturing Methods and Technology with ECOM, (2) Lockheed's C-4, (3) General Electric's MK-500 and General Electric's MK-12A. It should be pointed out that in the latter two cases, all of the devices are dielectrically isolated for radiation hardening capabilities.

Process improvements on these programs have made significant contributions in yield, reliability and ultimately lower cost.

The purpose of the Beam Lead Device Manufacturing Methods and Technology program is as follows:

1. Improve yields - From wafer start to die shipments.
 - (a) Discretes - 20 percent
 - (b) IC's - 10 percent
 - (c) 60 Gate Array - 5 percent
2. Availability of part types.
3. Lower cost.

Tables I and II provide lists of all of the beam lead devices under development at Motorola, both junction isolated and dielectrically isolated.

MASTER MASK

Two of the primary reasons for yield loss in LSI circuits are photoresist generated defects, (pin holes, etc.) and misalignment. The misalignment problem is two-fold: with wide tolerances, silicon real estate is used rapidly; with tight tolerances, misalignment loss is excessive.

To simultaneously solve these problems, a process using a single master mask was developed which largely rectifies both of these problems.

This master mask concept combines the isolation, collector, resistor and base diffusion on a single mask. Each aperture is dimensionally exact and alignment is, of course, exact also.

The starting material consists of the P-substrate into which an N+ buried layer has been added. The N-epi layer is covered with an oxide of 3000 Å followed by a nitride layer of 2000 Å.

The first photoresist step is the master mask into the nitride layer only. The nitride layer now contains the dimension and alignment information to be used for the next several diffusion steps.

Oversize mask layers of each diffusion step are now sequentially applied to the slice. Since the layer is oversize, alignment error is unimportant. True alignment and aperture size are still defined

MM&T BEAM LEAD DEVICE LIST

DEVICE	FUNCTION	DEVICE	FUNCTION
1N746	3.3V Z	5405	HEX INV O.C.
1N748	3.9V Z	5410	TRIP 3 NAND
1N5314	5.14 ma CURRENT SOURCE REG.	5440	DUAL 4 NAND
2N2484	NPN HIGH GAIN (100)	5473	DUAL JK
2N2907	PNP SWITCH AND AMPLIFIER	54LS04	HEX INV
2N3251	PNP HIGH SPEED SWITCH (200 ns)	54LS08	QUAD 2 AND
2N3467	PNP 1 AMP CORE DRIVER	54LS21	DUAL 4 AND
2N3501	NPN HIGH VOLTAGE (150V)	54LS32	QUAD 2 OR
2N3635	PNP HIGH VOLTAGE (140V)	54LS73	DUAL JK
2N3639	PNP HIGH SPEED SWITCH (20 ns)	54LS74	DUAL D
2N3725	NPN 1 AMP CORE DRIVER	54LS86	QUAD 2 EX OR
2N3960	NPN RF	54LS138	DECODE-DEMUX
2N4260	PNP RF	54LS193	UP-DOWN COUNTER
2N5115	P CHAN JFET	54LS194	4 BIT S.R.
RA108	60 GATE ARRAY	54LS196	DECADE COUNTER
5400	QUAD 2 NAND	54LS197	BINARY COUNTER
5401	QUAD 2 NAND O.C.	54LS253	DUAL 4-1 MUX
5404	HEX INV		

TABLE I.

**NAVY-LOCKHEED C-4 / NAVY-G.E. MK-500 /
AIR FORCE-G.E. MK-12A
DIELECTRICALLY ISOLATED BEAM LEAD DEVICES**

DEVICE	EQUIV.	FUNCTION	SYSTEM USAGE		
			C-4 LMSC	MK500 G.E.	MK12A G.E.
811	54LS00	QUAD 2-INPUT POS. NAND GATE	✓	✓	✓
812	54LS20	DUAL 4-INPUT POS. NAND GATE	✓	✓	✓
476	54LS01	QUAD 2-INPUT POS. NAND GATE (OPEN COLLECTOR)			✓
813	54LS76	DUAL J.K. FLIP FLOP	✓	✓	✓
814	741	OP. AMP.	✓		
815	54LS253	DUAL 4-TO-1 DATA LINE SELECTOR & MULTIPLEXER	✓	✓	
816	54LS155	DUAL 2-TO-4 DECODER DEMULTIPLEXER	✓	✓	
817	SIMILAR TO 54170	4 x 4 REGISTER FILE	✓	✓	
818	SIMILAR TO 54LS181	A.L.U.	✓		
819	SIMILAR TO 54187	256 x 4 ROM.	✓		
820	54LS193	UP/DOWN COUNTER	✓	✓	
821	54LS194	4-BIT SHIFT REGISTER	✓	✓	
822	NONE	R/W 64 x 1 MEMORY RAM	✓		
119	NONE	QUAD J-FET DRIVER SWITCH	✓	✓	
6205	5400	QUAD 2-INPUT NAND GATE		✓	
6206	5401	QUAD 2-INPUT NAND GATE (OPEN COLLECTOR)		✓	

TABLE II.

by the master mask cut in the nitride. Each oversize mask merely opens the appropriate window in the photoresist, and the nitride acts as a mask to etch the aperture in the underlying oxide. Note that pinhole protection is guaranteed. A pinhole would require coincidence on both the master mask and a sequential mask to penetrate both the nitride and the underlying oxide layers.

Each in turn, the photoresists and diffusions, are carried out, each through the master mask, up through the emitter mask. At this point, the nitride is stripped away and a new layer of nitride is deposited. This layer does not have the master mask cuts in it and, therefore, acts as a seal for these junctions.

Next, the junction seal and aperture photoresists are accomplished and the wafer continues through the metallization steps as covered next.

Yields with this technique are superior to conventional technology with more consistent slice-to-slice uniformity.

Four of the processing steps are shown in the cross-sectional drawing in Figure 1.

METALLIZATION PROCESS IMPROVEMENTS

The challenging yield and reliability objectives inherent to the MM&T beam lead program required a complete reassessment of process and equipment capabilities during the early stages of the program. Of the three primary technical areas involved in the fabrication of wafers, i.e. diffusion, metals and photochemical, only the diffusion and metals operations were specifically targeted for process improvements. In the diffusion area, the previously described master mask concept accounted for major improvements in device yields and performance. In the metallization area, however, the contribution was even more dramatic. Of the various metals processes evaluated, one of the greatest concerns involved the deposition of platinum to form platinum silicide ohmic contact for the trimetal (Titanium-Platinum-Gold) beam lead system. Prior to this study, the wafer rejects at this operation were often in excess of 25 percent as a result of incomplete chemical cleaning of the silicon surface. The fact that it is virtually impossible to guarantee a clean surface using only chemical processes led to the development and application of a highly controlled sputter etching technique. This process reproducibly removes several hundred angstroms of oxides and/or nitrides immediately prior to the sputter deposition of pure platinum. The value gained through the improved technique and process control has resulted in the achievement of sustained manufacturing yields greater than 99 percent during the first year of this operation.

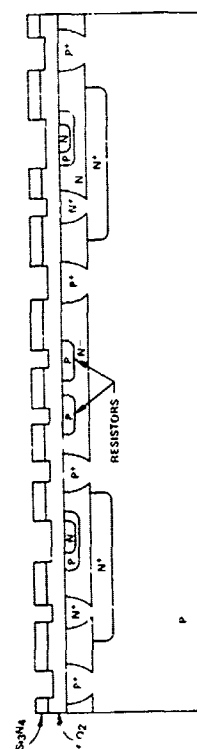
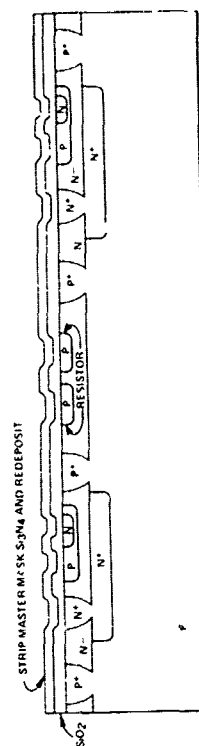
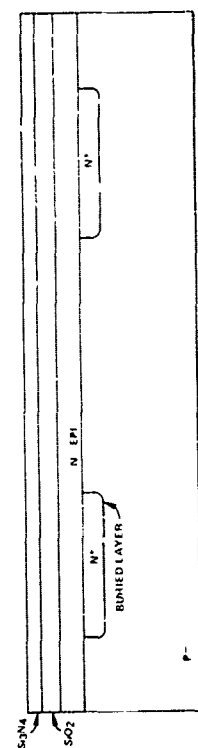
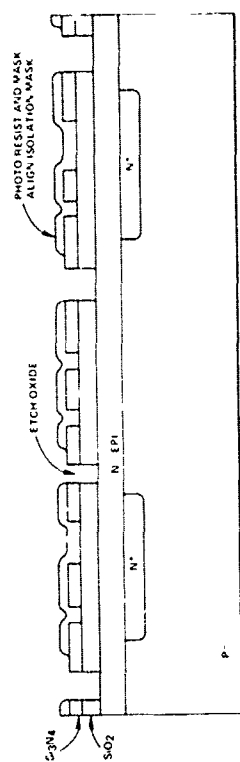


Figure 1 Master Mask Processing

A cross-section drawing of the metallization system with final passivation is shown in Figure 2.

BEAM LEAD CHIP CARRIERS

Handling and testing of beam lead chips has long presented problems. The inability to adequately perform the required AC tests at wafer probe, in addition to high and low temperature extreme testing, led to the development of a beam lead chip carrier.

There are several design approaches to manufacturing chip carriers; however a carrier assembly essentially is comprised of five components. Referring to Figure 3, the carrier (4) is used almost universally, i.e. with all sizes of chips. Only on very large chips would a larger carrier be required. The metallized substrate (3) is different for different sized chips and beam outs. The cavity, in which the chip (2) is placed, is designed for specific chip sizes. The glass cover (1) is compressed against the chip by the spring (5) thereby ensuring good electrical contact.

A photograph of an assembled chip carrier is shown in Figure 4.

A photomicrograph of a device beam bonded in a flatpack is shown in Figure 5. Although this same device had previously been assembled in a carrier, no abnormal beam deformation was observed.

The last photograph (Figure 6) shows our chip carrier loader, which is still under development. The chip carrier loader is designed to automatically load a beam lead chip into a carrier base and complete the assembly of the carrier. The purpose of the loader is to economically reduce the die handling requirements and thus decrease the percentage of die rejects due to physical damage.

A chip carrier unloader has been designed by Lockheed to automatically disassemble the carrier and present the die in a precise pickup location to the K. and S. automatic beam lead bonder. The purpose of the unloader is to automate the die handling, locating and pickup procedure for bonding.

The advantages of the chip carrier assembly system are as follows:

BEAM LEAD CHIP CARRIER ADVANTAGES

1. Component parts are reusable except for the spring.
2. Carriers are stackable and mechanically compatible with automatic loading and unloading equipment used for testing devices in flatpacks.

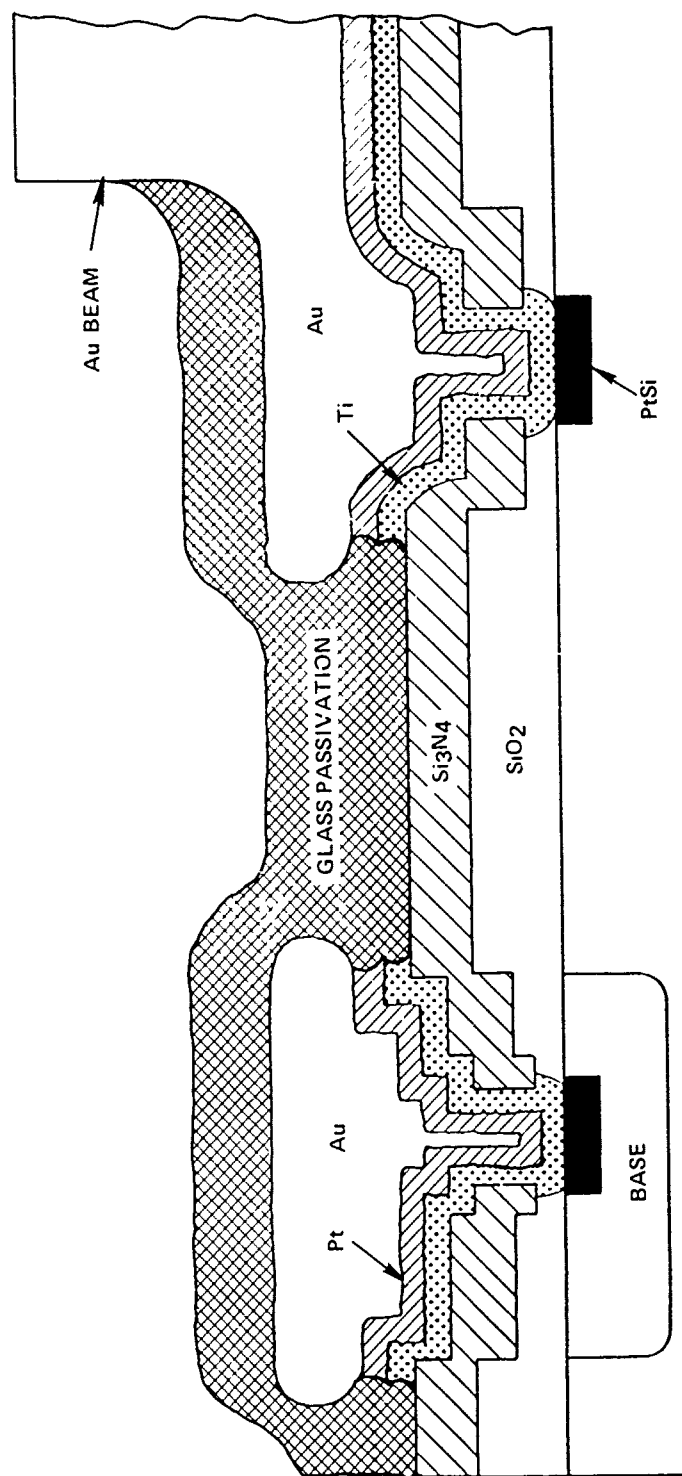
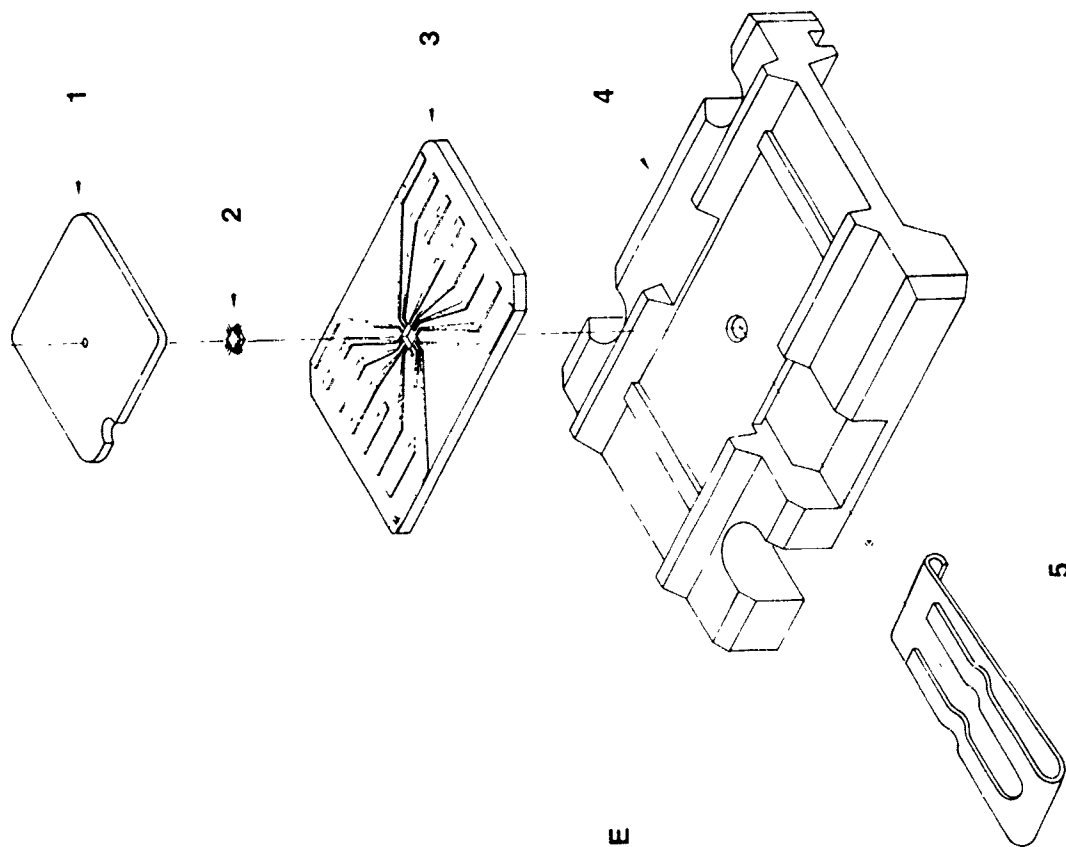
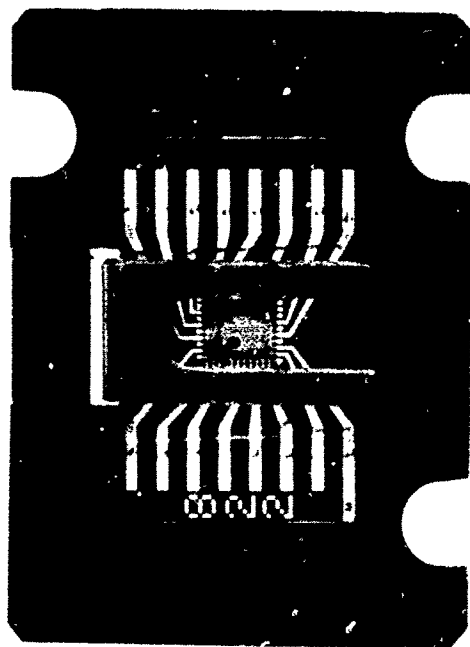


Figure 2 - Glass Deposition

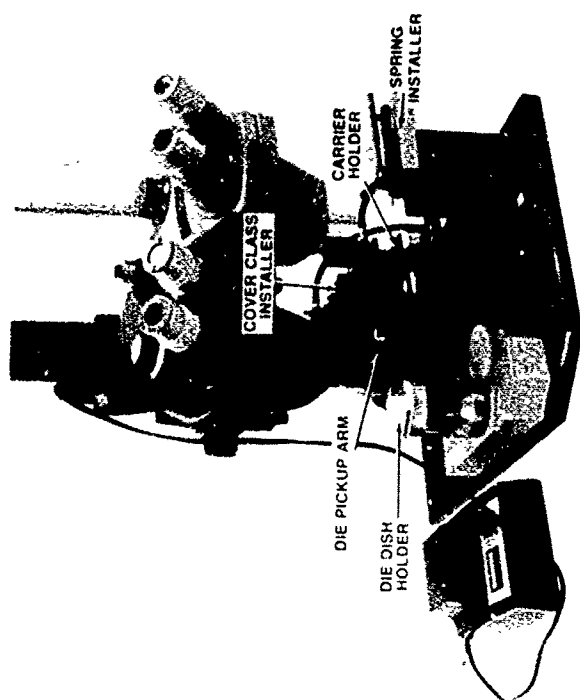


1. COVER GLASS
2. BEAM LEAD DIE
3. SUBSTRATE
4. CARRIER
5. SPRING

Figure 3 - Beam Lead Chip Carrier Assembly

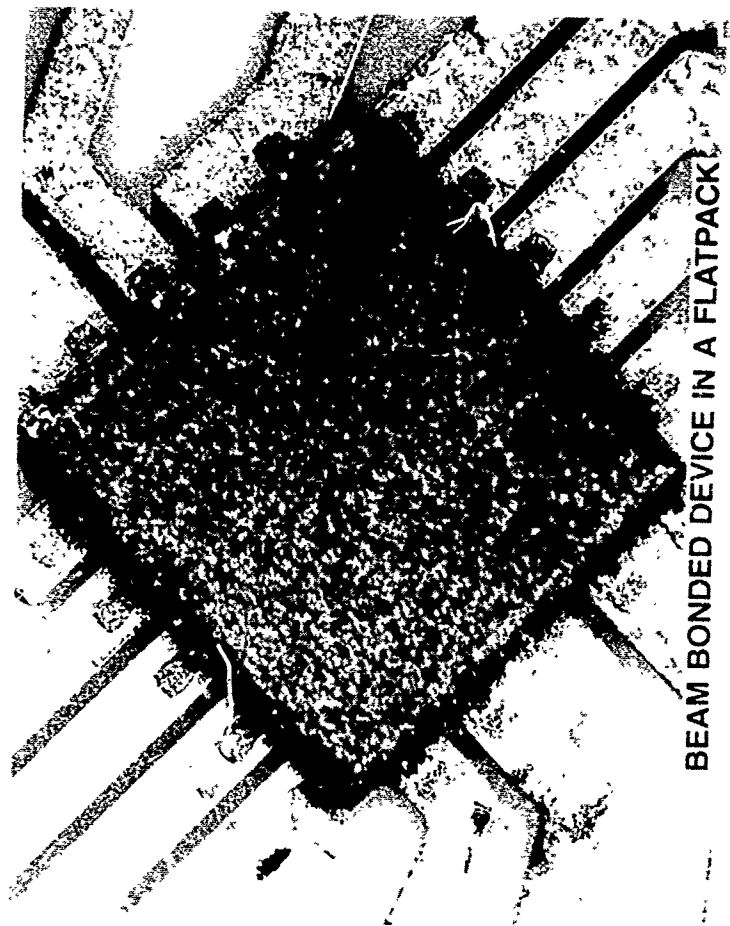


ASSEMBLED CHIP CARRIER



CHIP CARRIER LOADER

Figure 4



BEAM BONDED DEVICE IN A FLATPACK

Figure 6

3. It is now possible to precondition beam lead devices, i.e., AC/DC, burn-in, high temperature reverse bias (HTRB), Gp's A, B and C, etc.
4. Storage without concern of lead deformation.
5. Provides the capability of customers to screen beam lead devices electrically, environmentally and visually.
6. Reliability enhanced by less handling.
7. Better yields since devices can be AC/DC tested at room, high and low temperatures. There is no need to impose stringent guardband tolerances at wafer probe since these tests may now be performed.

COMPUTER AIDED MANUFACTURING IN BEAM LEAD DEVICE BONDING

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ABSTRACT

This paper describes a fully automatic facility used for bonding beam lead integrated circuit devices to thin film ceramic circuit packs.* The facility has proved to be a prime example of how effectively computer aided manufacturing techniques can be applied in the assembly shop. It makes extensive use of the high-speed processing power of computers in almost every phase of its operation: machine control, process control and the generation of data files which are used to run the machine. Rudimentary image processing is used for micropositioning devices and sites.

INTRODUCTION

Methods of production can be broadly described as process manufacturing, mass production and batch production.³ An example of process manufacturing would be steel mills or certain chemical manufacturing plants where a continuous process is controlled by rather straightforward sensor feedback controls. Such systems have been in use for a long period of time.

Mass production is the most common mode of manufacturing technique and is exemplified by many piece part or product assembly lines. Manipulation of such mass producing methods is usually obtained by designing control machinery dedicated to perform fixed repeat operations. A good example of this would be a turret machine having several work stations. Advantages of using a computer in such applications would be very minimal since very little flexibility is required.

In batch production the machinery has to be more flexible. The facility may be set up to produce a particular product for a certain lot size; then it may have to be reconfigured to produce a different product. This type of operation may require sophisticated scheduling and control of facilities and may demand more flexibility than that required in the other manufacturing modes.

The type of product that the bonding facility was designed to assemble fits perfectly the description of batch manufacturing. A number of factors played a key role in making the decision to engineer such a facility, probably the most important being the nature of the product itself.

New Bell System Electronic Systems use standardized logic circuit packs (figure 1). The circuit pack consists of a ceramic substrate with gold thin film metallization to which beam lead devices are thermocompression bonded. The integrated circuit device is 50 mils square, tip to tip, and has 28 beam leads, each of which is 2 mils wide by 5 mils long and spaced on 5 mil centers† There are many different electrical device codes

*Figure 7

†Figure 6

Ceramic Circuit Pack

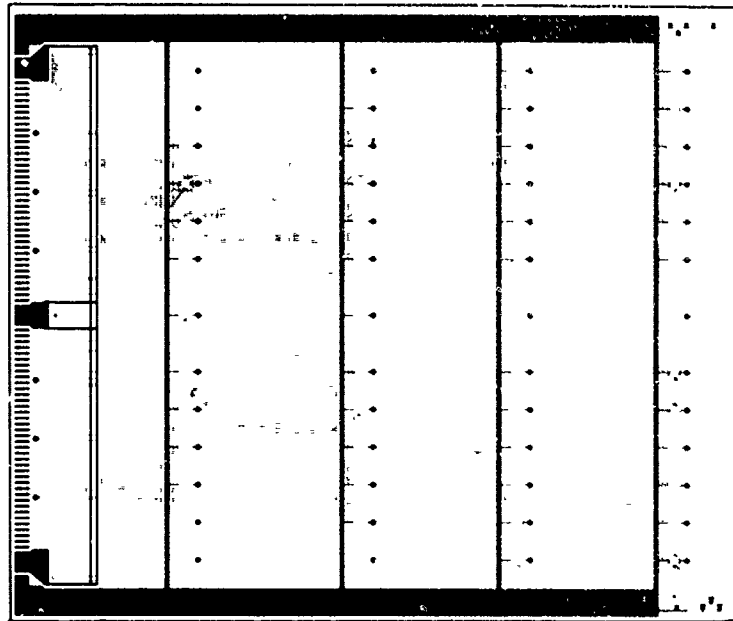


FIGURE 1

of this same size that are bonded to the ceramic substrate. The substrate has 52 possible dedicated positions for device placement. The conductor pads in the bonding area are nominally 3 mils wide. Overall device to bond site centerline accuracy of $\pm .3$ mil must be maintained. Hundreds of hybrid circuit pack codes have been designed by using combinations of the electrical device codes in varying quantities on ceramic substrates. There are currently over 1000 ceramic circuit pack codes with 12 to as many as 52 devices being assembled. Production batch sizes for this product line range from 1 per substrate code to over several hundred per code on a weekly basis.

One fact is quite clear from the foregoing description of the product; the microminiature size of the parts, enormous number of various different circuit pack codes and wide variation in the batch sizes make manual device bonding an undesirable and expensive proposition. Microscopic piece part assembly is subject to human variability or error, particularly when the assembly sequence is completely random. These errors have to be diagnosed through logic testing and repaired and this naturally adds considerably to the cost of the product.

The factors that proved the manual assembly techniques to be unwieldy, however, were the very factors that strongly advocated implementation of computer aided assembly techniques. Programmable operations offered flexibility in assembling a variety of product. This capability, combined with complete computer based scheduling and allocation of product resulted in a major increase in productivity, especially in the important area of batch production and testing.

The following requirements may be defined for the design of this facility:

1. Ability to store devices and select those required for bonding to a substrate
2. Flexible and with enough memory so as to assemble a large number of circuit pack codes
3. Handle, with equal ease, small or large batch sizes of individual pack codes
4. Ability to assemble all ceramics with minimal overall handling
5. Access, capture and microposition devices and sites repeatably at a high rate of speed

A Digital Equipment Corporation PDP8/E minicomputer controls all the machine sequencing and timing functions, matches proper device code to proper bonding site location, and coupled with a custom pattern alignment system, governs the micropositioning of devices and substrate bonding sites to centerline accuracies of $\pm .3$ mil. The facility has been developed to bond up to 9 electrical device codes in any combination. The facility is flexible enough to assemble a large number of different circuit pack codes in either small or large quantities without experiencing any appreciable loss in the bonding rate efficiency or quality of the product.

MACHINE DESCRIPTION

Figure 2 is a mechanical schematic of the bonding machine. The machine positioning system consists of a device pick-up station, bonding station and a transport system which carries the bonding head back and forth between these two stations. Two highly repeatable end points within $\pm .000050$ " are obtained by using Linear Variable Differential Transformers (LVDT) as position sensors.

The device pick-up station has a 9 position rotary carousel unit, mounted onto an X, Y stage which is mounted on a lower rotary stage. The centerline of the lower rotary stage is coincident with the centerline of the field of view of a TV camera and also with the centerline of the pick-up/bonding tool. This configuration allows for rotational correction without introducing translational errors during micropositioning. Each tray carries a 20×20 array of a code of devices. The devices are within ± 10 mils and $\pm 12^\circ$ of their theoretical true position. The devices in the array are located on 100 mil centers.

The bond side station has a patented substrate support mechanism and heating system mounted on X, Y stages which are mounted onto a lower rotary stage. There again, the centerline relationship of lower rotary, field of view of the TV camera and the pick-up/bonding tool holds true.

All the linear translation stages index 0.05 mils per step at speeds in excess of 13000 steps per second. The rotary stages index 6 arc minutes per step at 200-500 steps per second.

SCAN SYSTEM

The scanning system consists of two independent modular units, one for the pick-up side and one for the bonding side. Each unit is composed of a closed circuit television camera with a magnifying objective lens and a moveable mirror angled at 45° to permit straight down viewing and illumination of the object. Magnification onto the TV camera target is 3X on the bond side and 4.7X on the pick-up side.

Each camera employs a one inch silicon target vidicon image sensor. Any point within the camera's field of view can be represented by a pair of delay intervals from the vertical and horizontal synchronizing pulses. This direct time versus distance relationship can be used to delineate spatial areas of interest, called zones, within the field of view. These electronically synthesized zones are positioned and shaped so as to define a series of regions of interest which correspond to key features of the device or the bonding site to be positioned. The incoming video signal is processed and then combined with zone signals to obtain time functions of the spatial overlap of the zones and the processed video signal. This information is used in two ways; it may be time-integrated to find the area of spatial overlap, or it may be applied to storage elements for presence detection. Referring to figure 3, integrals in various zones A thru I are compared to decide how far and in which direction the device should be moved in order to capture it for the final micropositioning. This concludes the first phase of the scanning and cursory positioning and is under hardware control.

Auto Bonder Schematic

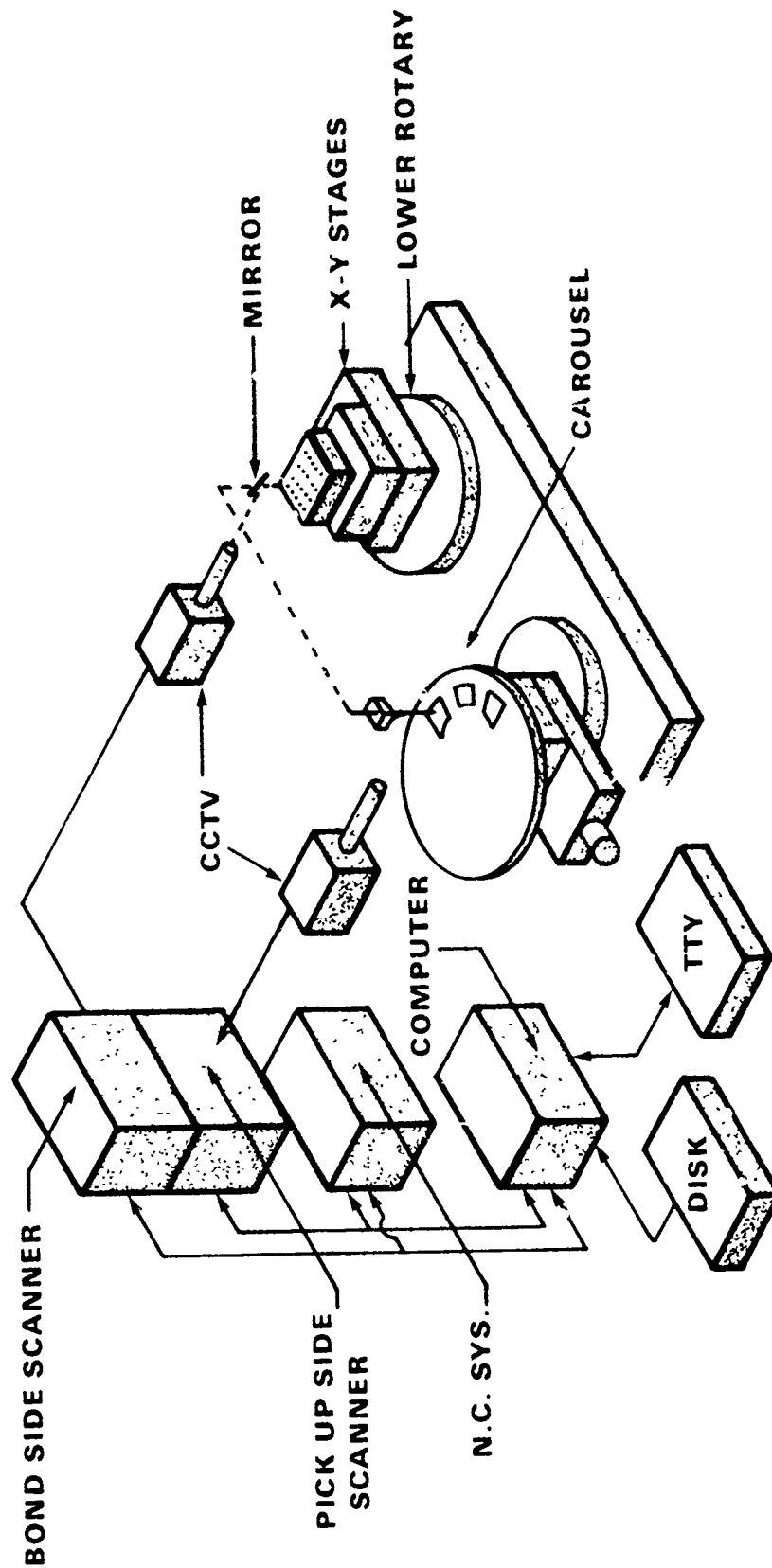


FIGURE 2

Pickup Side Micropositioning and Check Zone Group

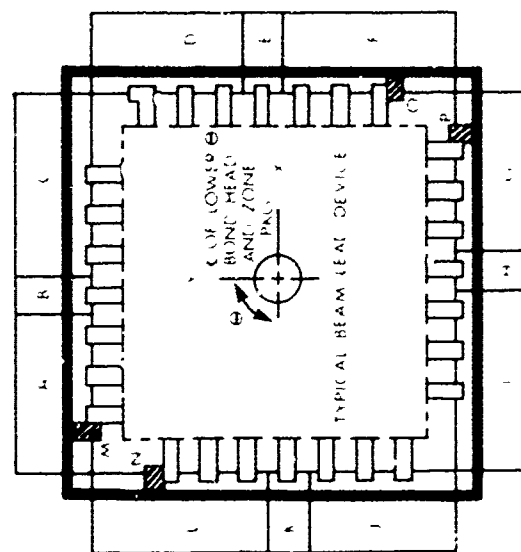


FIGURE 3

A set of 4 corner zones M, N, O and P, is used to sense critical edges of 4 corner beam leads. An iterative positioning algorithm is performed, through the computer, which moves the device and examines the contents of the associated storage elements. By making a series of these measurements, it is possible to compute the required X, Y and θ corrections for precise centering. This constitutes the second phase of scanning and micropositioning and is under computer control.

Having described various elements of the machine let us turn our attention back to the attributes of the computer as a central entity tying these elements together.

COMPUTER FUNCTIONS

The computer functions can be categorized into three major areas, namely, machine control, process control, and data generation. The control software is basically an assembly of function module programs that initiate various actions such as moving pickup or bond tables, moving mirrors or moving the transport. The control software performs these various actions in an asynchronous mode and it also keeps track of the current machine status on a per cycle basis. This method of operation dynamically allows for maximum machine speed as various parameters, such as access time for the next device or the next site, or the time to position the device or site, change continually from one cycle to the other. Although asynchronous in operation, a definite degree of synchronization has to be maintained. For instance scanning and positioning of the device will not be initiated unless the tables have settled at the new position and the pickup mirror is in the "lookdown" position. A pickup stroke will not be initiated unless positioning of the device is successfully completed and the mirror is cleared. This is accomplished through a device polling routine. Each function module is assigned a software event flag. As soon as action initiated by a certain function module is complete, its event flag is set. In between the execution of various function modules the processor scans these event flags and depending upon their state initiates the next action.

The natural synchronization requirements of the function modules combined with the disparity between the time required to initiate the action and the time required to complete produce idle time for the processor. The function modules are multiprogrammed to circumvent this situation as much as possible. They are made core resident and are multiplexed among each other's dead time intervals. Multiprogramming is achieved through the use of the interrupt facility. The PDP8/E has only one level of priority and hence all requests are handled on a first-come first-serve basis. The X-Y- θ carousel on pickup side, X-Y- θ on bond side, transport, pickup and bond stroke, pickup and bond side mirrors, pickup and bond site capture, pickup and bond side micropositioning and the Teletype^R terminal are the functions that are interlaced through the interrupt to maximize system efficiency. The Teletype^R terminal interrupt allows the operator to hold the machine in a standby state at any time and take charge under abnormal conditions. As mentioned before, the processor keeps track of the current machine status on a per cycle basis. It registers the tray positions, position of the next sequential device to be picked up on each tray, the codes of devices that are mounted on the carousel, position of the bond table and other pertinent information. A variety of different

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circuit pack codes can be assembled with virtually no effect on the machine output.

The process control through the computer consists of micropositioning the device and the bonding site after they have been captured within micropositioning range. Referring to figure 4, the computer reads the position of the device after it is brought in by the acquisition system and activates the proper algorithm to microposition it to the center of the rectangle defined by the reference edges of the four smaller zones (M, N, O & P). The algorithm successively examines and indexes two steps at a time simultaneously in both X and Y axes. When the desired position is located, a final correction is applied at once in all X, Y and rotational areas. A similar micropositioning is performed on the bonding site.

Sometimes missing or extraneous binary video information may cause the micropositioning algorithm to misposition the device or the site. Such information could also result in excessively long "search" times. The algorithm will reject the device or site, in such an instance, if the number of searching moves exceeds a preset limit. A unique example of such a case would be a blank position on the device tray where the device is missing. The computer aborts the search after the limit is reached and seeks the next device in order.

A device will also be rejected if, after micropositioning, it intersects the check zones around the perimeter of the device.

The pickup and bond side positioning are two independent processes. There is no direct interrelation between the two, except that determined at the initial set-up time between the device and the tool, and the tool and the site. To facilitate the initial set-up and also to provide the ability to make minute adjustments during normal machine operation, a biasing algorithm is provided. The operator can inspect the tool, device, and site interrelationship on a previously run circuit pack. Slight misregistration can be rectified through on line bias corrections by temporarily holding the machine in a standby state.

It will be apparent at this point that in order to improve the cycle time a number of factors have to be considered when assembling data files. The movement of the carousel from one tray to the other, the distance in the X and Y axes from one position to the next sequential device on some other tray, and the time to capture and microposition the devices or the sites are random variables which keep changing from cycle to cycle. A mathematical model of each of these functions has been developed and an off line discrete time simulation run on a central data processing system (DEC[®] System 10) which describes the interactions of these functions with each other. This yields a relation between the cycle time vs the travel on the circuit pack from site to site. Based on this information optimum bonding sequences are generated on per circuit pack code basis. These files are stored on the System 10. A PDP8/E post-processor program, on request from the operator, accesses the appropriate file and arranges it in machine compatible format.

The same technique was employed for scheduling the various codes of circuit packs selected for automatic bonding during a given shift.² The

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Process Control For Automatic Device Bonder

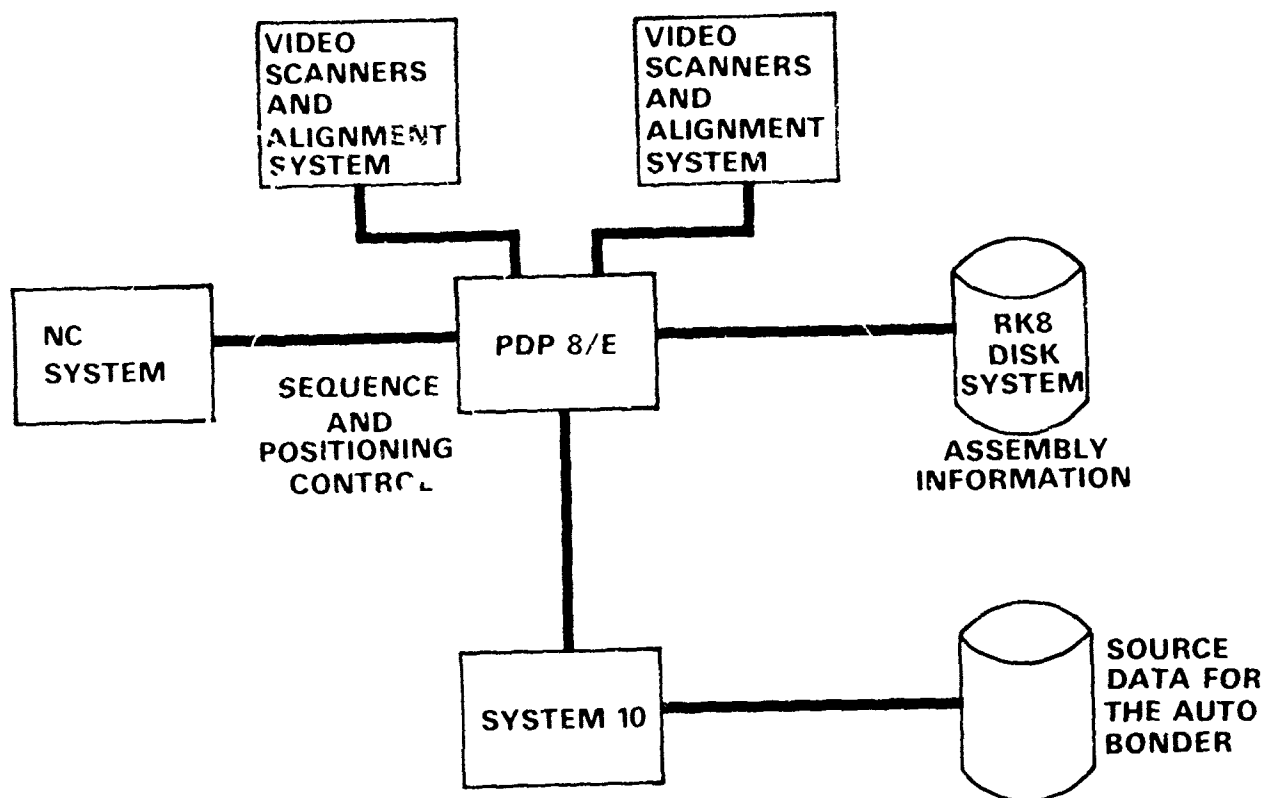


FIGURE 4

scheduling program takes advantage of assembly parts similarities among lots. A study of different device usage in terms of their quantities and combinations with other types was made and optimal tray positions on the carousel were determined from the study. Lots with similar device and data requirements tend to be closely grouped. This fact coupled with the relatively small number of possible carousel configurations, gives rise to a set-up time which is bounded and independent of the number of batches to be run. It is observed that total shift set-up time tends to stay fixed after about 10 batches per shift. This leads to a substantial increase in usable machine run time.

The assembly data referred to above is accessed from several computerized data bases, which provide for immediate and accurate data retrieval, both for computation and display. Additionally, assembly data either for new codes or new issues of old ones, can be added to the data bases automatically, making possible automatic generation of new bonding sequences.

CONCLUSIONS

This first generation facility automates the assembly of hybrid integrated circuit packs by having the ability to identify and microposition beam lead devices and substrates under machine control. This approach has eliminated the need for additional facilities (such as presequencers for devices) and has given us the ability to readily assemble any given circuit pack code within a few minutes with high assembly yields. Handling of the product during the assembly has been greatly reduced. Errors that are inherent in manual assembly process have been cut down. This has had a profound effect on the test yields. Figure 5 is the block diagram of the central data processing facility showing various shop operations tied together. The bonding facility has established a major link to the production shop in this network.

By using a new optimum bonding sequence for each code the total bonding cycle time has been minimized. Near optimum scheduling provides for minimum set-up costs. All assembly data has been computerized in regards to updating, retrieval and display.

Our results from this facility are as follows:

- Device to site alignment yield 99.3%
- Beam lead bond failures 6 out of 10,000
- 2 sec. average for micropositioning devices
- 1.2 sec. average for micropositioning sites
- Left to right transport time 1.7 sec.
- Average machine cycle time 512 device bonds per hour (14,336 bonded interconnections)

ACKNOWLEDGEMENTS

The authors acknowledge the principles of the Averaging System as developed by L. J. Montone and R. F. Frank, WECO, Reading and R. W. Hurlbrink (PTL). In addition, the valuable assistance of R. F. Myscofski, W. J. Edwards, C. J. Young, S. Golinski and E. J. Gimnig is acknowledged.

Computer Aided Manufacturing

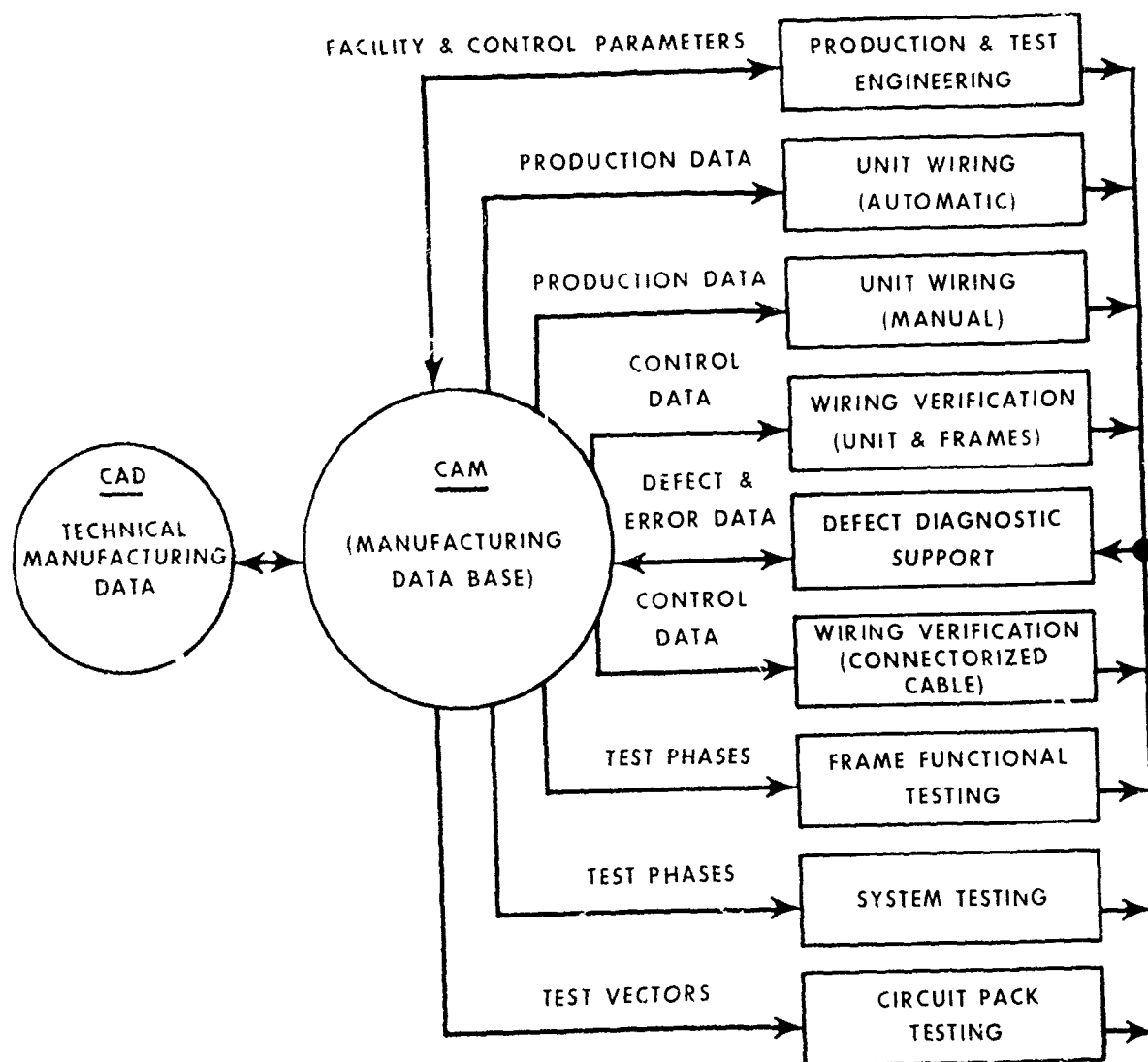


FIGURE 5

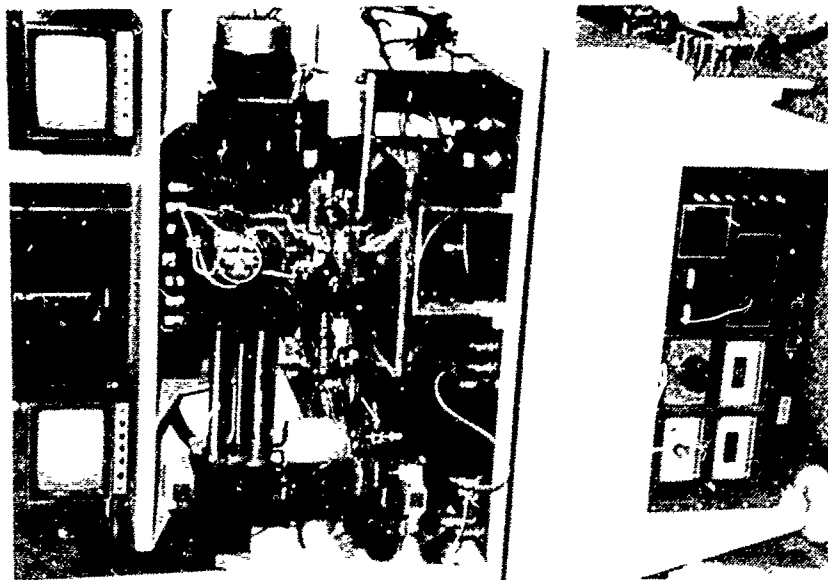


FIGURE 7
OVERALL VIEW OF BONDING MACHINE.
(NC AND CPU CABINETS ARE NOT
SHOWN IN THIS VIEW)

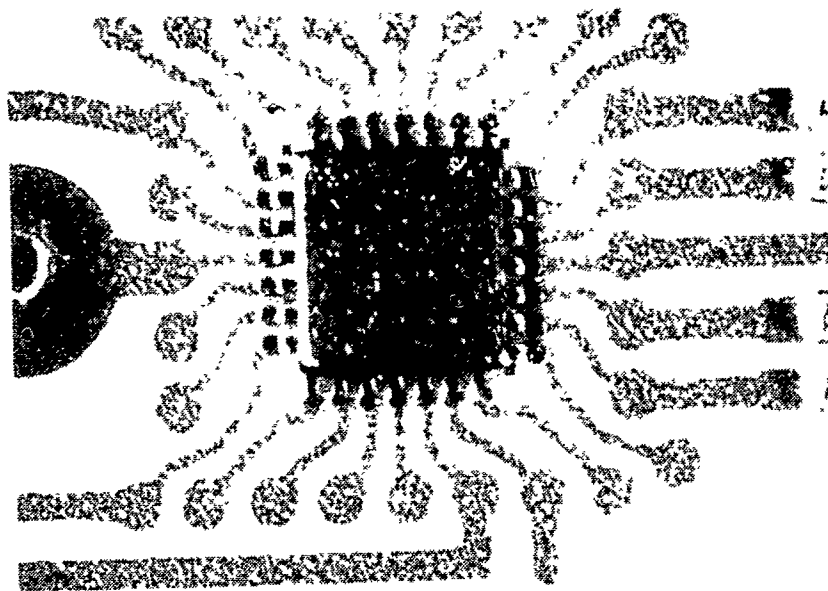


FIGURE 6
BONDED BEAM LEAD DEVICE (50 MIL²).
EXPANDER PATTERN AND DIAGNOSTIC
TEST PADS ARE ALSO SHOWN.

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SOLDER BUMPED SEMICONDUCTORS - AUTOMATIC

HANDLING FOR HYBRID MICROCIRCUITS

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ABSTRACT

The primary purpose of automatic handling of components for hybrid microcircuit assembly is to reduce the cost of labor associated with manual or semi-manual placement and bonding.

Solder bumped semiconductor devices offer several advantages in automatic handling provided the chips are manufactured within the necessary dimensional restrictions, desirable form factors, and tolerances.

The general methods of orienting, aligning and placing the semiconductor chips during testing and/or assembly onto thick/thin film substrates are described. The optimum desirable form factors and tolerances are discussed with regard to limitations to chip fabrication, testing and final use - assembly into hybrid microcircuits. The projected savings resulting from use of solder bumped semiconductors is presented.

INTRODUCTION

Assembly of hybrid microcircuits in high volume requires considerable amount of labor, particularly when semiconductors are mounted by the so called "chip and wire" technique. Because of the high labor content, this kind of volume assembly is often done off-shore in geographical areas where labor rates are low. It has been recognized by electronic circuit and equipment manufacturers that the use of low cost off-shore labor is a more or less "temporary" situation. The reasons for that are several:

1. The labor rates in several of the countries where assembly is being done have been increasing.
2. Political changes in some of the countries (or the threat of such changes) creates a natural question regarding the soundness of capital investment and future of these investments in plants and equipment.
3. Pressure from government and labor organizations is directed towards increasing domestic production and improving the competitive position of U.S. made products.

As a result, there seems to be an ever-increasing interest in automatic assembly of electronic equipment and in components which are designed and are suitable for efficient handling by completely automated assembly lines. This paper discusses the solder bumped semiconductors known as "Flip Chips" with respect to automatic assembly.

FLIP CHIPS - WHAT ARE THEY?

The name "Flip-Chip" has been used in the microelectronics industry for well over 10 years and describes a semiconductor device which is designed for face down bonding (and hence flip chip) as compared to "chip and wire" face up bonding and wire assembly of hybrid microcircuits (Figure 1). The Flip Chip referred to in this paper is a semiconductor device having a glass layer for protection against environment and having lead/tin bumps for contact (Figure 2). The basic requirement for a chip intended to be used in automated handling are:

1. The chips should have square edges and very uniform dimensions.
2. The chips should have Braille-like protrusions on one side of the chip for differentiating top from bottom.

Solder bumped flip chips fill these requirements quite easily.

FLIP CHIPS - HOW ARE THEY MADE?

The fabrication of flip chip devices starts with oxidation of epitaxial slices and proceeds through photo-resist, oxide etching and diffusion as shown in Figure 3. The basic process is the same as conventional planar process with the exception of an additional N+ diffusion for NPN transistor or diodes, and a P+ diffusion for PNP transistors. This additional diffusion step is necessary to assure low series resistance for the collector contact, which for flip chips has to be on the face side instead of the backside as for conventional chips. After diffusion, the slices are metallized with aluminum and the contact patterns are formed in a conventional manner.

The process steps for bump formation are listed in Figure 4. The process involves deposition of silox over the entire surface of the wafer. The purpose of the silox is to provide mechanical and environmental protection for the active area of the device. This silox layer also protects the device from flux and solder during mounting operations.

Next the wafer is coated with photo-resist, exposed and developed to etch via holes in the locations where solder terminals are to be formed, making sure that a clean surface of the aluminum pad is obtained inside the window.

The bump formation is accomplished by electron beam sequential deposition of Al and Ni in such a manner that a thin phased layer of AlNi is formed between the two metal deposits. The total thickness of the metal is approximately 10,000 to 12,000 Å. By a photo-resist step, the nickel is etched off everywhere except over the via holes. The nickel serves as a base for the solder bump. Subsequently, photo-resist is applied and exposed to form a plating mask. Copper and PbSn solder is plated onto the nickel. After the plating is complete, the photoresist is removed, the exposed aluminum is etched off and the PbSn solder is fused in pure H₂ atmosphere at approximately 400°C to form the smooth round bumps as shown in Figure 5, which is a scanning electron micrograph of a transistor wafer. A back-marking

pattern is formed on the wafer for the purpose of being able to identify each flip chip by type and orientation. The wafer is then sawed into individual chips (Figure 6). The metallurgy of a bump formed by the above method is shown in Figure 7. The electrical resistance of each individual bump is measured to be 0.005 to 0.015 ohms. This is lower than bump resistances obtained by vacuum evaporation of the metals in the bump. After the chips are separated, they are then tested automatically using a Bulova or a similar chip handler.

FLIP CHIPS - HOW ARE THEY USED?

The interconnection between the chip and the substrate of a hybrid circuit assembly is made by soldering the chip to the passive network in a face-down position. Figure 8 shows a hybrid circuit assembled with integrated circuits, diodes, transistors and capacitor chips. In this case, the assembly was accomplished by placing each individual flip chip and capacitor chip onto the substrate by hand and then reflow soldering the components in a single heat cycle. The reflow cycle involved is achieved by passing the substrates with the chips through a belt furnace. The assembly is exposed to a temperature above 300°C for approximately 30 seconds. During the soldering operation, both the solder on the substrate and the solder on the chip are remelted and they intermix. As the solder melts, the bumps collapse by some amount which is determined and controlled by surface tension. This collapse assures that all terminals of the chip make contact and connect to the circuit. This distance which a chip will move towards the substrate during solder reflow is determined by the size of the solder pads; i.e. the combined amount of solder on the pad and the bump on the device. Self alignment because of surface tension also occurs during reflow.

AUTOMATION WITH FLIP CHIPS

Flip chips can be used equally well in hand assembly operations and automated assembly operations. The main requirement for automatic assembly is that they are dimensionally held to a close enough tolerance to be able to be mechanically oriented and placed. Let us look back to the process of automatically testing the rough sawed chips. This is usually accomplished on a chip handler offered by Bulova. The way this handler works is that during the first cycle the chips are synchro fed to a slightly inclined plane, which contains micro-grooves. When the chips reach this plane, they pass ahead in the direction of the grooves. The size of the grooves and the decline is such that any chips with the bumps facing up would slide off and be recycled. The chips with the bumps facing down stay on this grooved track, they move on and get lined up in a channel one behind the other. The chips at this point are picked up by a vacuum tool and are placed onto a set of probes, where it is electronically decided whether the chip is oriented correctly or if it should be rotated 90°, 180° or 270°. The rotation is accomplished during the time the chip is transferred from the first set of probes to the second set of probes, where the testing and classification is done. Upon completion of the testing, the chips presently are accumulated in a vial, visually inspected, QC'd and sent to hybrid circuit manufacturers.

The orientation that was established, has now been lost again. It is quite easy to visualize a situation where instead of dropping the chips in a tube they can be placed either in a tray, which would maintain the chip orientation or actually place the chip on a substrate directly from the chip handler while the orientation has been established. Successful experiments have been performed along these lines and it is only a question of time and volume before it is done in production. Another approach which has been developed by Teledyne Tac is one where the chips are picked up from a wafer that is held on an expanded sticky tape and placed on a specially prepared carrier. With this approach transistors (or IC's) can be selected from a wafer and placed on the tape selected to any desired electrical performance criteria. (See Figures 9 and 10).

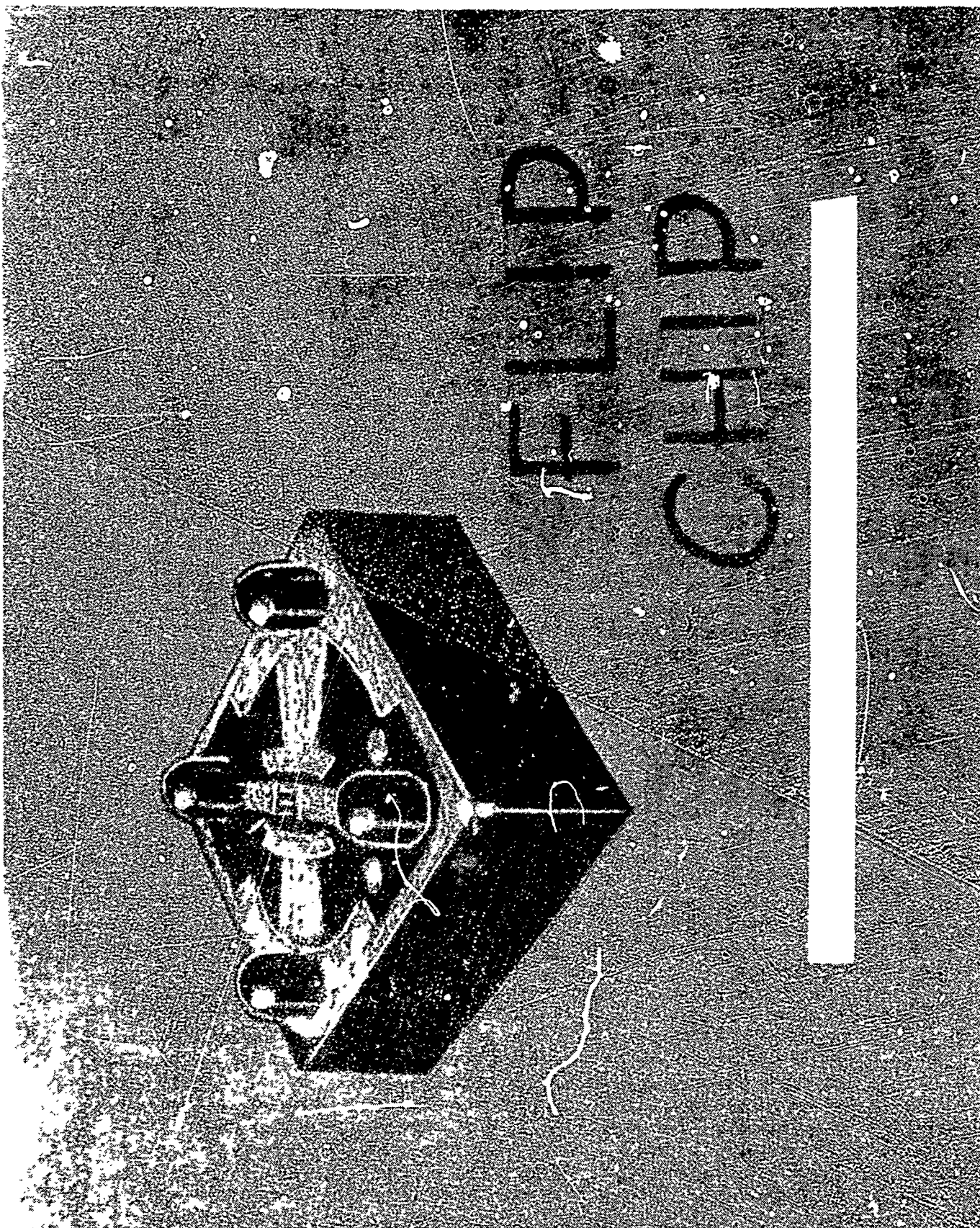
FLIP CHIPS ON TAPE CARRIERS

In some cases it is desirable to mount chips onto an intermediate carrier instead of mounting the chips directly onto the substrate. Such an approach has been described before by General Electric as the so called "Mini-mod". Also it is known as TAB for Tape Automated Bonding (Honeywell) and as Innerlead Bonding. There may be several different names by which this technique is known, but the common denominator in all cases is that the chip is bonded on a flexible carrier, which allows the chips to be automatically tested and automatically placed and bonded either on substrates or lead frames. The metallurgy of the described flip chips or modifications of it are well suited for this approach as well. In this case after completion of the copper plating step, the surface of the copper is plated with a thin layer of solder, gold, gold-tin eutectic or other metal which would be suitable for bonding to the tape or similar chip carrier. In any case the closely controlled dimensions of the silicon body and the small bumps on one of the faces of the chip provide an ideal semiconductor for automatic handling.

CONCLUSION

Semiconductor devices in flip chip form are ideally suited for automatic handling in testing and assembly. They can equally well be incorporated in thick or thin film circuits or mounted on tape carriers. The processes and metallurgy has been developed and it is expected that the chips will gain wide acceptance in applications where automation is essential.

- Figure 1 Chip with solder bumps - Artist's concept.
- Figure 2 SEM of chips with solder bumps.
- Figure 3 Fabrication steps (diffusion).
- Figure 4 Fabrication (bumping).
- Figure 5 Smooth round bumps.
- Figure 6 Individual chips with square edges.
- Figure 7 Bump metallurgy.
- Figure 8 Hybrid Circuit assembled with Flip Chips.
- Figure 9 Teledyne/Tac chip handler.
- Figure 10 Close up of handler.



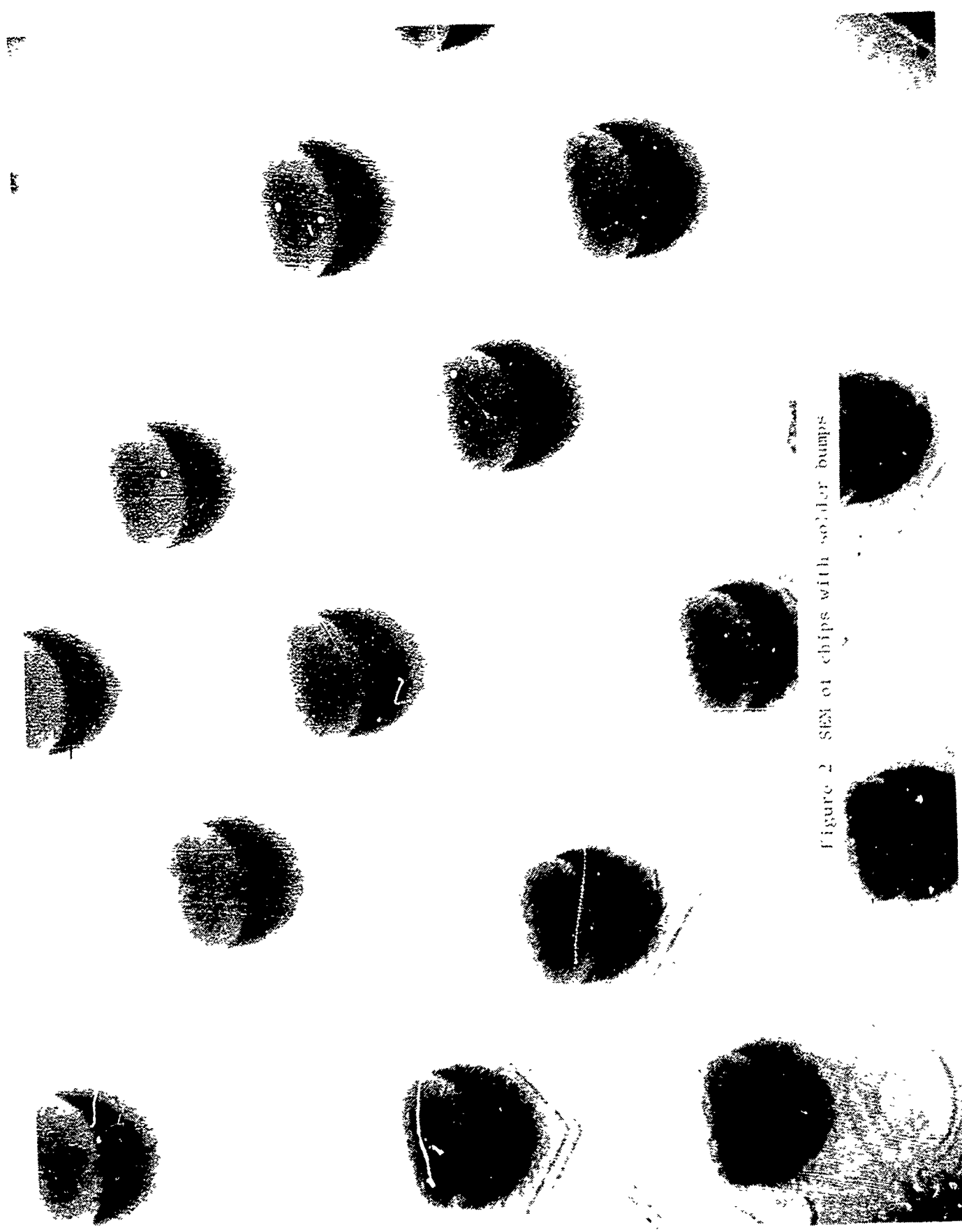


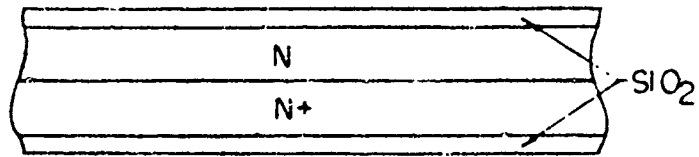
Figure 2 SEM of chips with solder bumps

Figure 3

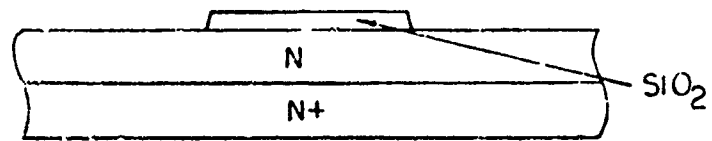
Fabrication steps (diffusion)

SILICON WAFER PROCESSING STEPS

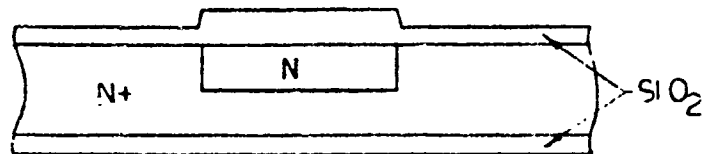
FIRST
OXIDE



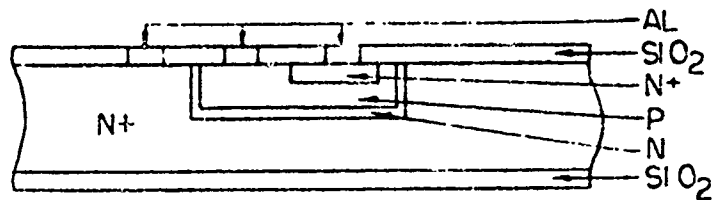
OPEN N+
WINDOW



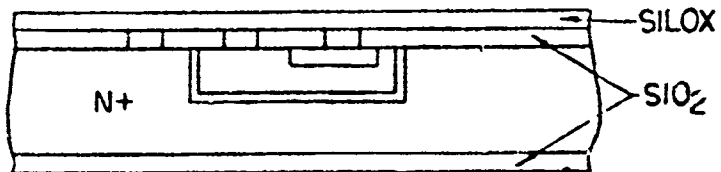
N+ DIFFUSION
& OXIDATION



TRANSISTOR
PROCESSING



SILOX
DEPOSITION



ETCH
WINDOWS

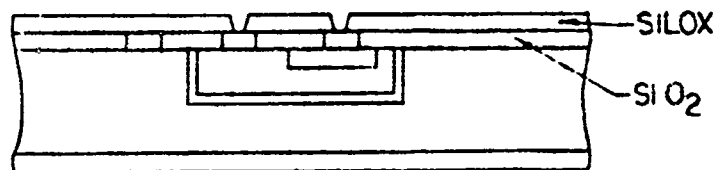
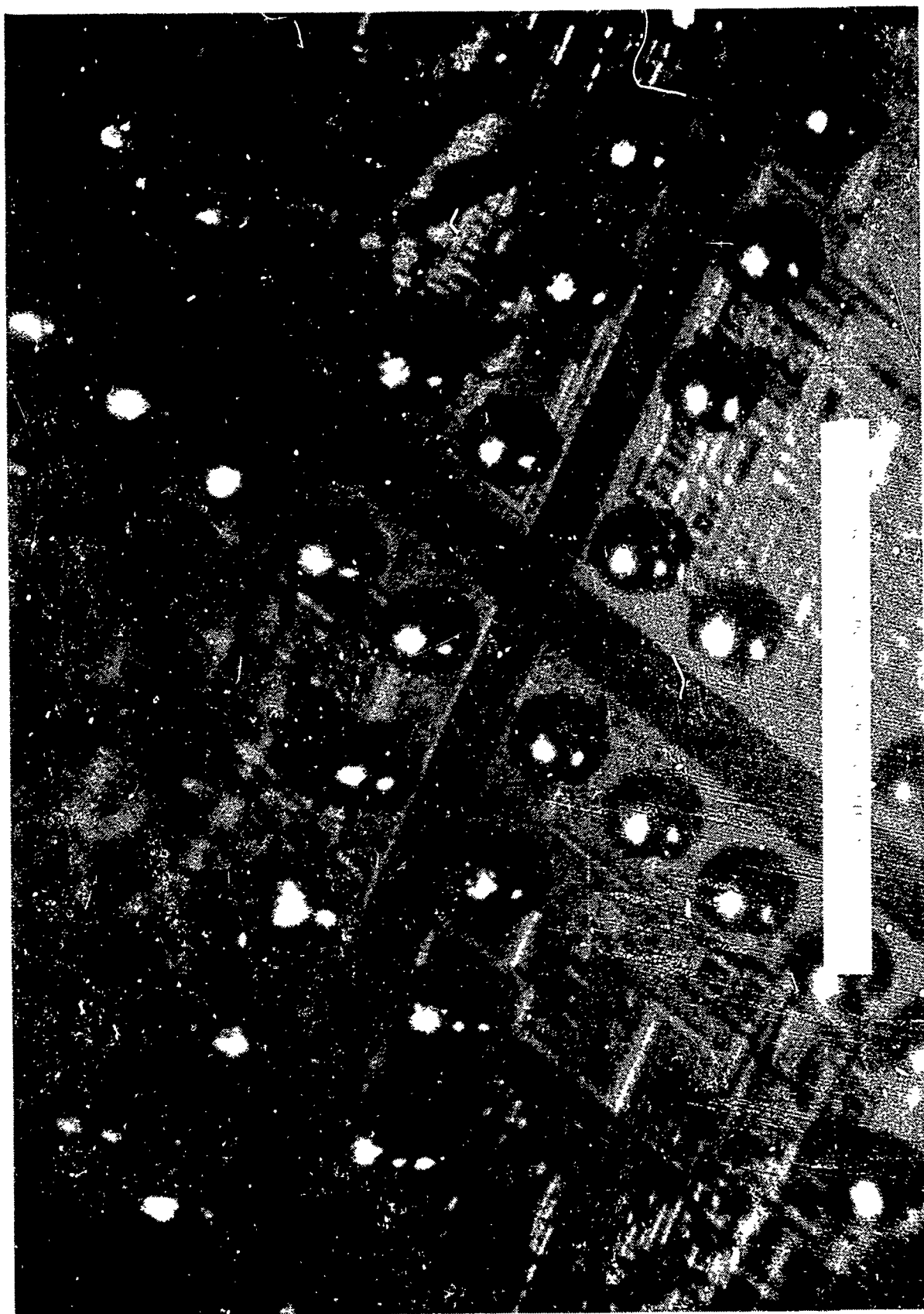


Figure 4

Fabrication (bumping)

PROCESS STEPS FOR FORMATION OF SOLDER TERMINALS:

1. Silox deposition
2. Photo resist application and etching
3. Evaporation of Al - Al Ni - Ni
4. Photo resist application and etching
5. Photo resist application and processing
6. Electrolytic plating of copper
7. Electrolytic plating of lead - tin
8. Buss metal etch
9. Spheridizing of solder terminals
10. 100% probing



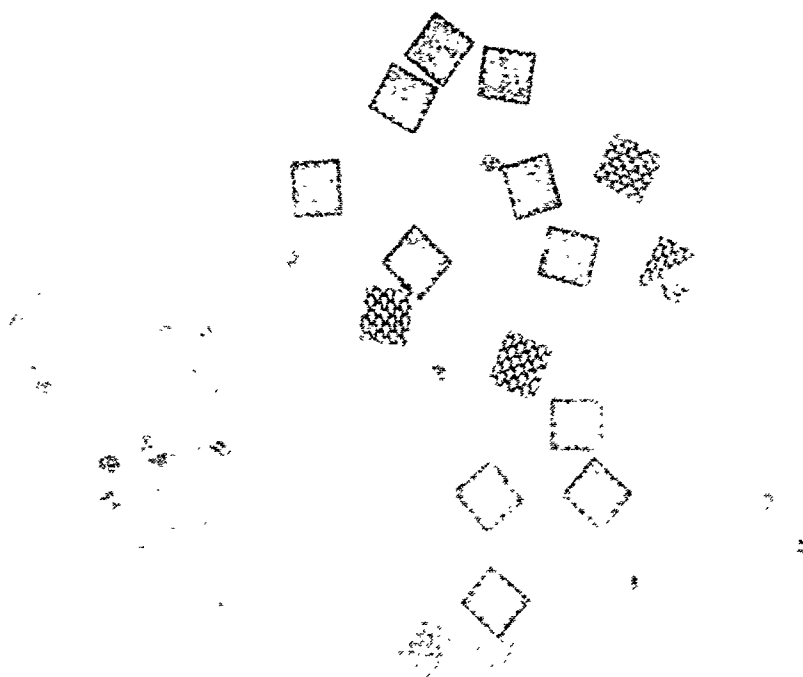
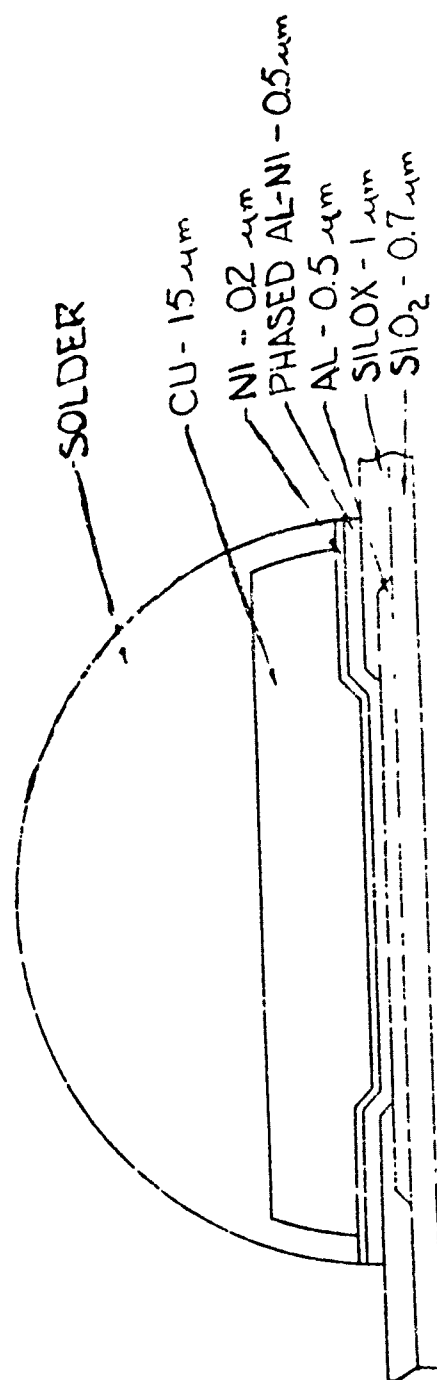


Figure 6 Individual chips with square edges

Figure 7

Bump metallurgy

METALLURGY OF CONTROLLED COLLAPSE INTERCONNECTIONS



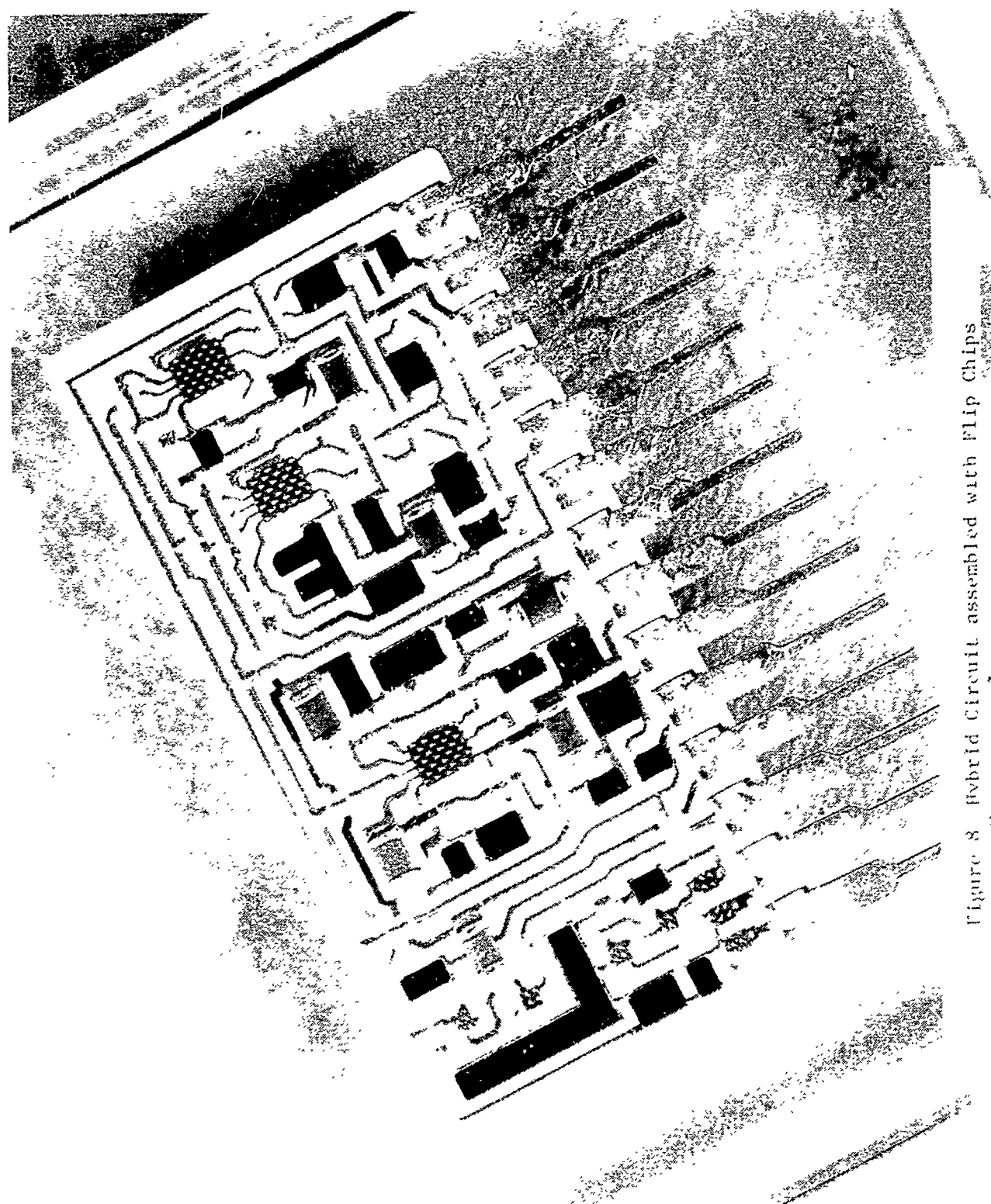


Figure 8 Hybrid Circuit assembled with Flip Chips

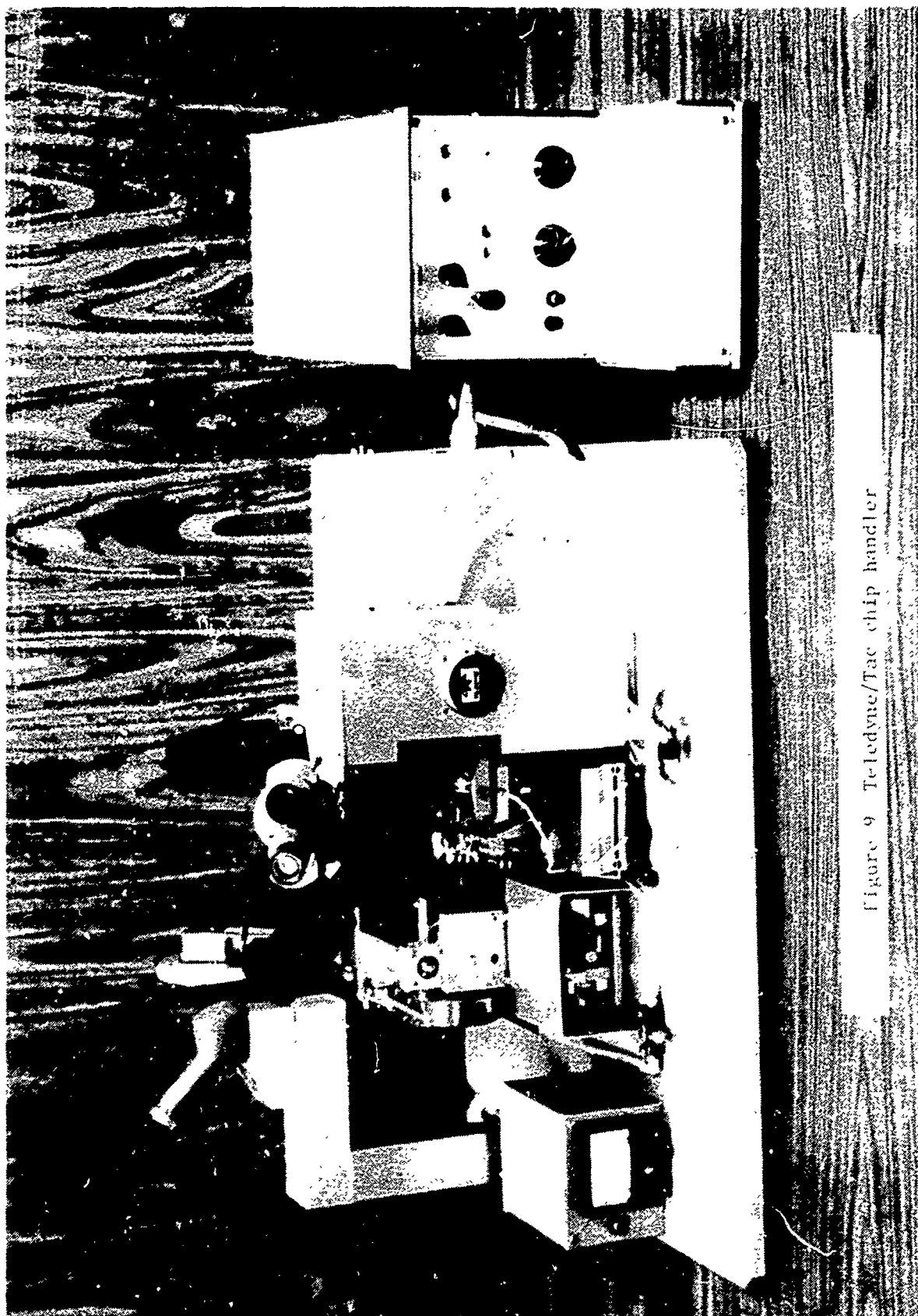


Figure 9 Teledyne/Tac chip handler

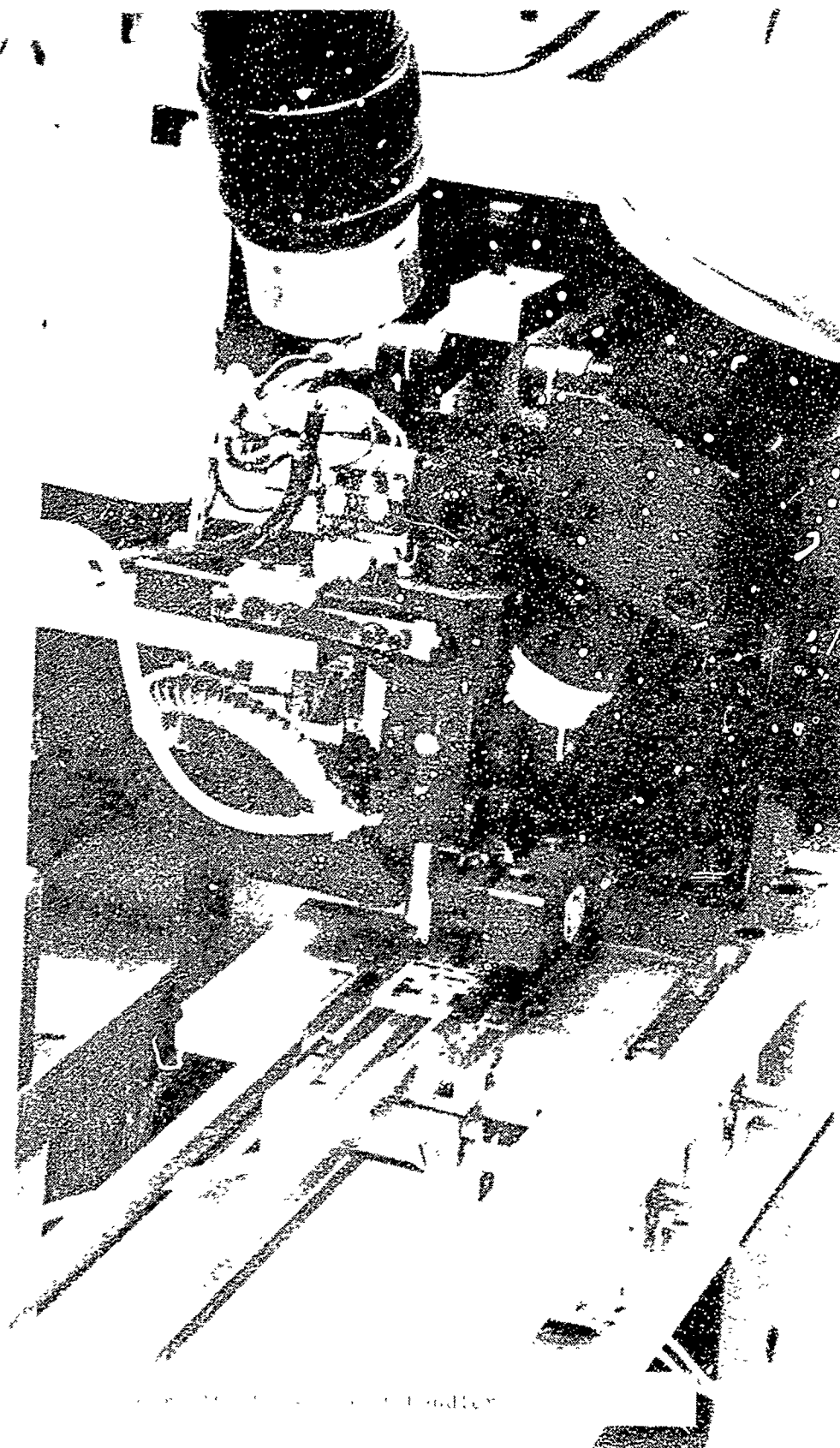


Figure 1. The mechanical assembly.

INTEGRAL SPIDERS

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ABSTRACT

This paper concerns itself with the design, fabrication and testing of an integral spider substrate assembly. The integral spider substrate was developed utilizing a thermally oxidized silicon wafer and a single metal interconnect system. The multilayer interconnect structure is composed of sputtered aluminum conductor and silicon dioxide insulator films. Interconnection between the two conductor layers was achieved by means of etched via holes in the dielectric film. The conductor and beam patterns were formed by conventional photolithographic techniques. Anisotropic etching of the silicon was used to open windows in the substrate and expose the overhanging beam leads. Beam leads were also provided along two substrate edges for interconnection to the package input/output pads. Conventional aluminum metallized semiconductor chips including transistors, integrated circuits and resistor arrays were ultrasonically bonded to the beams. The completed substrates were mounted into aluminized ceramic packages and the edge beams bonding to the package pads to give a total beam leaded structure. A number of working circuits containing as many as thirteen devices were assembled and tested to demonstrate the feasibility of the approach.

The technology which is applicable for hybrid packaging applications using MSI/LSI devices may also be used as a vehicle to test devices and as a subcarrier when used in conjunction with thick film copper multilayer substrates to build even more complex assemblies.

A summary showing the principle features of the Integral Spider process is discussed along with a comparison of Integral Spider, Tape Carrier, Chip-and-Wire and Beam lead techniques.

INTRODUCTION

For many years now the electronic industry has been searching for techniques to fabricate and interconnect semiconductor devices that can withstand Military nuclear environments.

The interconnection technology discussed herein is the result of many years of research and development by Raytheon Company in this field. "Integral Spiders (I/S)" the term which we have dubbed this technology, has now shown itself to be not only a very effective solution for radiation resistant applications but also possesses features which have applications in many other areas. Some of these applications are:

LSI Interconnects - Here the I/S technique has shown that it can reduce size by 75% and reduce stray capacitance by approximately 80% thereby improving speed characteristics.

Memory Interconnects- Here the I/S technique again provides a size and capacitance advantage as well as providing the ability to interconnect complimenting semiconductor devices.

In both the above applications the Integral Spider also offers both short and long term cost savings.

The Integral Spider Technology is the first interconnection technique that bridges the gap between semiconductor devices and printed circuit boards with completely compatible materials and processes. On the following pages is the story of how an integral spider is fabricated. From it one can see where it's compatibility and simplicity are derived from.

To begin, the term Integral Spider I/S which we have used here refers to the fact that the spider (or beam pattern) that connects to the semiconductor chip is an integral part of the interconnect pattern. The uniqueness of the technique is that all the materials and processes used in the fabrication of the integral spider are identical to those used in the fabrication of the semiconductor device itself. It also is the first hybrid concept that allows a functional electrical test to be performed prior to the actual bonding of the chips. This is accomplished through the formation of tiny pyramid nodes on the underside of the beams which under light pressure are able to break through the aluminum oxide formed and make a true electrical connection.

To provide some prospectus of what an integral spider looks like, Figure 1 shows a completed integral spider substrate. The black area being silicon which is used as the substrate material onto which the two layer interconnect is formed. The matted surface shows where the silicon has been etching away to expose the beam patterns which are on the perimeter and used for input/output connections. Also, cavities are etched in the silicon to receive the semiconductor chips which will be connected to the beam pattern exposed over the cavities.

Figure 2 depicts a cross-section of the spider interconnect showing the various dimensions of the silicon and deposited layers and also indicating the etched cavities for chip receipt and exposed edge beams. The overall size of this integral spider was approximately one inch square, however, other units have been built of varying sizes up to one inch as shown on the cover sheet and it is expected that the upper size limit can be as large as the largest piece of silicon available. The thickness of the silicon is determined by adding two mils to the thickness of the thickest chip used. The spread of chip thicknesses can vary by five mils without artwork compensation. The limiting factors are the bonding tool dimensions and the test pressure pad dimensions.

To get into the details of the fabrication processes used, Figure 3 depicts a typical process flow. The first block of 25 steps represents the processes associated with fabricating the integral spider substrate. In reviewing these one can see that the process steps are identical to those used in the fabrication of the MSI/LSI semiconductor devices themselves if you start at the point of the last diffusion step and proceed through the metallization and separation etch processes.

The second block of steps indicates those operations associated with the assembly of the semiconductor chips into the integral spider substrate.

At this point, there are two avenues of approach, one assumes the integral spider to be a complete assembly where the unit is placed in a ceramic flatpack and hermetically sealed. The other approach looks at the integral spider as a sub-assembly where the unit is inserted into cavities in a ceramic thick film multilayer substrate along with several other assemblies and odd configuration discrete devices that are desirous to be kept separate from the integral spider.

A 1-0-0 piece of silicon cut and ground planar with it's crystal axis is cleaned using a combination of chemical and ionic cleaning. A thermal oxide (SiO_2) is then grown over the entire substrate in a diffusion furnace (see Figure 4). A photoresist pattern is then applied and pyramid shaped cavities are etched into the silicon generally in patterns of three or four per beam. These patterns are typically .6 mils square at the surface and go to a depth of .5 mils controlled by the lattice characteristics of the silicon.

The first conductor layer is then deposited using sputtering techniques to a thickness of 2 microns. Photoresist is then applied and the first layer conductor pattern delineated. Using potassium ferri cyanide and potassium hydroxide solution, an aluminum etchant, the unwanted material is removed. The remaining photoresist is then stripped using Hunt Microstrip to complete the first layer metallization.

To insure the underside of the beam pattern is free of any oxide contaminants which may hinder electrical contact a photoresist pattern is applied and the thermal oxide removed in those areas where contact is to be made. See Figure 5.

Assuming that two levels of interconnect are required in order to interconnect the devices which are to be bonded to the integral spider substrate a layer of SiO_2 is deposited using sputtering techniques also. The reason for the choice of an all sputtering approach to the multilayer process is it's high degree of uniformity over large areas without the need for any exotic tooling or fixtures. This degree of uniformity in coating insures a high yield through the multilayer process. Also, by regulation of the power and time, variations in the hardness of the aluminum beam can be

optimized to provide both a hard sharp node for testing and a softer aluminum for ultrasonic bonding. This is a very critical aspect of the metallization system. After the SiO_2 is deposited, a photoresist pattern is delineated and plasma techniques are employed to etch away the unwanted SiO_2 and to form vias to expose the first layer metallization. The plasma technique was chosen because of its self-stopping feature when it reaches the first layer aluminum. This removes any criticality from this operation while insuring a clean aluminum first layer surface to later make a good ohmic contact. See Figure 6. The unwanted photoresist is then removed using conventional techniques.

In Figure 7 we see the second layer of aluminum has been deposited to a level of 15 microns or approximately one-half mil. While this is a very slow metallization process in conventional sputtering systems (about 10 to 12 hours) it can be performed using a magnetron target in a little over one hour. As shown in Figure 7 the top metallization forms the beam pattern, input/output pattern and provides for crossovers. Prior to the actual deposition of the aluminum a reverse sputtering process is performed to remove any aluminum oxide which may have formed on the first layer.

Photoresist is then applied and the second layer pattern delineated. Etching is performed with conventional aluminum etchants with some care being exercised to minimize undercutting. The unwanted photoresist is then removed. The degree of dimpling on the topside of the beam is a function of the node size and with the multinode system where the nodes are no greater than .6 mils at the base, it is almost nonexistent (Figure 8).

A final clean-up is done to remove any residue and the circuit pattern tested for continuity and shorts. This completes the fabrication of the Integral Spider substrate which now can have the active components added to it. Not discussed to this point is the possibility of forming resistors on the substrate as well as the interconnect pattern by either diffusion or thin film processing techniques. Both are feasible and economical with this approach (Figure 9).

Figure 10 depicts a completed integral spider substrate with two layers of metallization. In Figure 11 the underside of a beam is shown which has four nodes. The purpose of multinoding is to eliminate any possibility of contamination getting under the node to interfere with the electrical test operation.

Assembly of the chips to the integral spider substrate is accomplished in the following manner. See Figure 12. A glass plate which is used as a working fixture is coated with photoresist and the same pattern that has been generated on the integral spider is created on the glass plate by exposing and dyeing. The glass plate is then spin coated with a thin layer of wax which has a relatively wide muddy range.

Under a microscope with an IR spot heater on the underside of the glass tooling plate each chip is located with respect to the pattern, the wax locally heated using the IR spot heater and the chip fused in place. This process is continued until all the chips have been located on the glass plate. By using the same pattern that is used on the integral spider each chip is in precise location to the spider substrate. The next operation involves the placement of the integral spider on top of the glass plate with the chip being located into the cavities in the substrate and the beam pattern on two chips diagonally opposite from each other being aligned with the pattern on the chip face. Because all alignment is accomplished with respect to the pattern on the chips the tolerance variations in dicing the chip have no effect. After the integral spider substrate is aligned the entire surface of the glass is heated to fuse the substrate to the glass as well as the chips. The wide muddy range of the wax prevents any movement of the chips during this operation. At this point the back side of the substrate and the back side of all the chips are now on the same plane. By doing this die attach of the entire assembly it is greatly simplified when it is later performed.

Figure 13 reviews briefly the features of the node(s) which have been placed on the underside of the beam. It's three principle advantages are:

1. Prevents passivation cracking on the monolithic chip which is typically higher than the aluminum pads. Also, it allows the beam to ride over exposed conductors on the chip when the pad being connected to is not on the perimeter.
2. The second and most important feature is that by applying a compliant pressure pad to the top side of the beam the node with two grams of pressure per beam applied is able to penetrate the aluminum oxide on the chip pads and makes an electrical connection to the chip. By applying pressure simultaneously to all the beams on the integral spider substrate a complex functional test can be performed.
3. The other advantage of the node is that by highly concentrating the ultrasonic energy during bonding parameter, settings such as power and force can vary widely without affecting bond strength.

After the substrate and the chips have all been located, aligned and bonded to the glass working plate the entire assembly is placed in a modified probe head. (Figure 14 shows a unit in position that has just one chip.)

After the input/output contacts are made a compliant ram made from a high durometer silicon rubber that has a raised configuration which corresponds to the location of each of the chips is pressed against the surface of the substrate. This compressing action forces the nodes on the underside of the beams (see Figure 15 and 16) which have a very sharp pyramid shape to penetrate any oxide that is on the surface of the chip pads. (See Figure 17 and 18) Electrical contact is then made and the circuit

tested electrically in a functional manner. If any devices are shown to be defective the unit still on the glass holding plate is removed from the tester, the integral spider substrate dewaxed and removed, the defective chip is replaced with another one and the integral spider again placed in position and waxed down. The test is then repeated to assure all components are now operative. We have performed this operation up to 12 times with the same integral spider assembly and found that we were able to make electrical connection every time. In practice we have not had the need to repeat the cycle more than three times.

After completion of electrical test the entire assembly still on the glass holding plate is located on the ultrasonic wire bonder that has been modified in the following manner. The bonding tool with the hollow cavity for wire feeding was replaced with a solid tool with a wedge shape tip. The micropositioner for moving the substrate under the bonding tool was replaced with a numerically controlled table which is controlled by the same information obtained during the design of the beam pattern. The entire assembly is then ultrasonically bonded one at a time automatically. Wobble bonding is not possible because the chip sits in a well and access is limited. The bonding operation itself, however, is quite fast on the order of 20 to 30 bonds per minute. See Figure 19 to 23.

Another electrical test is then performed by probing the input/output leads. This insures that all bonds were properly made. Figure 24 depicts the various other types of components that could be used with this packaging technique and how it is accomplished.

For transistor and diode chips with back side electrical connections they are premounted to a Kovar mounting base that has an aluminum tab welded to it that is the same thickness as the chip. The entire assembly is then treated like any other semiconductor device and mounted in a well under the beams. Resistor and capacitor chips with connections on one side are also assembled in the same manner as I.C. type chips. Large coils or capacitors are mounted onto the top surface of the substrate using aluminum-germanium-zinc as a soldering medium.

To package the integral spider within a ceramic flatpack requires some initial preparation of the package unless it was specifically designed for this purpose. As shown in Figure 25 we wanted to create an all aluminum interconnection and as such had to metallize the inside of the package, photoresist, and etch in such a manner as to leave aluminum pads on top of the molybdenum pads that connect through the wall of the package. The intention here is to use epoxy die attach techniques and as such no preparation of the package floor is required. For applications where a eutectic bond is required, the package floor would be metallized with the same material that is on the backside of the integral spider substrate and chips. This is essential as there is no possibility of scrubbing with this approach and to obtain a good eutectic die attach both surfaces must have a clean metallized surface.

The substrate assembly which now has been removed from the glass holding plate and cleaned is placed inside the package on top of a pre-form of epoxy. The corner output leads are aligned and the entire assembly heated to flow and cure the epoxy, thus making complete die attach of all the chips and the integral spider substrate to the package. The output leads are then ultrasonically bonded to the aluminized pads on the package and the complete assembly tested.

The final operation involves the parallel seam welding of the package cover and the performance of any electrical or environmental testing. See Figure 26. Figure 27 depicts the repair procedure used if a device fails.

Two completed assemblies are shown in Figures 28 and 29. The unit has been completely environmentally tested to Mil Standard 883, Level B while the unit in Figure 29 has been exposed to high degrees of radiation to determine the worth of the technology in a nuclear environment. While details of these tests are classified it can be said that the system is capable of meeting any known requirements that have been specified to date.

In summary, the four principle objectives: cost, reliability, performance, and radiation have been met to provide a hybrid technology that has many potential applications. See Figure 30 a and b.

Also, a bridge between the hybrid monolithic industry has now been built which allows the hybrid designer or user to take full advantage of monolithic techniques.

Shown in Figure 31 is an artist's concept of the integral spider being utilized as a submodule. This interconnection approach which we have dubbed "Integral Spider Interconnects I/S/I" is currently being developed by Raytheon Company in Sudbury, Massachusetts and will be reported on at a later date.

With regard to other hybrid technologies the integral spider approach seems to fare very well technically. Figure 32 compares integral spiders with chip-and-wire, beam-lead and tape carrier. These technologies are compared only with what is considered the standard approach for each. There are variations of these approaches which conflict with that summarized in the chart, however, it is felt that the chart does provide a basic means of comparing the four approaches.

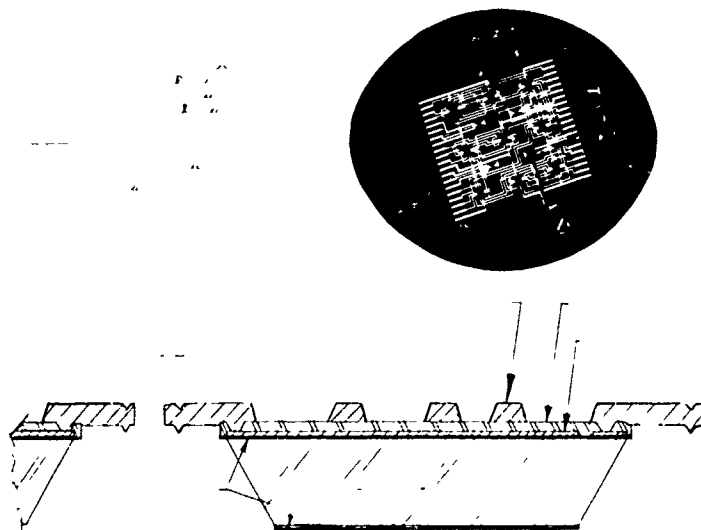
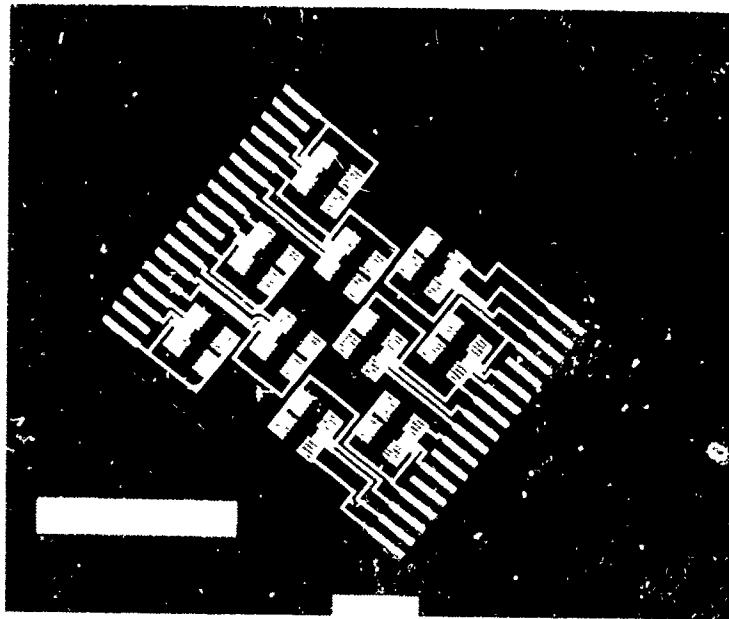


FIG. 91

INTEGRAL SPIDER PROCESS FLOW

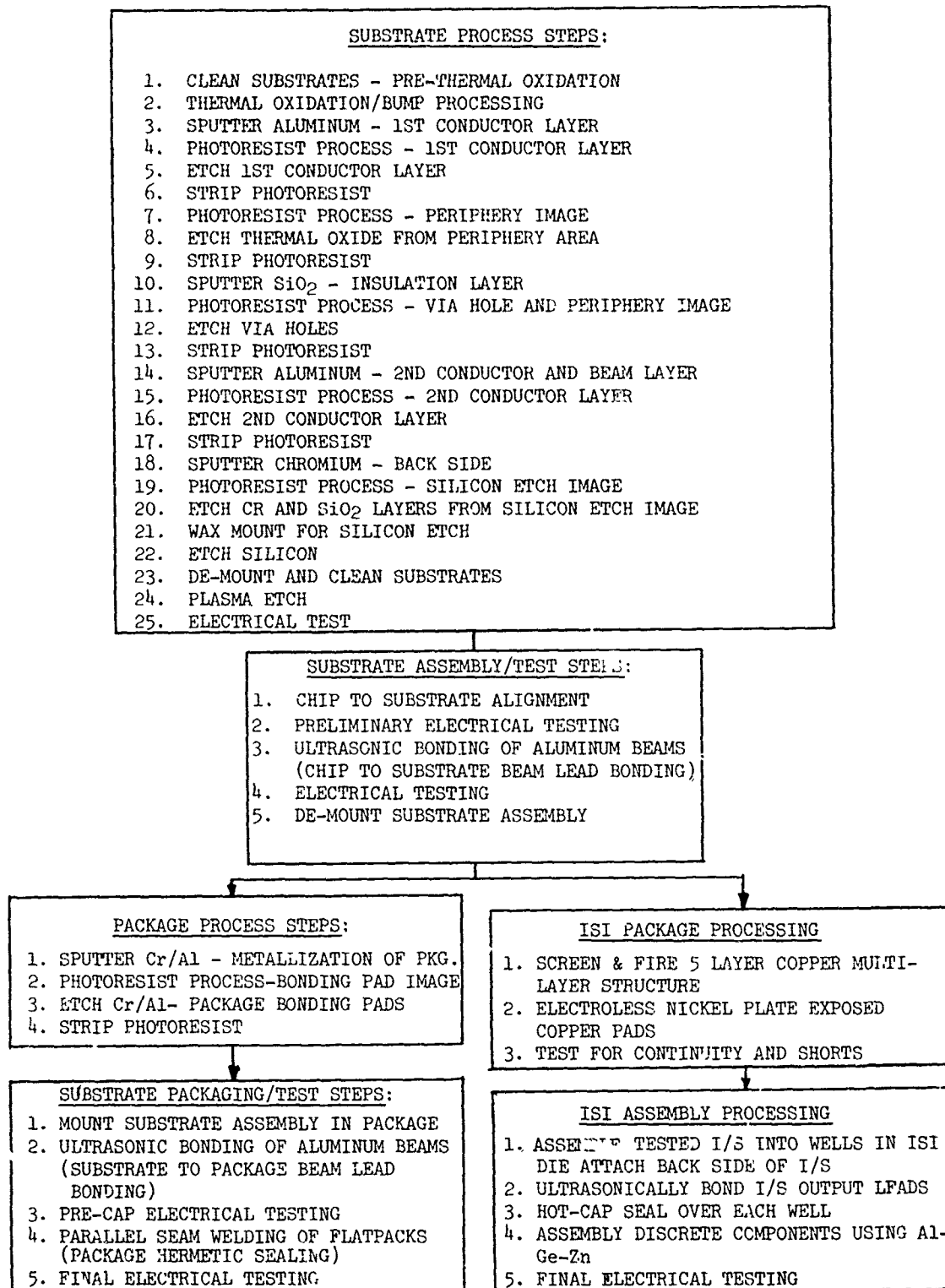
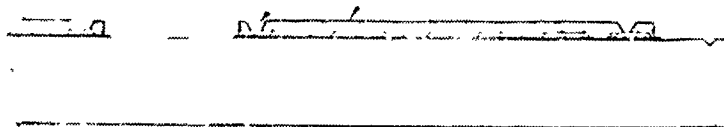
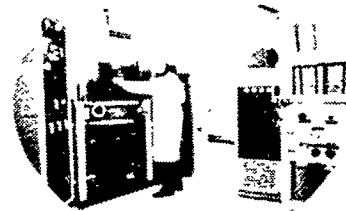
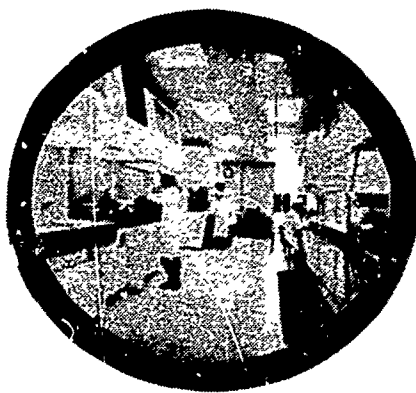
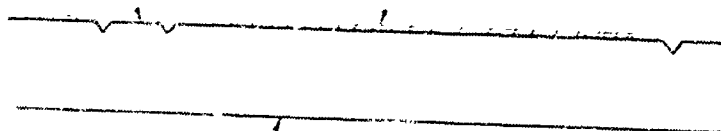
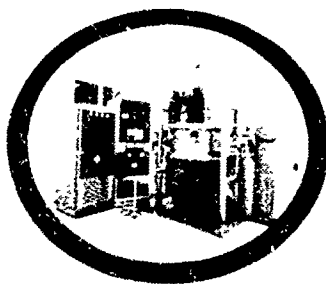
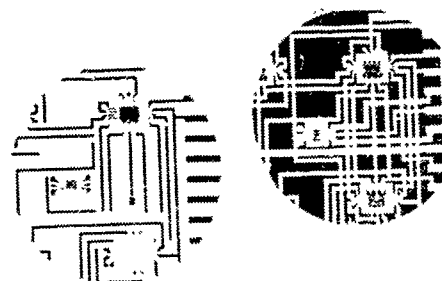
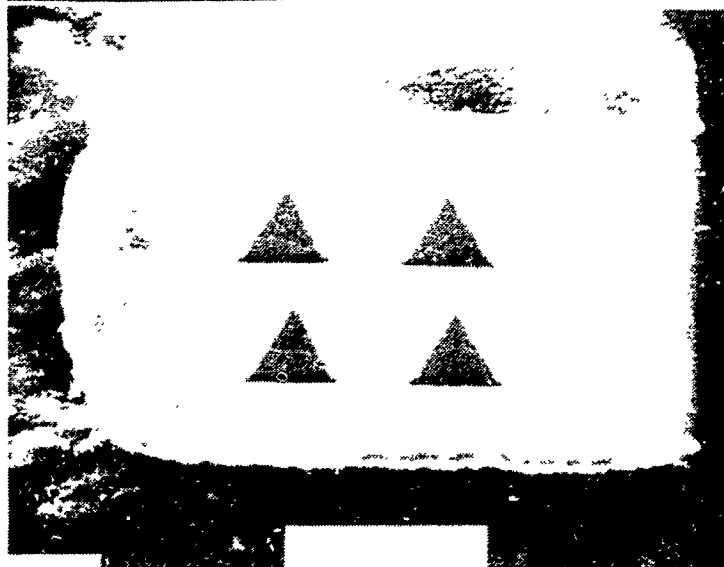
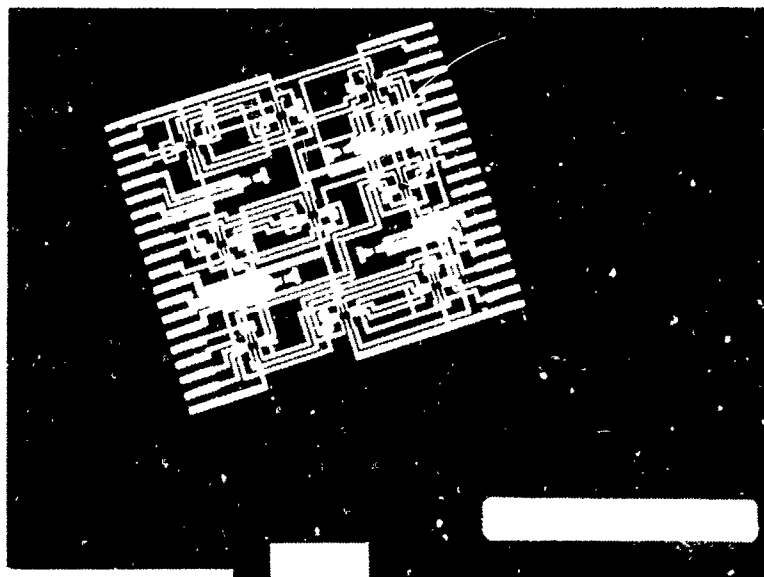
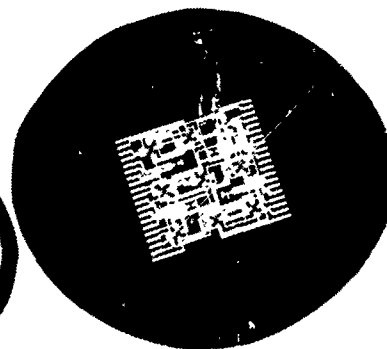
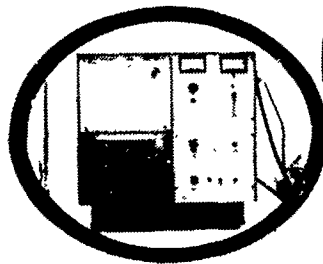
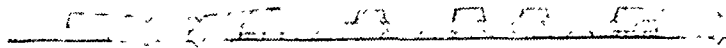
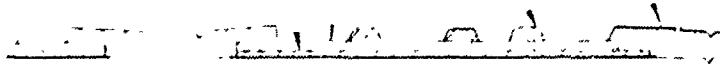


FIGURE 3







U19 1

"NODE" FEATURES

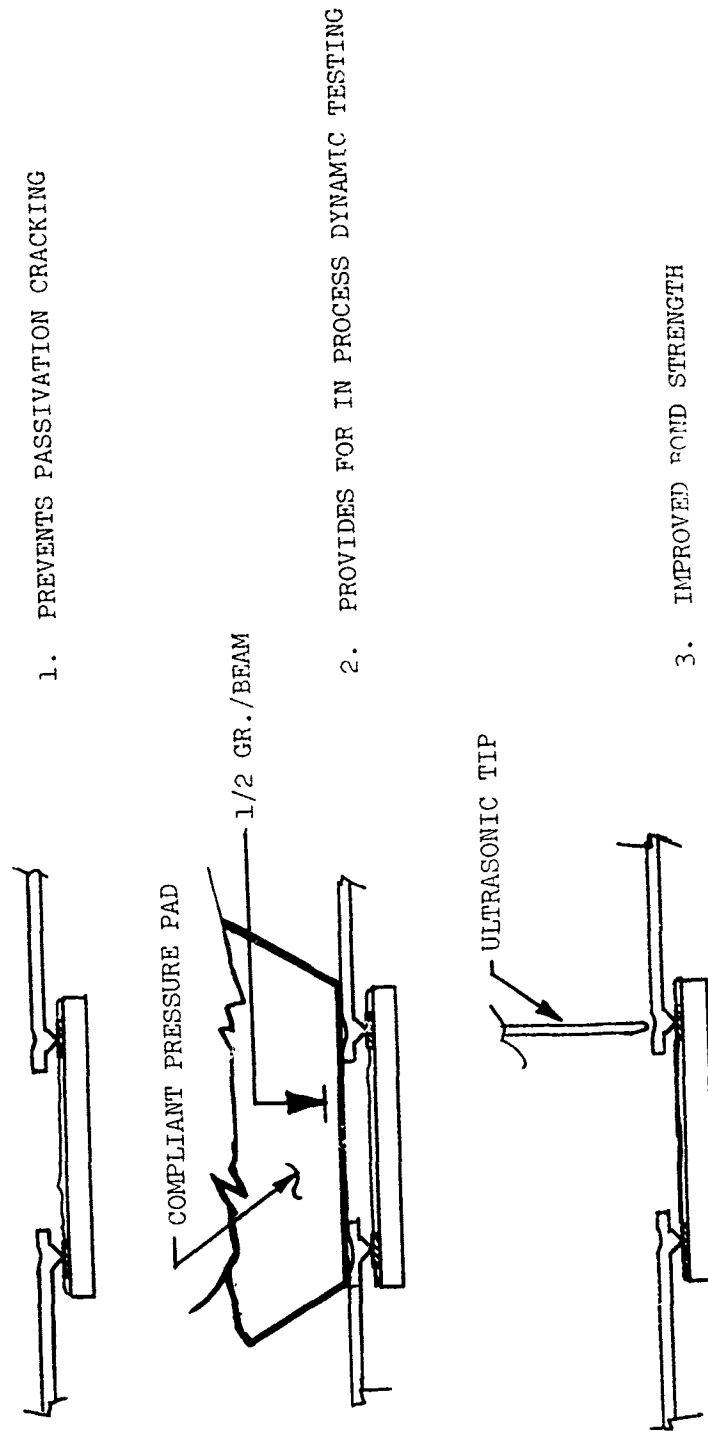
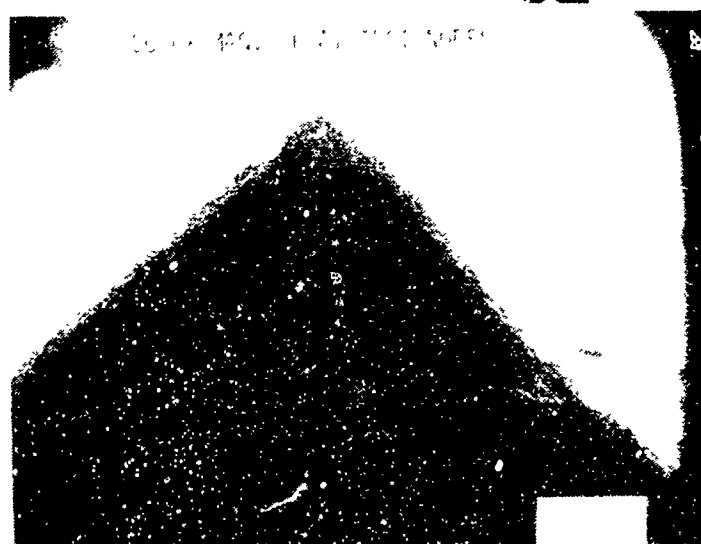
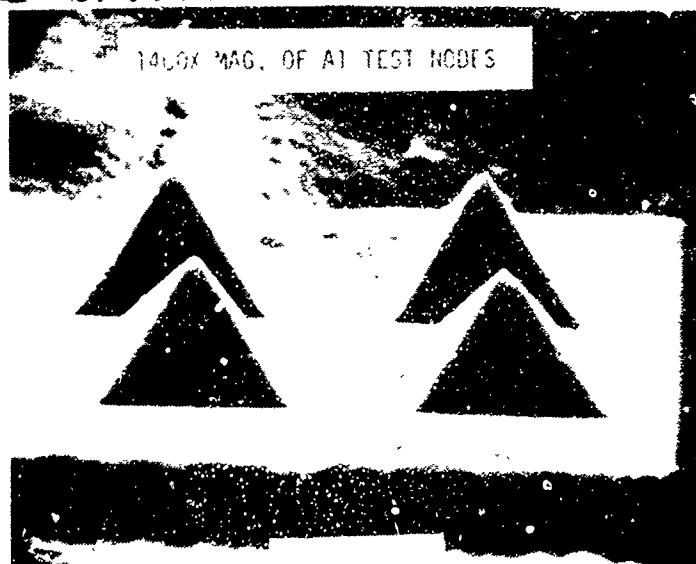
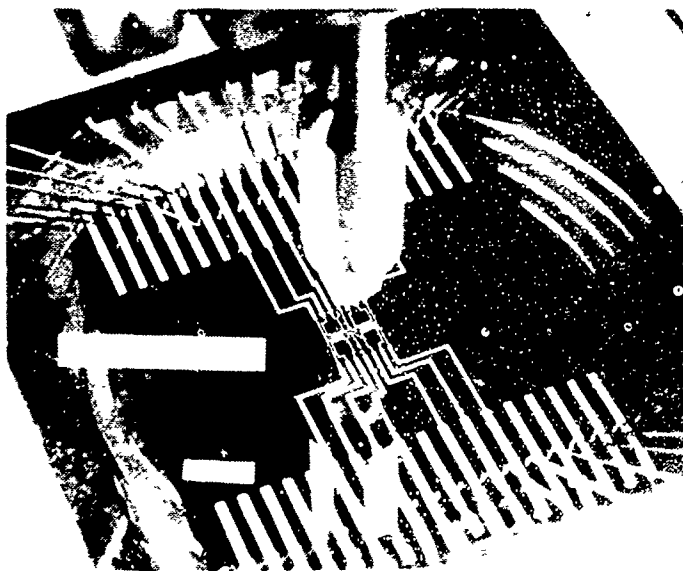
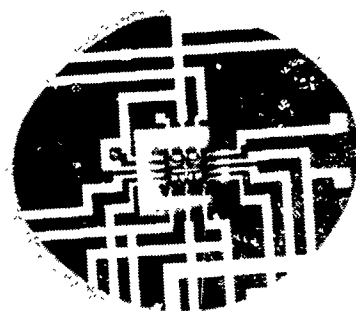
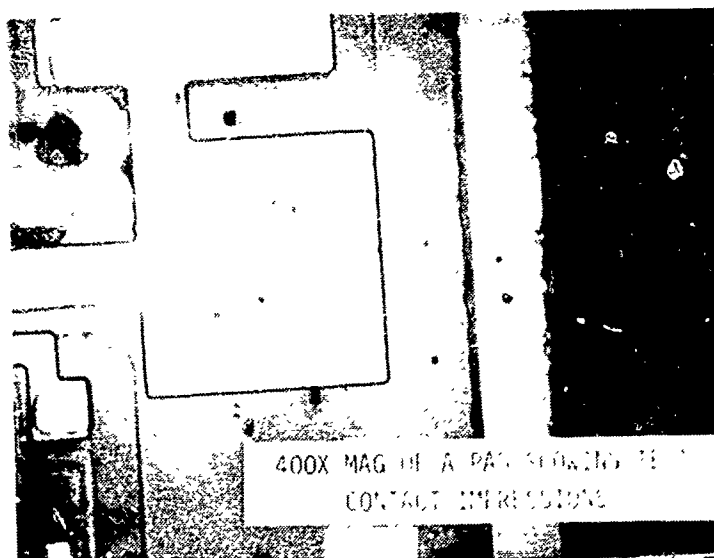
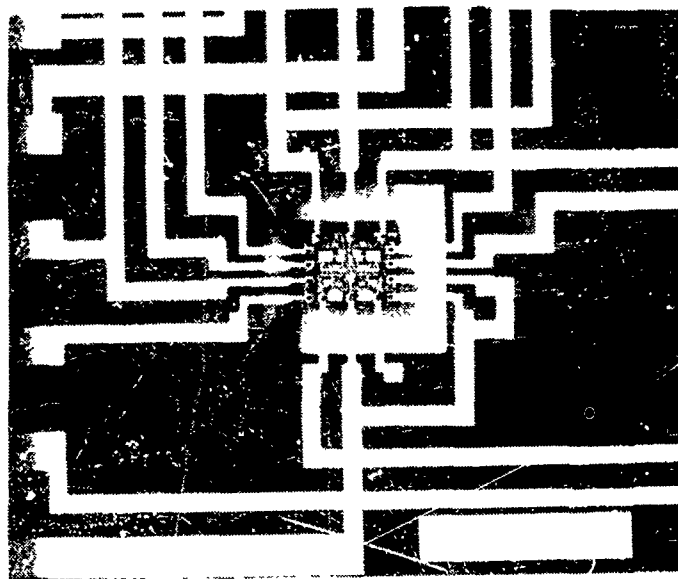
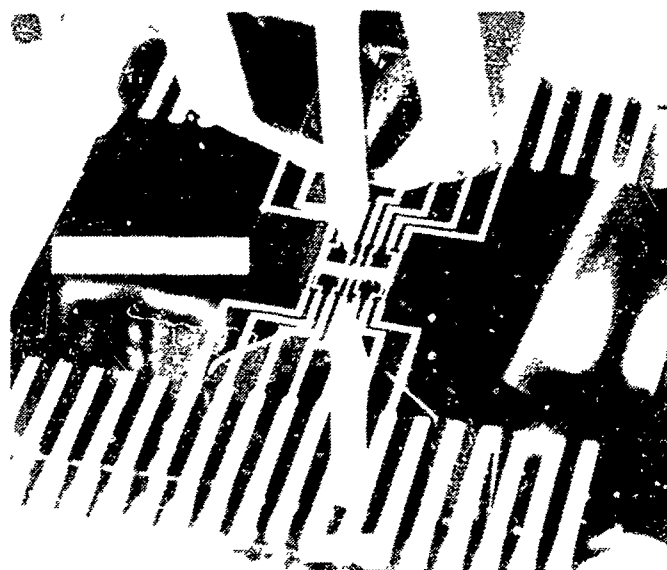
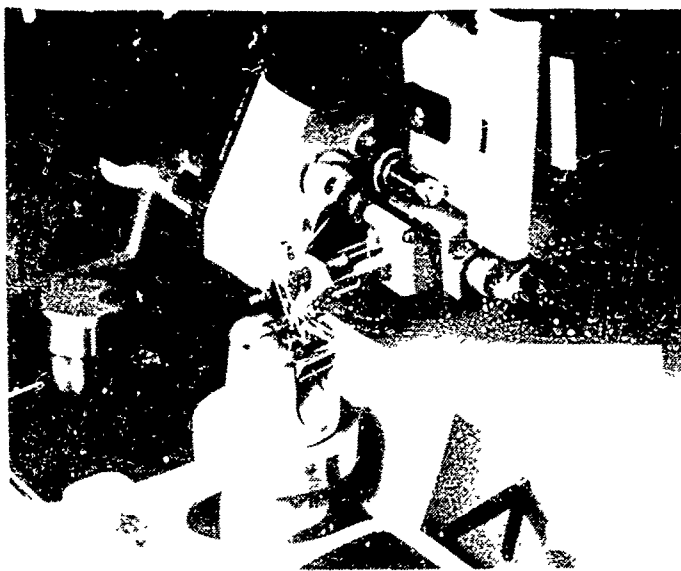
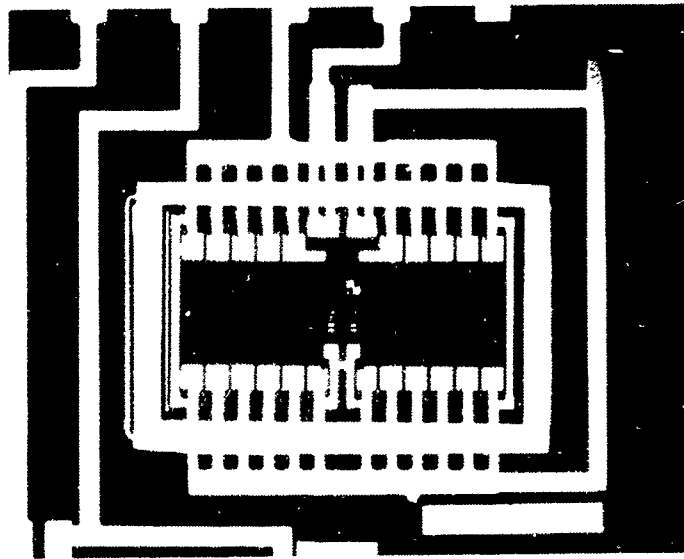


FIGURE 13









PACKAGING TECHNIQUES FOR CARBON-
MOUNTED TANTALUM CAPACITORS WITH EPOXY

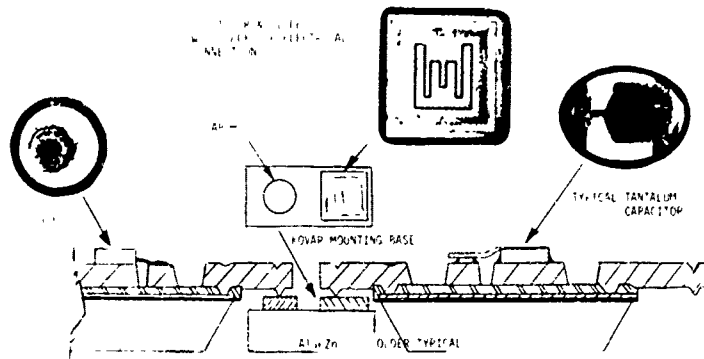


Figure 24

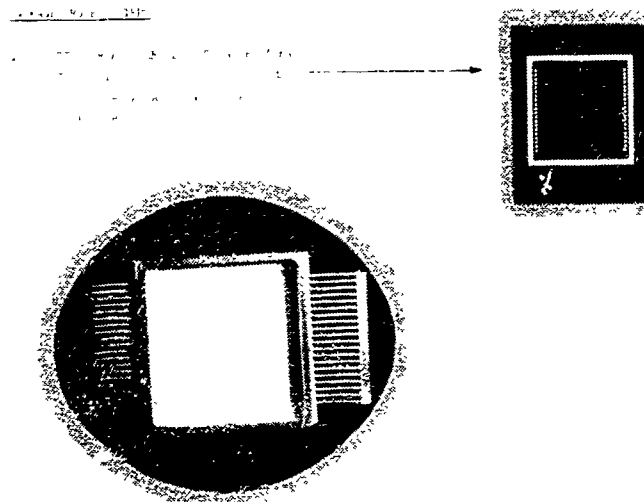
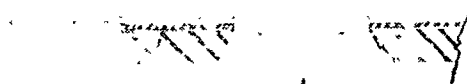
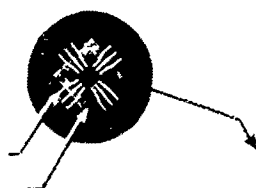
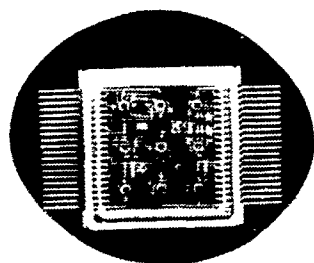
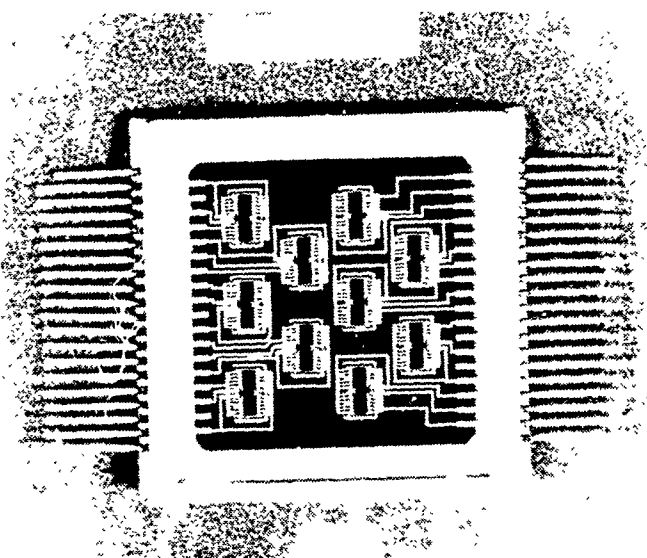
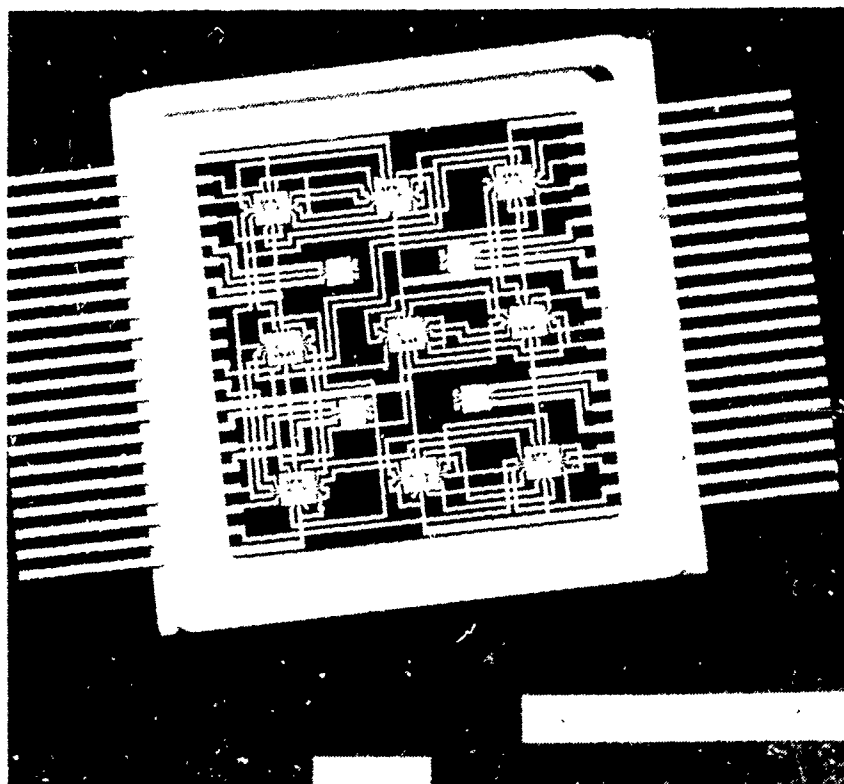


FIGURE 25





SUMMARY

PRINCIPLE ADVANTAGES

COST:

- ALL PROCESSES IDENTICAL TO THOSE USED CURRENTLY IN THE FABRICATION OF MSI DEVICES
- AUTOMATIC EQUIPMENT EXISTS FOR BEAM BONDING AND ALL PROCESS OPERATIONS
- ALL COMPONENTS CAN BE TESTED PRIOR TO COMMITMENT WHICH MINIMIZES REWORK
- UTILIZES NO PRECIOUS METALS
- FULLY REPAIRABLE
- ANY OFF THE SHELF SEMICONDUCTOR COMPONENT CAN BE USED WITHOUT SPECIAL PROCESSING.

RELIABILITY:

- INTEGRAL SPIDER INTERCONNECT AND DEVICES ARE OF THE SAME BASE MATERIAL WHICH PREVENTS THERMAL MISMATCH
- MAN MADE CONNECTIONS ARE REDUCED TO ONE-HALF THOSE IN CONVENTIONAL CHIP AND WIRE SYSTEMS
- MULTILAYER PROCESS IS BACKED UP WITH BILLIONS OF HOURS OF LIFE DATA
- MONOMETALLIC CONNECTIONS ELIMINATES POTENTIAL INTERMETALLICS PROBLEM

Figure 30a

SUMMARY (CONT'D)

PRINCIPLE ADVANTAGES

PERFORMANCE:

- SHORTEST POSSIBLE LEAD LENGTHS
- SHORTEST POSSIBLE THERMAL PATH
- FUNCTIONALLY OPTIMIZED
- HERMETIC
- LOW PROFILE (.050")
- HI-DENSITY

RADIATION:

- MONOMETALLIC INTERCONNECT MATERIAL
- NO FLYING LEADS
- "HOLE TESTED"
- COMPATIBLE WITH ALL EXISTING (AND UNDER DEVELOPMENT) RADIATION RESISTANT SEMICONDUCTOR DEVICES

Figure 30b

INTEGRAL SPIDER INTERCONNECTS (I/S/I)

KEY FEATURES

LOW COST
RELIABLE
RADIATION RESISTANT
IMPROVED PERFORMANCE

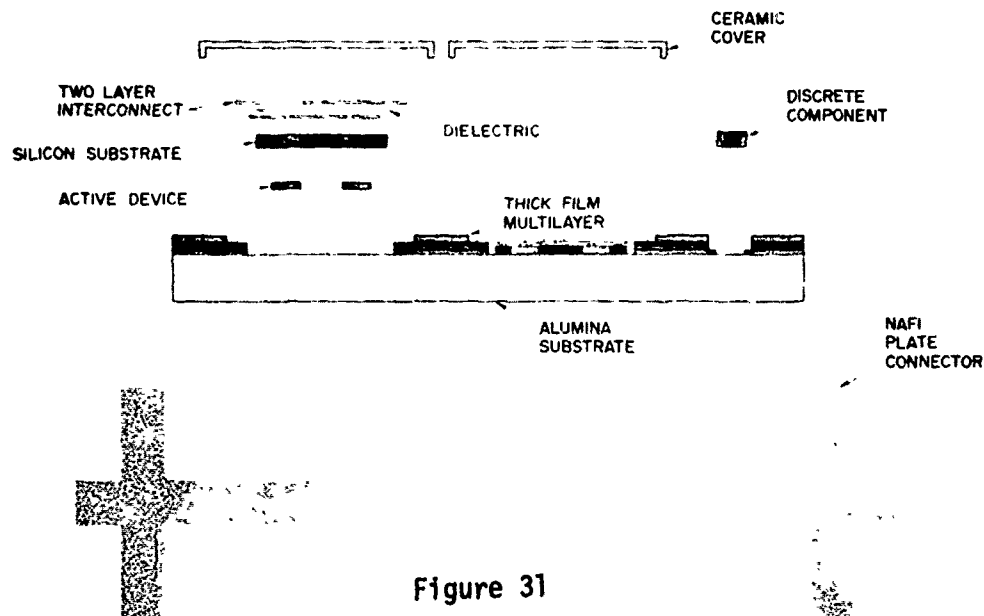
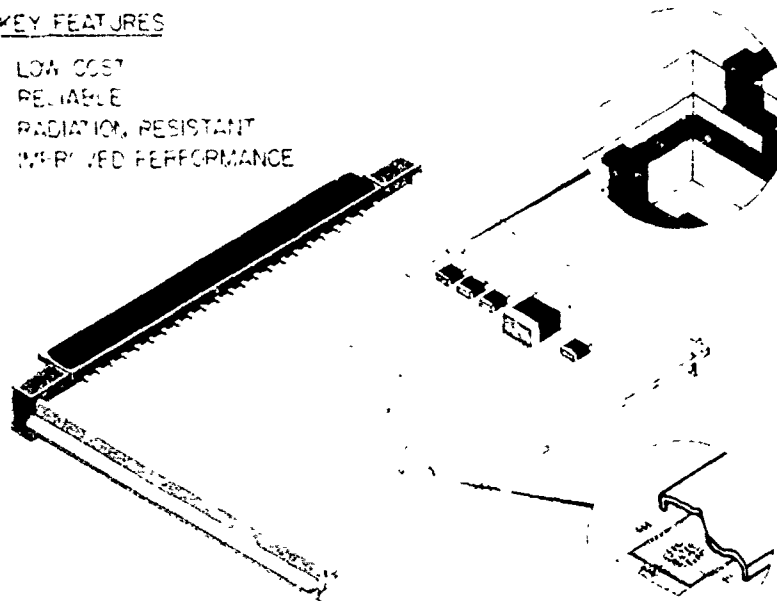


Figure 31

TECHNICAL COMPARISON OF INTEGRAL SPIDERS I/S WITH TAPE CARRIER T/C,
BEAM LEAD B/L AND CHIP AND WIRE C/W

	I/S	T/C	B/L	C/W
ADDITIONAL CHIP PROCESSING REQUIRED	NO	YES	YES	NO
NUMBER OF MECHANICAL CONNECTIONS PER OUTPUT	1	2	1	2
MONOMETALLIC	YES	NO	NO	NO
MULTILAYER	YES	YES	YES	YES
SAME SUBSTRATE AND DEVICE MATERIAL	YES	NO	NO	NO
MULTIPLE DEVICE VENDORS	YES	NO	NO	YES
THERMAL PATH	DIRECT TO PKG.	THRU SUBSTRATE	THRU BEAMS TO SUBSTRATE	THRU SUBSTRATE
RADIATION RESISTANT	YES	NO	NO	YES
HERMETIC	YES	YES	YES	YES
MFG. EQUIP. COMMERCIALY AVAILABLE	YES	NO	YES	YES
VOLUME REQUIRED PER CHIP	3-4X	6-9X	6-9X	12-16X
AREA REQUIRED PER CHIP	3-4X	2-3X	2-3X	3-4X
DISCRETE AC & DC TESTING PRIOR TO BONDING	N.A.	YES	YES	NO
FULL FUNCTIONAL TESTING PRIOR TO BONDING	YES	NO	NO	NO

X = SUMMATION OF COMPONENTS NOT INCLUDED IS PACKAGING AREA WHICH IS ASSUMED TO BE EQUAL.

FIGURE 32

HYBRID MICROELECTRONIC APPLICATION TO MISSILES

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US Army Missile Research, Development & Engineering Laboratory

US Army Missile Command

ABSTRACT

Gun fired projectiles induce severe mechanical stress on hybrid micro-circuits, often time leading to loss of guidance and control system and failure of mission. Techniques for hardening hybrid micro-circuits were developed and evaluated using centrifuge, shock and actual cannon firings.

Reduced missile and projectile size has imposed a requirement to reduce the size of control and guidance electronic packages. This has led to high density hybrid microcircuits and thus a problem with maintaining the temperature of the package within safe operating limits. Investigation has been initiated into heat source and design techniques to minimize temperature problem in microcircuits.

I. INTRODUCTION

There are two problems that are presently providing difficulties in the use of hybrids in missiles. The first is the requirement to design and fabricate gun harden hybrids (Figure 7a, b, c). The second problem is being driven by the continuing requirement of high density electronics. This high density requirement in turn produces a higher density of heat sources and heat removal becomes a critical problem. This paper deals with both high gun hardening and thermal resistance of hybrid circuitry work that is being conducted at MIRADCOM.

First, this paper reviews the performance of hybrid microelectronics in severe environmental conditions. The topic is developed by emphasis of the mechanical stresses and the techniques used to cope with them, the test evaluation techniques and the cost considerations imposed upon the circuits. The stress environment results when the projectile is launched from a 155 mm cannon. The electronics performs the tracking and flight controls to intercept a high speed maneuvering ground target. A test and evaluation plan which included centrifuge testing, shock testing and actual cannon firings provided valuable results which supported the design effort. The support of analysis laboratories during the testing provided quick turn around and implementation of demonstrated problem solutions. The performance was equally weighted with cost effective implementation to insure a product that not only performed in severe environmental conditions but was competitively priced.

In order to assure reliability of electronics in an operating environment the junction temperature must be held to a temperature lower than that specified by the manufacturers. This investigation will provide information needed by the hybrid designer in order to make calculations to within plus or minus 10%, thereby allowing intelligent designer trade-offs to be made with respect to materials and fabrication techniques. Thus, costly overdesigns or redesigns can be minimized.

The study was undertaken to determine the thermal resistance variations brought about by several common assembly techniques. Variables investigated include package styles, substrate attachment materials, chip bonding techniques, and multilayer circuitry (typical of analog circuitry). Thick film test circuits were specially fabricated for measurement of the effects of these variables.

II. GUN HARDENING OF HYBRIDS

The results of the high environmental forces imposed upon the microelectronic circuits can be seen in figures one, two and three. The high g loading which results from the shock of cannon launch can cause the failure of many different types of components and package configurations. The mounting of circuits on printed boards and the distribution of forces on the individual boards have been shown to be important considerations. The deformation of package leads rather than the package has been important for such high shock environments. The forces are both positive and negative shock along with the angular velocities associated with spinning of the round prior to fin stabilization.

The placement of components was an important design layout consideration. The mass of capacitors and other relatively large components would result in cracked substrates if unsymmetrically positioned. The overbonding of these larger components, (figure four) was also necessary to insure success in the "rattle test". (This occurred following high stress environments by shaking the package and listening for the results). The heavy platform package was chosen as the most substantial design for the packaging density required. The use of stiffeners on the package insured the most rugged container for the circuit. (see figure five).

The performance of the hybrid microelectronic interconnections was an important process control consideration. An extensive metallurgical evaluation of the soldered interconnections was performed when the worst case mechanical simulation indicated that life testing could end in sudden death (see figure six). The use of one hundred percent non-destructive wire pull testing also insured that wire bonds in circuits would be as reliable and rugged as possible. The deformation of package covers could result in electrical shorts to certain tall components. The use of insulative layers between the metal cover and these components insured proper operation of the circuits.

The current interpretation of simulation testing data helped provide information as to the ultimate strength of the packaging technologies. The ductile to brittle transistions of materials and the microstress analysis required in microelectronics were found to be important to insure program success.

The effective implementation of techniques for gun hardening of hybrid microelectronic circuits starts with a careful analysis. A design review with representatives from different disciplines of engineering was called to analyze standard fabrication techniques. Emphasis was placed upon substitutional changes to the standard process rather than initiation of completely new types of process technology. The design review provided a forum for the structuring of a test and evaluation sequence for process technologies defined as critical risks.

The application of centrifuge step-stress testing provided a valuable method to evaluate package designs and bonding materials. The effects of high accelerating forces (30 to 50 kg's) along specified axis directions provided valuable information as to the merits of different surface preparations and basic bonding techniques. The sensitivity of very rugged packaging designs to slight unbalances in the force distribution indicated the important considerations in symmetric placement of components. The benefits of improved flatness and homogenities of substrates were significant parameters. The step-stress to failure (rattle test) became a valuable method to identify the best adhesive material and its safety margin. The testing of improved adhesives and optimum attachment techniques required very careful analysis because of microcracking and minor component displacements which manifested itself as intermittent operation at temperature extremes. The use of dye penetrants and examination with optical and electron microscopes were necessary for accurate assessment of the stress extent of specific testing sequences using the centrifuge.

The results of constant acceleration centrifuge testing were evaluated and used as a baseline for the next phase of the test sequence. The use of modern facilities of dynamic testing in specially calibrated and maintained shock machines were another valuable testing procedure. The testing of hybrid circuits in shock environments showed the deficiencies in product design and material compatabilities with no doubt as to the weak link in the design concept. The senstivity of brittle materials in tension and their corresponding strength in compression became major design consideration for rugged microelectronic circuits where smaller size and higher strength were constant tradeoffs. The compound forces produced by spinning, and both positive and negative shock waves traveling through the components were difficult to simulate with accuracy. The shock testing of environmentally screened circuits was a necessary testing sequence to ensure reliability for both electrical and mechanical considerations. This required careful tradeoffs as to burn-in and bake temperature and their consequent affect on the mechanical reliability of bonding and interconnections in such high shock environments.

III. THERMAL INVESTIGATION

This investigation has two objectives: The first is to provide thermal resistance data on package and attachment methods for hybrid microcircuits. The goal is not to determine the thermal resistance for each specific microcircuit for the following reasons: One, hybrid microcircuits are very often used for applications requiring only very small production runs making it too expensive to analyze or measure each specific design type to determine its exact thermal resistance. Two, because of many heat sources and hot spots possible within a hybrid microcircuit, the determination of its thermal resistance is more complex and expensive than a similar effort on behalf of a single packaged semiconductor die.

The data to be obtained from this effort will be for specific package types and specific construction techniques and certain materials. Hence, the microcircuits will be categorized into groups characterized by features which limit the thermal resistance to a narrow range of values. The objective is to provide thermal resistance values for the most used categories of microcircuits for high reliability government systems. In this manner, much more accurate information will be obtained without the expense of determining thermal resistance for every hybrid microcircuit design.

The variation in hybrid microcircuits which most influence thermal resistance are:

- (a) Package type
- (b) Substrate to header attachment method and material
- (c) Die to substrate attachment method and material
- (d) Whether die is attached directly to a metal pad on the substrate or is separated from the substrate by a multilayer sandwich of dielectric and metal.

System or circuit constraints often dictate package type, die mounting location (on top of multilayer or on metal substrate pad), and die attach method. Eutectic attachment is often required for low collector to emitter saturated transistor voltages. On the other hand, rarely do such constraints dictate substrate to header attachment process. Consequently, in order to get the most useful information with the budget available, this effort has been limited to the following: determination of the thermal resistance for design types involving four package types, two die attachment methods, and two die locations (on top of multilayer films and on a metal substrate pad). This will require determination of thermal resistance for 4 x 2 x 2 or 16 categories of hybrid microcircuits as shown in the table below.

HYBRID MICROCIRCUIT DESIGN TYPES BUILT AND
INSTRUMENTED FOR MEASUREMENT OF
HEAT GENERATING SOURCES

Die Pad Location	On Top of Multi- layer Dielectric Films		On metal Pad Printed Directly on the Substrate	
	Eutectic	Epoxy	Eutectic	Epoxy
Die Attachment				
32 Pin, 1 inch Square Flat Pack	3 each H214-1	3 each H214-2	3 each H214-3	3 each H214-4
26 Pin, 3/4 inch Square Flat Pack	3 each H215-1	3 each H215-2	3 each H215-3	3 each H215-4
24 Pin, Double Width Dual-in-line	3 each H216-1	3 each H216-2	3 each H216-3	3 each H216-4
16 Pin, Double width Dual-in-line	3 each H217-1	3 each H217-2	3 each H217-3	3 each H217-4

Three samples of each of the sixteen categories have been fabricated for test to permit some statistical averaging of data and to help detect any aberrations. The test mode represents a worst-case situation where all the power dissipation is concentrated on one semiconductor. This mode of operation will provide a worst-case thermal resistance value. When this figure is used in designing hybrid microcircuits, it will assure the designer that he is within safe operating limits.

Presently, the assembled hybrids are undergoing calibration over the required temperature range. Every junction in every package is being calibrated using the V_{be} method with a constant current source limited to 1 MA. A V_{be} vs. temp curve is being drawn on each device so that junction temperature can be read off the graph during the actual testing.

The second objective is to develop thermal models of heat generating devices, active and non-active mounted on hybrid substrates. Valid mathematical models will be used for computer simulation for calculations of thermal resistance for heat generating devices on hybrid microelectronic structures. The availability of these models will lead to employment of computer aided layout and design, incorporation thermal, electrical and topographical criteria in substrate circuit designs. Assurance of long life circuit reliability, based upon proper operating temperatures

could therefore be realized early in design stages. These models must satisfy the following requirements:

1. They must give accurate predictions of actual operating temperatures. For this reason, experimental measurements will be made for model verification.

2. The models must not be overly complex. This would require expensive computer time and/or memory for simulation as well as programming effort. They must also be adaptable to computer-aided-design systems, such that the layout designer need only to input a minimum of dimensions, material parameters, etc. into the computer.

3. The models of individual devices must be capable of being integrated into overall thermal models of actual hybrid circuits.

Three basic hybrid test units have been designed and fabricated. These three types of units are for experimental study of transistor chips (Figure 8), paste resistors (Figure 9), and chip resistors, (Figure 10), respectively. Variations, such as device mounting techniques, resistor trimming methods, etc. are included within the basic units. These units are for experimental verification of mathematical models to be simulated on the computer.

A temperature measurement facility is completed with appropriate fixtures and instrumentation. This facility uses both diodes and thermocouple probes (Figure 11) as temperature sensors, so that experimental cross-checks can be made. Calibration of the diode sensors, located on the hybrid test units, is in progress.

A mathematical thermal model of the test unit incorporating paste cermet resistors has been formulated, using finite-difference techniques. This will soon be studied on the computer, with results compared to experimental measurements.

Probing of the hybrid structures with thermocouple probes causes thermal loading problems such that the indicated surface temperatures are generally somewhat lower than the actual operating temperatures. Without correction, this gives erroneous probe readings. The tiny diodes on the hybrid substrate give excellent accuracy of their corresponding surface temperature measurement, but lack the mobility of thermocouple probes. There is also a problem of precisely locating the probes on the substrate.

Two methods of increasing probe measurement accuracy are in the process of being implemented. The first involves determining a correction factor by calibrating the probe against the diode sensors at locations symmetric to the diode locations. The second is a unique method showing promise of being even more effective. Differential variations of heat sink temperatures will be made, when variations of hybrid device dissipation are applied, in such a way as to keep the probe reading constant. Hence

probe loading is also maintained constant. Thermal resistance from hybrid heat source to heat sink is then determined on an incremental basis. Heat sink temperature will be controlled electrically by thermoelectric modules.

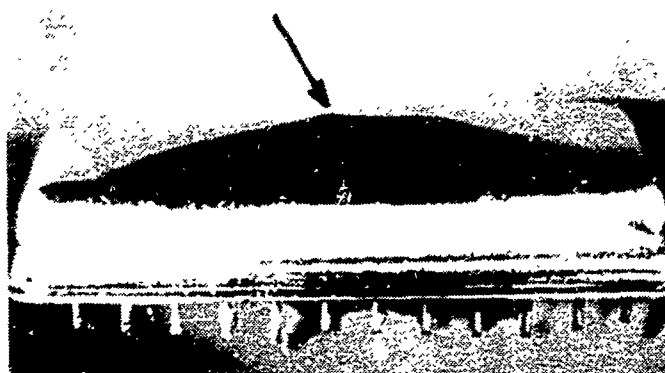
A micrometer positioner will be used to accurately position probes, This will consist of a modified electrical probe mechanism and magnifier arrangement.

Completion of thermal measurements as well as modeling and computer simulation will be made for all three basic types of test units, as well as for all variations within the types. The resulting experimental and analytical data will be compared to test validity of the various thermal models used. Based upon this data, several important results are expected to be revealed. Among these are:

- a. Improved material and mechanical structures, including layout on substrate, that enhance heat removal.
- b. Specifications of improved thermal measurement techniques that are implemented without overly complex and expensive instrumentation, while maintaining accuracy.
- c. Simplifying assumptions that will lower mathematical model complexity and still give useful and accurate thermal resistance results.



Figure 1 Depressed Lid



DIMPELED CAN

Figure 2

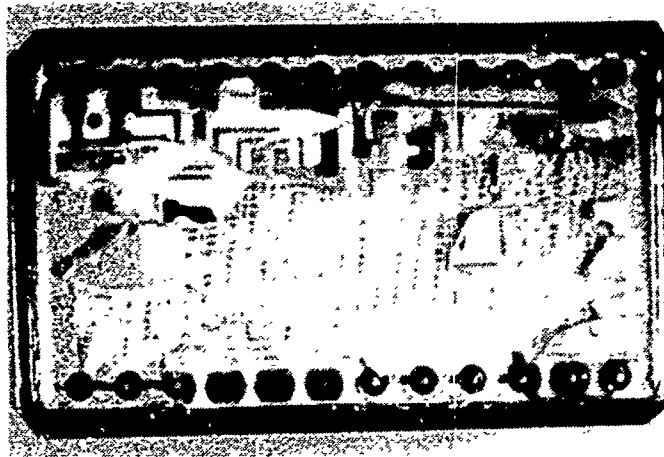


Figure 3 Cracked Substrate

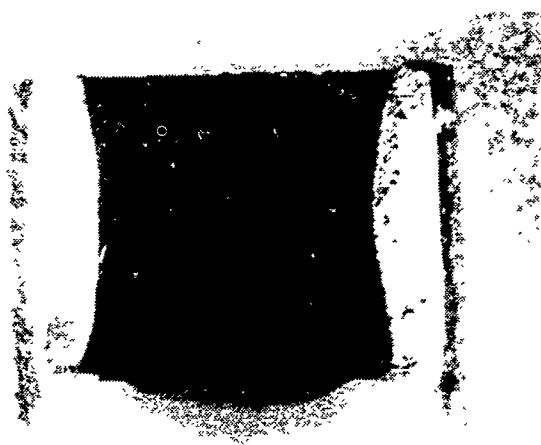


Figure 4 Overbonded Capacitor



Figure 5



Figure 6 Cracked Solder Joint

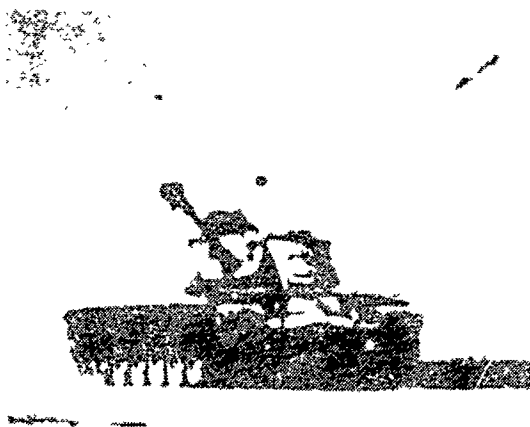


Figure 7a Results of Gun Hardened Hybrids

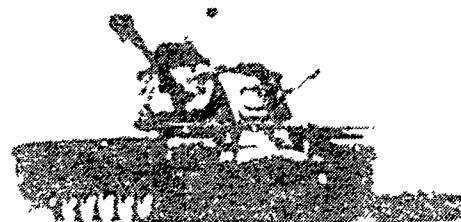


Figure 7b



Figure 7c

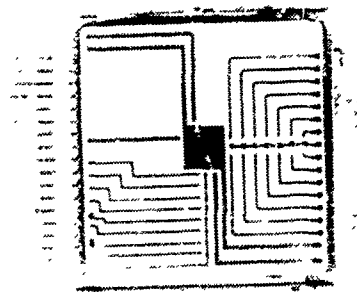


Figure 8 Transistor Chip

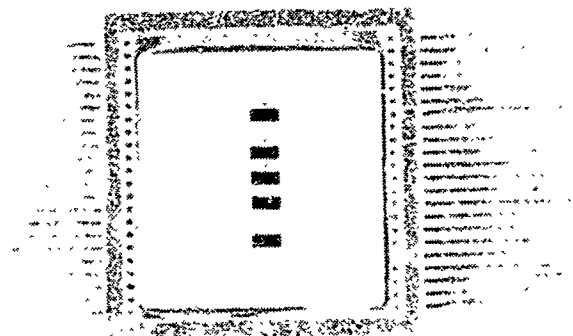


Figure 9 Thick Film Resistors

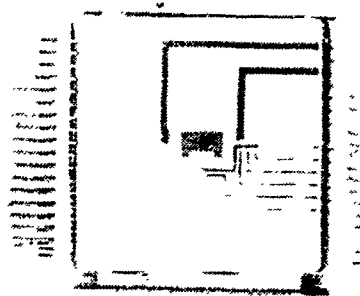


Figure 10 Chip Resistor

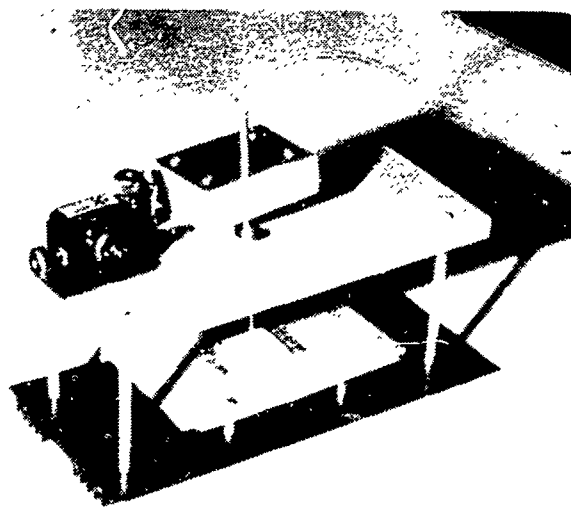


Figure 11 Temperature Measurement Facility

RUGGEDIZED HYBRID MICROCIRCUITS

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ABSTRACT

An investigation was conducted of assembly and packaging techniques to ruggedize hybrid microcircuits to withstand artillery launching and impact shock of 30,000 g. The ECOM applications require small, lightweight circuits that exhibit high stability and reliable operation after impact. Areas of investigation include material selection, circuit assembly, and overall packaging considerations. Design and fabrication techniques presented in this paper are suitable for high shock hybrid microcircuits.

INTRODUCTION

The majority of the hybrid microcircuits used by the military are not exposed to extremely harsh mechanical shock conditions. ECOM has special applications that require circuits to operate in this environment. This paper gives the results of an investigation of packaging and assembly techniques for hybrid microcircuits capable of withstanding a high g shock. The techniques are applicable to ECOM electronics that are to be field delivered by artillery with one application being Remotely Monitored Battlefield Sensor System (REMBASS) packages. The mechanical shock requirements are 16,000 g in a 4.5 millisecond time period and 30,000 g in a 6 millisecond time period with certain reduced electrical requirements allowed for the higher shock. There are also spin and radial acceleration requirements based on firing from a 155 millimeter howitzer.

These high g shock environmental requirements have been simulated by the use of an air gun situated at Picatinny Arsenal, Dover, N.J. Mechanical shock with nominal peak amplitude of 10,000, 20,000, and 30,000 g was applied normal to the test units. This force was also applied 90° from normal to simulate the spin and radial acceleration requirements. Figure 1 shows the acceleration and shock time for a typical 20,000 g shock for the air gun at Picatinny Arsenal. The time period is 0.25 to 0.5 milliseconds. The actual expected field conditions of 4.5 milliseconds could not be simulated in this air gun.

The principle areas reported on are (1) overall packaging methods, (2) bonding of chips to substrates and substrates to headers, (3) wire interconnections, and (4) thick-film resistors. Throughout this investigation no use was made of any type of coating on the chips or wires because of the possible effect on reliability. The application of these units requires that they operate reliably for a period of time after they have been artillery delivered.

Packaging: An evaluation of packages normally used for hybrid circuits was conducted to determine their ruggedization capability in a high g environment. It was determined early in the investigation that these packages would not withstand the high g shock requirements. As a result, a different packaging concept was evolved. Figure 2 shows the common header package assembly. The package itself is constructed from one piece of aluminum machined such that a ceramic substrate can be placed on each side of the header. This type of construction accounts for its high resistance to shock. Aluminum was chosen because of its machinability and high strength to weight ratio. The wall thickness is 40 mils* and the header thickness is 30 mils. These values were experimentally determined to be the minimum that could withstand the 30,000 g mechanical shock. External connections are made through the end of the package via glass bead feed throughs. Substrate to substrate interconnections are also made via glass bead feed throughs, not shown in Figure 2, passing through the header. For the sensor application, a printed circuit board and connector are located on the top of the package. The two 25 mil thick substrates with thick-film and chip components are bonded to the aluminum package header. The aluminum lids, 26 mils in thickness, were attached to the package lip. This paper covers both solder and epoxy bonding for these attachments and describes how the bonds withstood 30,000 g mechanical shock. This packaging concept was found to be satisfactory for the 30,000 g mechanical shock and probably would be good for higher level shocks, if necessary. Figure 3 shows how the package can be encapsulated along side an open unit. The encapsulation was used around the enclosed unit to fit into a particular geometry. The encapsulation material did not contact any of the circuitry portions.

Even through this packaging concept is rugged, it was necessary to investigate other means of packaging to improve cost effectiveness. With reduced cost in mind, the packaging concept shown in Figure 4 was studied. This design has the two ceramic substrates bonded back to back using thick-film metallization for circuit interconnection and external connections. The circuitry would occupy the substrate area protected by the aluminum caps. This package was tested at 10,000, 20,000, and 30,000 g. It was determined that this packaging concept was good to g levels of 20,000 but failed at 30,000 g. Figure 5 depicts the results of this packaging scheme for a 30,000 g mechanical shock. The center of the substrate, which naturally has the most flex, cracked causing fractures to propagate in all directions. Also, in many of the tests, breakage occurred at the junction of the substrate and aluminum cap.

Bonding: Figure 6 shows the common header package and a test substrate with chip capacitors and chip enclosures attached. Various methods of capacitor chip attachment were investigated using conductive epoxy, non-conductive epoxy, solder, or combinations of these. Attempts to use solder alone resulted in a high number of failures due to capacitor breakage, normally through the center of the component. The other methods attempted successfully withstood the 30,000 g shock. The most satisfactory method for chip capacitor attachment was solder for electrical connection with epoxy used along both sides of the capacitor for reinforcement.

*See last page for metric equivalent units.

A liquid single-stage epoxy was used for the reinforcement and a solder (tin, lead, silver) was used for electrical connection. Another technique using epoxy with wire electrical connections was also satisfactory but caused assembly problems because the epoxy had to be applied before the thermocompression bonds. The integrated circuit chips were attached using a silicon gold eutectic solder. These chips cannot be seen in Figure 6 because they are within the enclosures. Thick-film interconnections were used to connect components on the substrate to those components inside the chip enclosure. Two layers of dielectric were used to insulate the thick-film interconnections from the metallized enclosure. Satisfactory operation under the high g shock was verified by before and after electrical tests of the enclosed integrated circuit chips (741 operational amplifiers). These enclosures were used so that the active devices could be hermetically sealed thus allowing the use of high strength epoxy for bonding passive chips to the substrate and for bonding the substrate to the common header. The enclosures were originally attached with solder only. The arrangement did not withstand the 30,000 g shock. With solder attachment and epoxy reinforcement (Figure 6) results were completely satisfactory under the shock conditions.

Throughout the investigation it was consistently found that attachment of chips and substrates with epoxy was satisfactory for the high shock environment; however, some failures occurred as shown in Figure 7. In this case, the packages were not tightly held by the test fixture resulting in a greater shock than would normally be expected from the air gun. Figure 7a shows the substrate torn away from the header which was one of the few cases where the substrate did not remain attached. Figure 7b shows two small pieces of substrate torn away from the header. The two capacitors bonded to these small areas of the substrate remained attached and were embedded in the test jig. The epoxy used throughout the investigation for substrate attachment was a glass impregnated preform type.

Wire Interconnections: This investigation was made to determine the type of wire, gold or aluminum, and the size of wire, length and diameter, that could withstand the high g shock environment. Two basic tests were used to determine wire strength in this environment.

In the first test, the force direction tended to deform the wires downward onto the substrate while in the second test the force was applied in a direction that would deform the wires sideways. Figure 8 shows the failure modes that were defined for these tests. Figure 8a illustrates the wire being deformed in a downward direction. The definition of failure is a deformation sufficient to short a conductor that would be between two bonding connections. Figure 8b illustrates the definition of failure for wire movement in the sideways direction which would be caused by spin rotation of the artillery shell. A wire movement of 5 mils was defined as a failure, because this was the nominal distance between pads on the specific integrated circuit chip used in our application. In all cases, the wire length was measured from bond to bond and was not the loop length of the wire. All gold wires were attached using a K&S thermocompression bonder model 478, and the aluminum wires were bonded using a K&S ultrasonic bonder model 484. Figure 9 shows one of the test substrates used for this wire experiment. A force of 33,000 g was applied

in a direction which tended to deform the wires downward onto the substrate. Different lengths of wire (25, 35, 50, 75, and 100 mils) were bonded on this substrate. Aluminum and gold wires were alternately placed across the substrate. Each wire on the substrates was examined using a microscope after the high shock. In Figure 9, the gold wires are shown flat against the substrate while the aluminum wires remained in their approximately original looped position. These results are not obvious from the photograph, but note that the light reflection from the whole length of the gold wires indicates that they are flat, whereas the light reflection from only a small portion of the aluminum wires shows they are still in their original looped condition.

Figure 10 summarizes the results obtained from this part of the experiment. The results shown in the top portion are for a 33,000 g shock applied downward onto the wires. For the 1.0 mil diameter aluminum wires, there were no shorting failures for any length from 25 to 100 mils, but there were two bond failures. For the 1.0 mil diameter gold wires, there were no failures for wires of 25 mil length. For 35 mil length, approximately 25% of the wires failed and for wire lengths of 50 mils and greater there were practically 100% failures. For gold wires of 0.7 mil diameter, not shown in Figure 10, all the 35 mil length and longer wires failed.

The lower portion of the figure shows results for a 27,000 g shock applied in a direction to deform the wires sideways. For the 1.0 mil diameter aluminum wires there was slight movement for lengths of 50 mils and movement of 5 mils or greater for wire lengths of 75 mils and longer. As indicated, one 50 mil aluminum wire broke. For the 1.0 mil gold wire, there was slight movement of the 35 mil lengths and 10 mils or greater movement for wire length of 50 mils and longer. For gold wire of 0.7 mil diameter, not shown in Figure 10, there was a slight movement of 35 mil wire lengths and 7 mils or greater movement for wire length of 50 mils and longer.

Thick-Film Resistors: An experiment was conducted to determine the stability of thick-film resistors as a function of the high g shock environment. Figure 11 shows the arrangement that was used for the thick-film resistor experiment. There were a total of 72 thick-film resistors on each substrate. Of these 72 resistors, 18 were left untrimmed, and groups of 18 were trimmed 8%, 25%, and 67%. Of the trimmed resistors, half were straight cut and half were L cut. Measurements were made after fabrication. The resistors were then trimmed and remeasured two weeks later. Measurements were made just prior to the shock which occurred two months after the initial set of readings and just after the shock.

The resistance change as a result of this shock, was small compared to the changes that took place during the initial two months of aging, except for the cracked substrates which resulted in very large resistance changes. Results for 1 k ohm/square resistivity paste were as follows:

AGING - TWO MONTHS

<u>Amount of Trim (Laser)</u>	<u>Percentage of Resistors Changing Greater than 0.1%</u>
67%	70%
25%	40%
8%	30%
No Trim	30%

As a result of the shock, less than 1% of the resistors changed greater than 0.1%.

Conclusions

This paper described experiments conducted to determine materials and fabrication techniques suitable for ruggedizing hybrid microcircuits. The common header package consistently withstood the high g shocks. The best results for capacitor bonding were obtained by the use of epoxy for strength and solder for electrical interconnections. The integrated circuit chips were mounted by eutectic bonding which was determined to be satisfactory. Chip enclosures were attached with solder and were reinforced with epoxy. For substrate to header bonding, the glass impregnated epoxy preform gave excellent results. For circuit interconnection, 1 mil gold wire is satisfactory as long as the bond to bond length is kept to 25 mils. If longer gold wire is used, specific precautions should be made for any cross-over situation; that is, a dielectric film should be used between the gold wire and any lead underneath. Aluminum wire was found to be sturdy for lengths up to 50 mils. However, there were cases where the bond failed or the wire broke as a result of the shock. The resistance change of thick-film resistors due to shock was small compared to initial aging for the 1 k ohm/square resistivity paste.

Acknowledgements

The authors wish to thank their colleagues who helped them with this investigation; particularly Bill Weintraub, who has recently retired, for his thick-film work; John McCarthy for his many hours of thick-film resistor measurement; and a special thanks to Ed Malecki who took care of our needs for wire bonding chip mounting, and substrate attachment.

<u>METRIC EQUIVALENT UNITS</u>			
<u>Mils</u>	<u>mm</u>	<u>Mils</u>	<u>mm</u>
0.7	0.0178	25	0.635
1.0	0.0254	26	0.66
5	0.127	30	0.762
7	0.178	35	0.889
10	0.254	40	1.016
12	0.305	50	1.27
15	0.381	75	1.905
		100	2.54

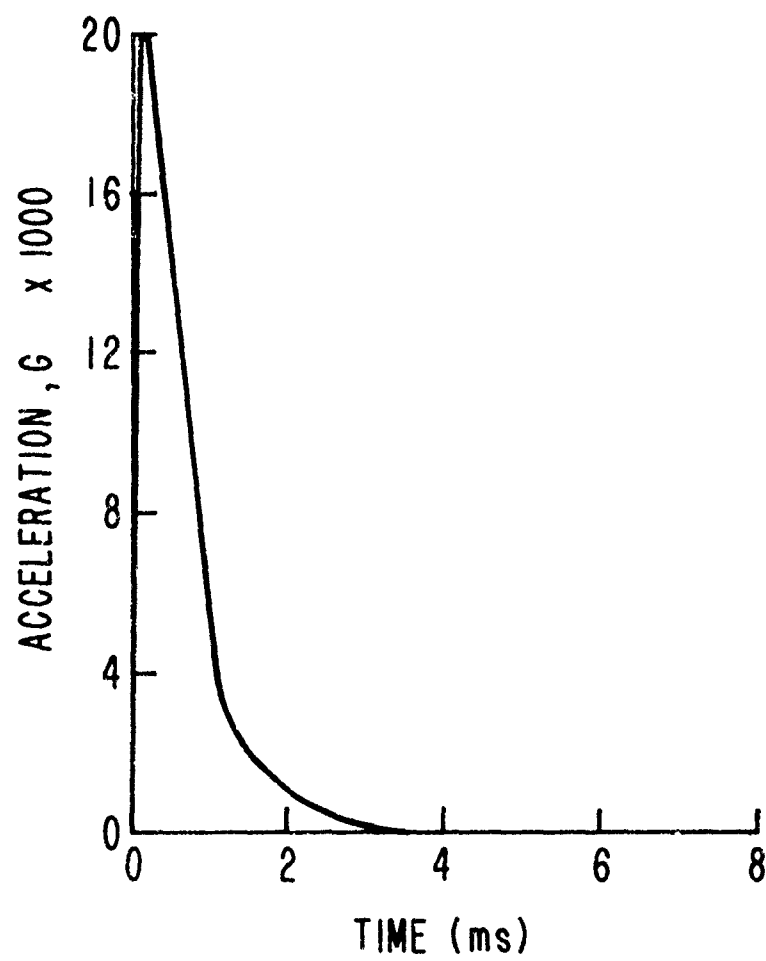


FIGURE I AIR GUN SHOCK

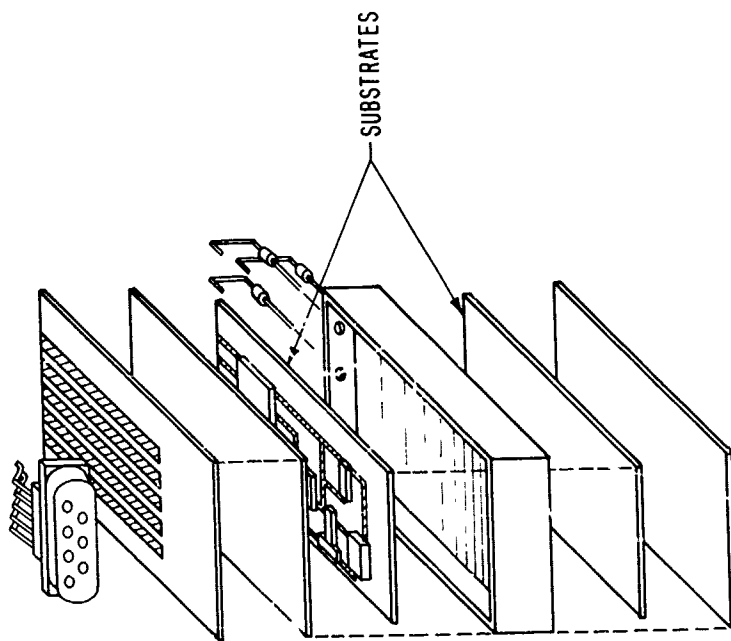


FIGURE 2 COMMON HEADER PACKAGE

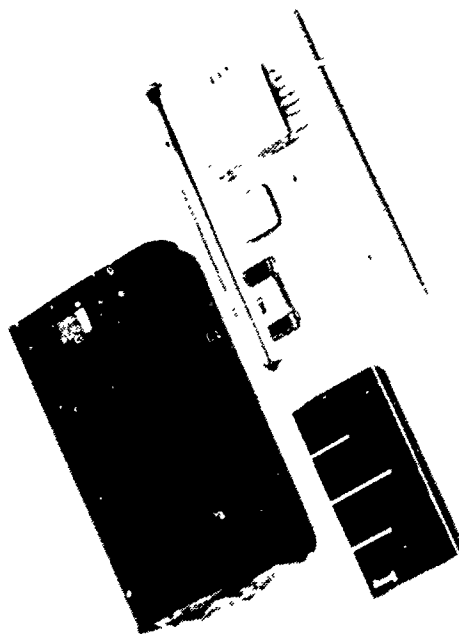


FIGURE 3 ENCAPSULATED & NONENCAPSULATED PACKAGE

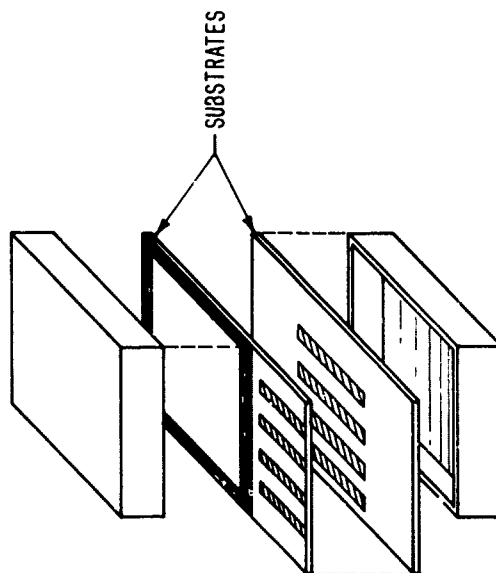


FIGURE 4 BACK-TO-BACK PACKAGE



FIGURE 5 BACK-TO-BACK SUBSTRATES
AFTER 30,000g SHOCK

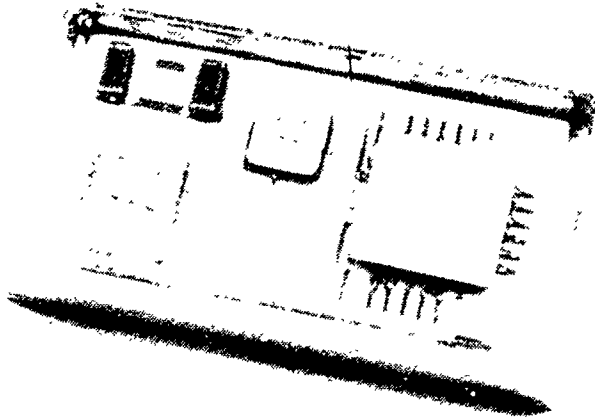
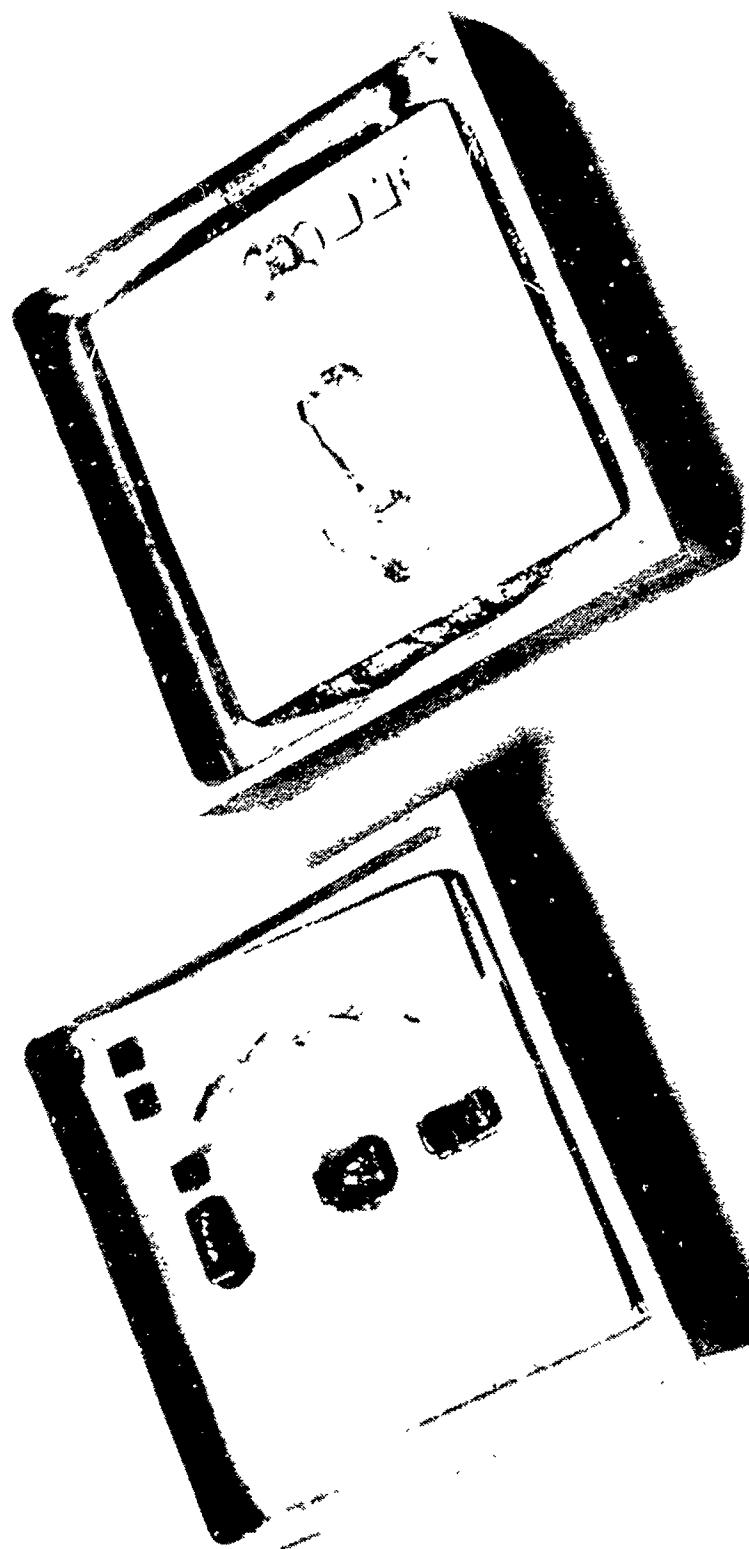


FIGURE 6 BONDING TECHNIQUES



B

A

FIGURE 7 SUBSTRATE FAILURES

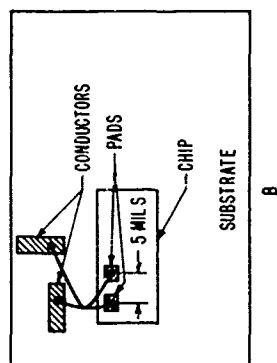
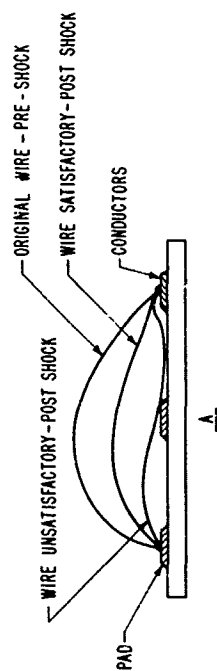


FIGURE 8 INTERCONNECTION WIRE FAILURE MODES

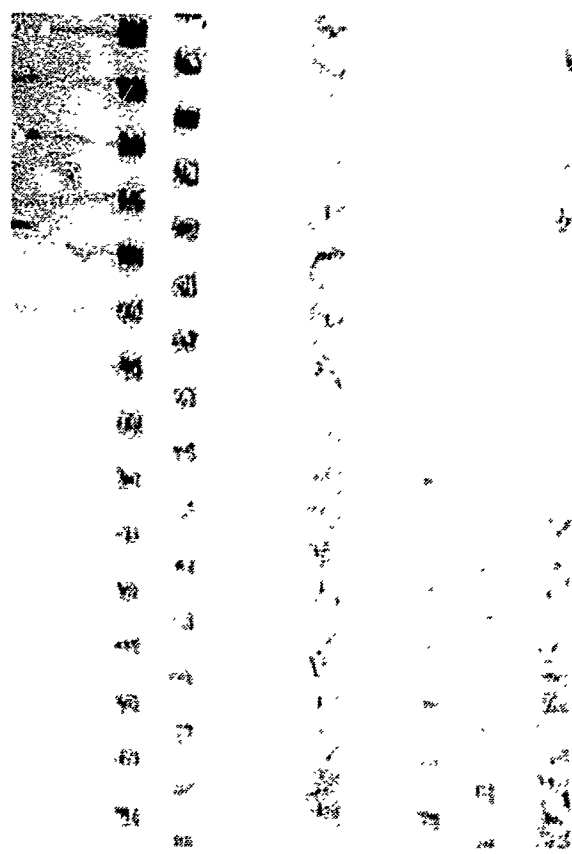


FIGURE 9 WIRE EXPERIMENT RESULTS

FIGURE 10 WIRE INTERCONNECTIONS VERSUS MECHANICAL SHOCK

Wire Length (mils)	<u>ALUMINUM</u>			<u>GOLD</u>		
	No. of Wires	Failures		No. of Wires	Failures	
25	62	0		57	0	
35	63	0		56	14	
50	53	0		48	47	
75	53	2*		48	48	
100	52	0		48	48	
*Bond came loose Shock: 33,000 g down onto substrate Wire Diameter: 1.0 mil						
Wire Length (mils)	No. of Wires	Maximum Wire Deflection		No. of Wires	Maximum Wire Deflection	
25	29	0		32	0	
35	31	0		31	Slight	
50	32	Slight**		32	10 mils	
75	32	5 mils		32	15 mils	
100	32	12 mils		32	15 mils	

**One wire broke
Shock: 27,000 g perpendicular to wire and parallel to substrate
Wire Diameter: 1.0 mil

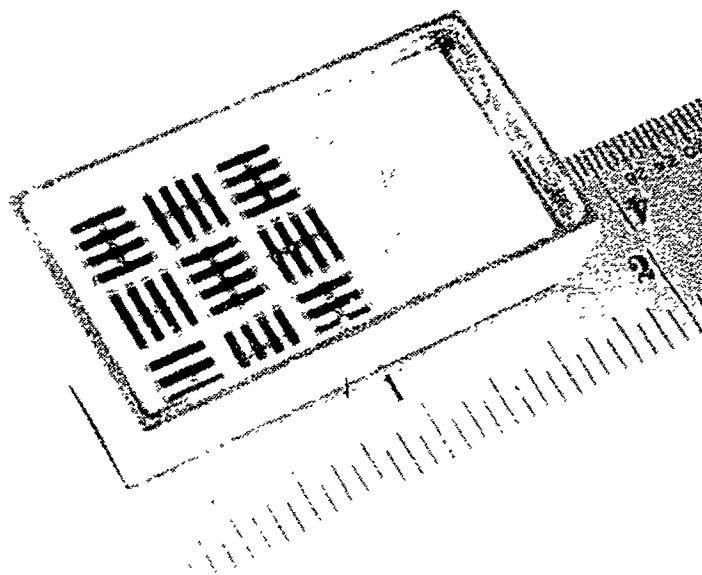


FIGURE 11 THICK FILM RESISTOR EXPERIMENT

DESIGN AND FABRICATION OF A TEMPERATURE-COMPENSATED
VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR

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ABSTRACT

This paper describes the evolution of the electrical and mechanical design of a ± 5 ppm frequency tolerance quartz oscillator for use in remote sensor transmitters. The design is traced from the initial limited temperature range, low shock, voltage-controlled crystal oscillator (VCXO) to the current wide temperature range, gun-hardened temperature-compensated voltage-controlled crystal oscillator (TCVCXO). High density thick-film microcircuit techniques were evolved and applied in construction of the crystal oscillators. Problems met in multilayer printing, abrasion and laser trimming of resistors, bonding of leads and chip elements, and attempted solutions for a low shock (1000 g) TCVCXO module configured in a 1 inch by 1 inch by 0.2 inch* case are discussed.

INTRODUCTION

High accuracy, hybrid microcircuit quartz oscillators for use in sensor systems such as the remotely monitored battlefield sensor system (REMBASS) and the field artillery acoustic locating system (FAALS) have been the subject of recent R&D efforts at the ECOM Electronics Technology and Devices Laboratory. This effort has been directed towards meeting the requirements for a ± 5 ppm frequency tolerance voltage-controlled crystal oscillator (VCXO) to improve sensor systems performance capability by increasing the number of available data channels for a given band.

Advanced remote ground sensors such as the Phase III transmitter or "common module" deployed in Southeast Asia provided, at best, a ± 30 ppm transmit frequency tolerance under operating conditions which included 1000 g (6 ms) shock for air delivered units and a limited operating temperature range of 0°C to +60°C peculiar to that geographical area.¹ A ± 30 ppm frequency tolerance was representative of the state-of-the-art of producible miniature VCXO at that period of time.

*See last page for metric equivalent units.

The initial development effort addressed the feasibility of a ± 5 ppm VCXO for a narrow, 0°C to 60°C , temperature range and air delivery usage.² Then, in anticipation of world-wide deployment needs, the development was focused on a temperature-compensated voltage-controlled crystal oscillator (TCVCXO) capable of -40°C to $+75^{\circ}\text{C}$ temperature operation with the highest shock level (1000 g) still determined by the air drop delivery.³ When finally artillery delivery emerged as a highly desirable mode of sensor deployment, effort was redirected to meet the added requirement imposed by the 15,000 g levels of the high shock environment.

The electrical approach chosen for this oscillator represents a significant departure from the classic VCXO circuit which uses an inductor and often additional tuned circuits to shape the frequency deviation and linearity characteristics. In addition to not readily lending itself to microcircuit construction, the inductor usually possesses undesirable nonrepeatable thermal characteristics and is difficult to adjust. The chosen approach which utilizes functional thick-film resistor trimming to achieve exact required performance provides for a low cost, high yield frequency linearization and temperature compensation method.

Restricted size, tight resistor tolerances, and a circuit topology rich in crossovers created formidable requirements for construction of this high density microcircuit TCVCXO. Techniques used to meet these constraints included multidecked substrates, multilayered conductors, many 25 mil wide thick-film resistors, and 10 to 15 mil conductor widths and spacings. Problems met in multilayer printing, abrasion and laser trimming of resistors and bonding of leads and chip elements, and attempted solutions for a low shock (1000 g) TCVCXO module configured in a 1 inch by 1 inch by 0.2 inch platform case are discussed.

DESIGN EVOLUTION

A Phase III transmitter plug is shown at the top in Figure 1. A cavity, seen in the figure with lettering on its walls, contains the discrete components of the original ± 30 ppm frequency tolerance VCXO operating in the 20 to 22 MHz frequency range. Channel selection was accomplished by crystal replacement, with access at the end plate of the plug. At the lower left is shown a retrofit hybrid microcircuit VCXO assembly which was developed and built at ECOM to demonstrate the feasibility of meeting a ± 5 ppm overall frequency tolerance. Several of the Phase III transmitter plugs, modified using these oscillators, met requirements and successfully passed REMBASS tests in June 1974.

A sample of the extended temperature range (-40°C to $+75^{\circ}\text{C}$) TCVCXO, developed subsequently, is shown on the lower right in Figure 1. Microcircuit construction details concerning two iterations of this design, TCVCXO-I and TCVCXO-II, will be described in a latter section of this paper. This module was destined to be incorporated into a completely

redesigned transmitter plug, still within the overall size constraints of the original Phase III plug. Since the circuit performance of each TCVCXO is optimized for a specific oscillator crystal, channel selection using this unit is required to be performed at a module replacement level. The increased complexity of the device, apparent in the photograph, is due primarily to the additional circuitry required to compensate for the excursions of the crystal frequency as a function of temperature. (The best oscillator stability attainable over a wider temperature range, without compensation, is in the order of ± 15 ppm for air drop environment and about ± 20 ppm for artillery delivery, if production tolerance is to be kept within still reasonable limits.)

A powerful temperature compensation technique, to be described later, which lends itself to ease in manufacture and allows a reasonably large crystal angle tolerance, was employed to meet a ± 2 ppm frequency/temperature stability requirement. An additional ± 3 ppm was permitted for the effects of shock, 6 month aging and other frequency error contributions of lesser importance. The unit has the capability for both digital frequency-shift keying (fsk) and analog modulation. Deviation sensitivity is 500 Hz per volt and deviation linearity is better than 1%. Not optimized for power consumption, the unit consumed 85 mW and required a bipolar 9 V regulated supply voltage. The total drain on two 15 V batteries due to this oscillator is about 180 mW, if the dissipation in the regulators is included. (This has now been reduced to 50 mW and the need for a bipolar supply eliminated.)

Circuit techniques evolved in the development of this early thick-film hybrid TCVCXO, augmented by computer-aided design techniques, and experience gained in shock testing of both the package and microcircuits established the basis for the current design of the gunhardened TCVCXO. An artist's conception of the TCVCXO module is provided in Figure 2. Intended for insertion into a cavity accessed from the side of the terminal delivery vehicle, the molded module has the geometry of a truncated cylinder. Following insertion of the TCVCXO module into its printed circuit connector, the other, smaller, part of the truncated cylinder is wedged between the module and cavity wall to secure the two sections.

Two 0.030 inch by 0.850 inch by 1.525 inch alumina substrates comprising the linearized VCXO section and the compensation sections, respectively, are bonded back-to-back, with the circuitry protected and hermetically sealed by thick-walled metallic lids. The rectangular geometry of a ceramic flatpack crystal unit may be seen in the exposed linearized VCXO section in Figure 2. The ceramic flatpack crystal is one of a family of new microcircuit compatible crystal units currently under development.⁴ The crystal unit is situated such that the axis of rotation of the projectile passes through the center of the crystal and normal to its larger surface, thereby minimizing centrifugal forces under the rotational acceleration of 322,000 rad/sec². Initial air gun tests of mock-up models have indicated the capability of this configuration to survive a 20,000 g, 0.5 ms shock level. This configuration is intended

to be eventually employed for both low and high shock applications.

TCVCXO DESCRIPTION

The functional block diagram of the TCVCXO illustrating the design approach is shown in Figure 3. An antiresonant Pierce crystal oscillator circuit was selected to provide an optimum in stability performance. The oscillator contains a voltage variable capacitance in series with the crystal unit, whereby the output frequency is changed in response to variation in the voltage applied to this capacitance. The relationship between output frequency and applied voltage is normally nonlinear. To permit simultaneous functions of digital fsk or linear analog modulation, frequency compensation and frequency trim, linearization of the VCXO tuning characteristic to better than 5% over a deviation range of 100 ppm is required. This is accomplished by a diode function generator (DFG) design which produces a two-segment voltage transfer characteristic having a nonlinearity approximating the reverse of the oscillator's frequency-voltage tuning characteristic. The number of required segments is related to the degree of linearity required, e.g., the 1% linearity previously specified on an early TCVCXO required six segments.

A more conventional approach to VCXO linearization was considered and found to possess undesirable characteristics. For example, 5% linearity at 100 ppm frequency deviation may be obtained from a 20 MHz VCXO by introducing an inductor in series with the crystal unit, in addition to the varactor. It can be shown, however, that this causes large, unpredictable contributions to the VCXO frequency temperature characteristic. Further, additional tuned circuits are required to be incorporated to suppress possible spurious oscillations.^{5,6} The overall effect is a significantly reduced stability.

The temperature compensation is accomplished by a six-segment DFG which produces both positive and negative slope segments to approximate the required cubic frequency-temperature-compensating function. The compensating DFG is driven by a temperature sensing circuit employing the repeatable temperature characteristics of a silicon diode to sense the package temperature. Crystal units having lower to upper tuning point deviations, ranging from 10 ppm to 30 ppm, may be compensated to within ± 2 ppm with this method. Existing compensation techniques require much tighter control in crystal temperature behavior.

The summing amplifier shown in Figure 3 is a differential operational amplifier which combines six separate voltages for operation within the linearized section of the frequency voltage tuning characteristic. Five of the six inputs are indicated in the figure: (1) the temperature compensation, (2) the digital (fsk) modulation, (3) an analog control, logic 0 or 1, which restores center frequency for analog modulation, (4) the analog modulation, and (5) the frequency adjust for frequency calibration of the TCVCXO. The sixth is a voltage derived from a silicon diode

temperature sensor to cancel the temperature effects of similar diodes in the linearization DFG. The voltage regulator supplies the 9 V regulated bus from input supply voltage, which can vary from 10 to 15 V. The regulator consists of discrete parts and is of a type previously used in a high stability temperature compensated crystal oscillator.⁷ Because of the high efficiency associated with an input/output differential of less than 100 mV, it was selected over IC regulators which typically have an input/output differential of 3 V. Line regulation is better than $\pm 0.05\%$, and temperature stability of the 9 V output is better than ± 10 mV (-40°C to $+75^\circ\text{C}$).

THE DIODE FUNCTION GENERATOR

The general form of the diode function generator used in the TCVCXO for linearization and compensation is shown in the three-dimensional schematic of Figure 4. Four segments of the network are shown which yield a piecewise-linear approximation of the required voltage transfer function. Piecewise-linear approximation techniques are preferred for the generation of a nonlinear function when a high degree of accuracy and good long term stability are important.^{8,9} The voltage transfer characteristics of the linearization DFG has a non-linearity approximating that of the oscillator's frequency/voltage tuning characteristic. It is a monotonically increasing function approximating a near square law characteristic. For the temperature compensation DFG, the required function is a cubic approximating the cubic frequency-temperature characteristic of an AT-cut crystal.

A basic segment is comprised of a four-resistor bridge, two summing resistors, R_A and R_B , (one each for the inverting and noninverting inputs of the operational amplifier) and a diode switch which is in an "ON" condition whenever the input voltage exceeds a threshold voltage described by the sum of the reference voltage V_R and the forward voltage drop of the diode. The imbalance of the bridge, determined by the value of the bridge resistors, establishes the differential voltage ($V_B - V_A$). Resistors R_A , R_B , R_C , and R_F and bridge resistors R , R_X , and R_Y determine the incremental segment gain. The approximation function, for N segments, is obtained by summing the successive voltages resulting from the incremental segment gains. Accuracy in fitting a required curve is improved with use of an increased number of segments. The threshold voltages, or breakpoints, being related to the forward drop of the diode, will vary with temperature. This condition is easily rectified by introducing an equal but opposite variation into the DFG driving voltage derived from a similar diode type.

FUNCTIONAL TRIMMING

Functional trimming has been used advantageously to achieve exact required performance. A total of 10 resistors are functionally trimmed in the current procedures for fabrication of the TCVCXO. Five percent

initial tolerance is currently specified, as opposed to the 1% and 0.1% tolerance of the early design, for each of the 105 resistors in the complete TCVCXO schematic of Figure 5. Of the 10 functionally trimmed resistors, six are trimmed to provide a given dc voltage, two to provide a given ac (audio) voltage and two to provide a given rf output frequency. The latter is accomplished by sequentially trimming the proper segment bridge resistor in the linearization DFG to give a correct frequency at an input voltage corresponding to the threshold voltage of the next segment.

TEMPERATURE PERFORMANCE

A comparison of TCVCXO compensated and uncompensated characteristics is shown in Figure 6. Compensation to approximately ± 1 ppm is indicated, a compensation ratio of 8 to 1 for the particular crystal used and is typical of recent breadboard units compensated. The improved compensation procedure requires prior knowledge of the frequency-temperature characteristic of the particular crystal unit to be used. Based on this characteristic, the proper values of one or two resistors in the temperature-compensation DFG are determined, graphically or by calculation, and adjusted to these values by trimming at room temperature, all other resistors having already been trimmed to standard values. A single temperature run of the completed oscillator, to confirm the attained stability, is required. Indications are that ± 2 ppm stability will be readily obtained in actual production units. Compensation techniques employed prior to this development required one or more temperature runs of the entire oscillator—a major cost factor—for achieving the desired stability.

DESIGN CONSIDERATIONS FOR TCVCXO-I

Design of the two thick-film feasibility models will be discussed next, beginning with TCVCXO-I.

There were some unusual initial considerations. The nature of the application required a small electronic package, about 1 inch by 1 inch by 0.2 inch. This had to contain almost 150 thick-film and chip circuit elements, a cased quartz crystal (0.5 inch long [excluding pins] by 0.4 inch wide by 0.15 inch thick), and a sensistor (0.35 inch long by 0.105 inch diameter).

From trial circuit layouts, it was obvious that the unusually high packing density (for a thick-film hybrid) would require very small resistors. Enough space had to be left between them to permit air-abrasive trimming to $\pm 1\%$ or (for 12 voltage divider elements) $\pm 0.1\%$.

To permit functional trimming with air-abrasive equipment, certain resistors would have to be located in accessible places away from associated circuitry. Because of this and the general circuit topology (including two sets of paralleled Y networks), numerous crossovers of conductors could be expected, complicating the layout and fabrication.

On the other hand, many resistors were in reiterative networks which would tend to facilitate their layout.

CIRCUIT TOPOLOGICAL DESIGN OF TCVCXO-I

Preliminary sizing procedures indicated that, even with resistors so small as to push the state-of-the-art, we could not situate all of the parts onto a single substrate fitting the desired package size.

The decision on how to subdivide the overall circuit into sub-circuits on several substrates was based on preliminary circuit layouts and adherence, as far as possible, to such principles as (1) minimizing the amount of connections between substrates, and (2) facilitating functional trimming and testing.

Three decks of substrates were planned, the decks to be separated by miniature pedestals, about 40 mils long by 40 mils wide by 25 mils thick, epoxied in place. (The triple deck structure of a completed TCVCXO-I is shown in Figure 7.)

The lowest deck would consist of two substrates covering a 1 inch by 1 inch base area. One of these, 1 inch by 0.4 inch, was to support the crystal, sensistor, and basic oscillator circuit. (The thick-film portion is shown as Section 1A in Figure 8.) The second substrate was to contain the linearization segment and associated operational amplifiers (Section 1B).

Stacked over the linearization section would be a second substrate of the same size on which most of the sensistor and temperature-compensation circuitry and associated operational amplifiers would be supported (Section 2 of Figure 8).

Resistors on both larger substrates would be made with three different resistivity pastes, nominally 1, 10, and 100 kilohms per square per mil of thickness. To avoid using more than three pastes, thus complicating fabrication unduly, chip resistors were used for extreme values of 47 ohms and 1 megohm.

Finally, stacked over the upper 1 inch by 0.6 inch substrate was to be the third deck (Section 3 in Figure 8) consisting of a 1 inch by 0.25 inch substrate bearing six resistors which must be separated from the remaining circuitry during temperature-compensation adjustments. (As the remaining circuitry is stepped through five different temperatures, these six outboarded resistors are kept at room temperature and trimmed to provide a desired output frequency.)

Except for these six resistors and the oscillator circuit, most of the TCVCXO (including 95 film resistors) was to be supported, then, on two substrates totaling only 1.2 square inches in area.

THICK-FILM CIRCUIT LAYOUT OF TCVCXO-I

As indicated, the major circuit layout problem was to cram almost 150 circuit elements into an unusually small space for a thick-film hybrid microcircuit, while keeping these elements and package terminations in optimal juxtapositions. "Optimal" refers to satisfaction of such requirements as (1) minimizing thick-film conductor lengths, (2) reducing quantity of crossovers, (3) not exceeding 100 mils for bonding wire lengths, (4) reducing the possibilities for shorting of film and wire conductors, (5) providing enough space for test probes and trimming, and (6) avoiding unwanted electrical coupling.

Such requirements are part of a larger set of guidelines and rules of good practice which designers have evolved to provide reasonable assurance that (1) a circuit can be fabricated with available equipment without excessive rejects, and (2) that the fabricated circuits will perform as expected. To meet the space requirement, some compromises were necessary, which increased the risk of reduced yield.

To permit the required high parts density, a majority of the film resistors had to be designed with 25 mil widths. (The preferred minimum size is 30 mils.) Resistor dimensions were based on trials with test patterns, to take into account effects related to geometry and terminations. Conductor widths and spacing of 15 (and occasionally 10) mils were necessary in most cases. (The preferred minimum value is 20 mils).

CIRCUIT FABRICATION OF TCVCXO-I

Conventional artwork and photofabrication steps were used to convert the layout into stencil screens. Birox 1000 resistor pastes and gold-palladium conductor paste were used to print circuits on 1 inch by 1 inch substrates (Figure 8), which were later cut to size.

An air-abrasive trimmer was used for TCVCXO-I resistor and linearization adjustments. As anticipated (but not always for expected reasons), the small resistor dimensions and spacings caused trimming problems despite extra precautions such as following a particular order of trimming which would least affect resistors already trimmed.

A second problem was contamination of ICs and other mounted parts by abrasive material during functional trimming. This condition was partially alleviated by placement of an auxiliary exhaust tube over the trimmed substrate.

Another problem was caused by generation of static electricity as a result of gas and abrasive material flow through the trimmer head nozzle. Static tended to lower resistance values of some resistors (probably by causing dielectric breakdown of insulating material between conductive particles in the resistive material matrix). Hence, these resistors had to be trimmed more than was normally necessary to attain target values. When such resistors were reheated to stabilize them or as a result of adjacent bonding operations, their values dropped appreciably. Apparently, this resulted from oxidation of the considerable amount of unprotected material exposed by the extra abrasion. To regain target values, the resistors had to be retrimmed, sometimes more than is normally desirable for retaining required power dissipating capability.

Figure 7 shows an almost completed TCVCXO-I in a 44 pin Tekform No. 20269 platform type case. With a Tekform No. 20270 package cover, the overall dimensions are 1.28 inches long by 1.28 inches wide by 0.25 inch high (excluding pins).

DESIGN CONSIDERATIONS FOR TCVCXO-II

The experience obtained with TCVCXO-I resulted in the second feasibility model, a redesign based on modifications in circuitry and adjustment procedure.

It was decided to eliminate as many bonded wire leads as possible to facilitate production and enhance reliability. Reduction from 280 bonded wire connections in TCVCXO-I to 130 in TCVCXO-II was accomplished by (1) using 22 thick-film crossovers, (2) replacing chip resistors with thick-film resistors, (3) moving functionally trimmed resistors closer to related circuitry, and (4) permitting closed resistor loops.

The last two measures mentioned were made possible by the acquisition of a laser trimmer system. Not only can it be used to trim in close quarters, but its resistance bridge can monitor and control trimming of individual resistors in closed loops.

CIRCUIT TOPOLOGICAL DESIGN OF TCVCXO-II

The second feasibility version of the TCVCXO turned out to be a two-decker, employing three substrates, which are shown in Figure 9 before cutting to size.

Substrate 1A, 1 inch by 0.4 inch, contains the oscillator circuitry and space for the sensistor, all on a 0.4 inch by 0.4 inch area at one end. The other end is occupied mainly by the crystal, although it also contains thick-film conductors for connecting some substrate 1B terminals to package terminals.

Substrate 1B holds linearization and operational amplifier circuitry on a 1 inch by 0.6 inch area. Substrate 2, containing temperature compensation and operational amplifier circuits, is the same size.

THICK-FILM CIRCUIT FABRICATION OF TCVCXO-II

A gold conductor paste was used that was compatible with Cermalloy resistor pastes that had been obtained because of reported immunity to static electricity.

In general, we stopped the trimming of each resistor at a value about 0.1% below the target value to allow for drift, which invariably was in a positive direction. Trimming of the 0.1% tolerance resistors was done in two steps. After an initial trim to about 1% to 2% below target value, resistances were allowed to drift for a day or so before final trimming.

For comparison, side and top views of both feasibility models are shown in Figures 10 and 11, respectively. Some of the pedestals separating the decks are visible in Figure 10.

CONCLUSIONS

It has been shown that R&D efforts have provided a 5 ppm TCVCXO design suitable for remote sensor use over an extended temperature range of -40°C to $+75^{\circ}\text{C}$ and a 1000 g shock environment. Significant progress has been made in the design of a gunhardened TCVCXO, and currently, fully operational units are being prepared for confirmatory testing.

The success of the TCVCXO electrical design is largely attributed to the capability of the diode function generator to approximate the required correction functions and of the functional resistor trim method to provide exact performance--both representing a departure from the more conventional methods of frequency linearization and temperature-compensation of crystal oscillators.

When translating the TCVCXO circuit concepts into working models that would meet stringent size requirements it was frequently necessary to design to "minimum" guideline values, resulting in microcircuit layouts with very small, closely spaced elements. Exceptional care was required during fabrication of the thick-film elements to avoid shorting and to produce resistors within desired $\pm 0.1\%$ and $\pm 1.0\%$ tolerances.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the many contributions of Dr. E. Hafner and Mr. P. Thompson of the Frequency Devices Team and Mr. Owen P. Layden, I. Pratt, E. Malecki, and W. Weintraub (retired) of the Hybrid Microcircuits and Assembly Team and the many others who provided their enthusiastic cooperation in direct support of this project.

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METRIC EQUIVALENT UNITS

<u>MILS</u>	<u>mm</u>	<u>INCH</u>	<u>mm</u>
10	0.254	0.03	0.762
15	0.381	0.105	2.667
20	0.508	0.15	3.81
25	0.635	0.2	5.08
30	0.762	0.25	6.35
40	1.016	0.35	8.89
100	2.54	0.4	10.16
		0.5	12.7
		0.6	15.24
		0.85	21.59
		1.0	25.4
		1.28	32.512
		1.525	38.735

<u>TEMPERATURE CONVERSION</u>	
<u>°C</u>	<u>°K</u>
-40	233
0	273
+60	333
+75	348

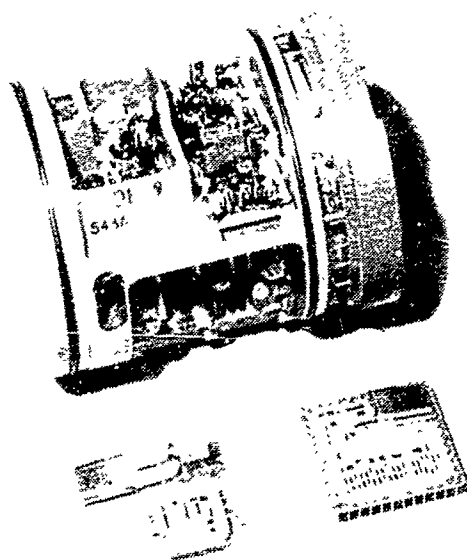


Figure 1. Phase III transmitter plug & high stability VCXO.



REMBASS TCVCXO MODULE

Figure 2. Artist's conception of REMBASS TCVCXO Module.

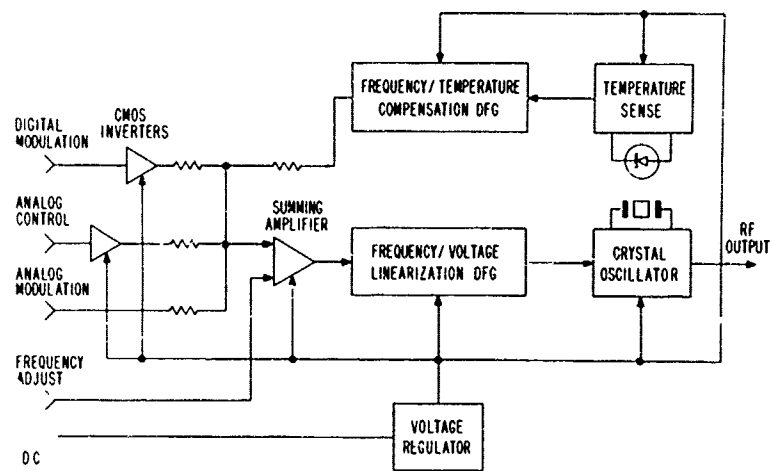


Figure 3. TCVCX0 block diagram.

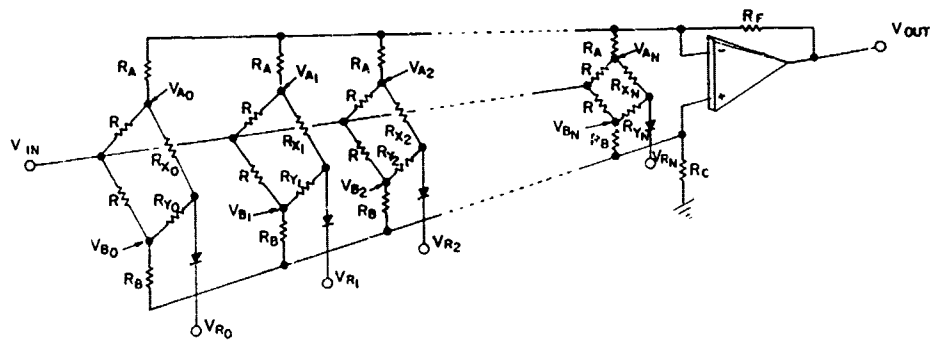


Figure 4. The diode function generator.

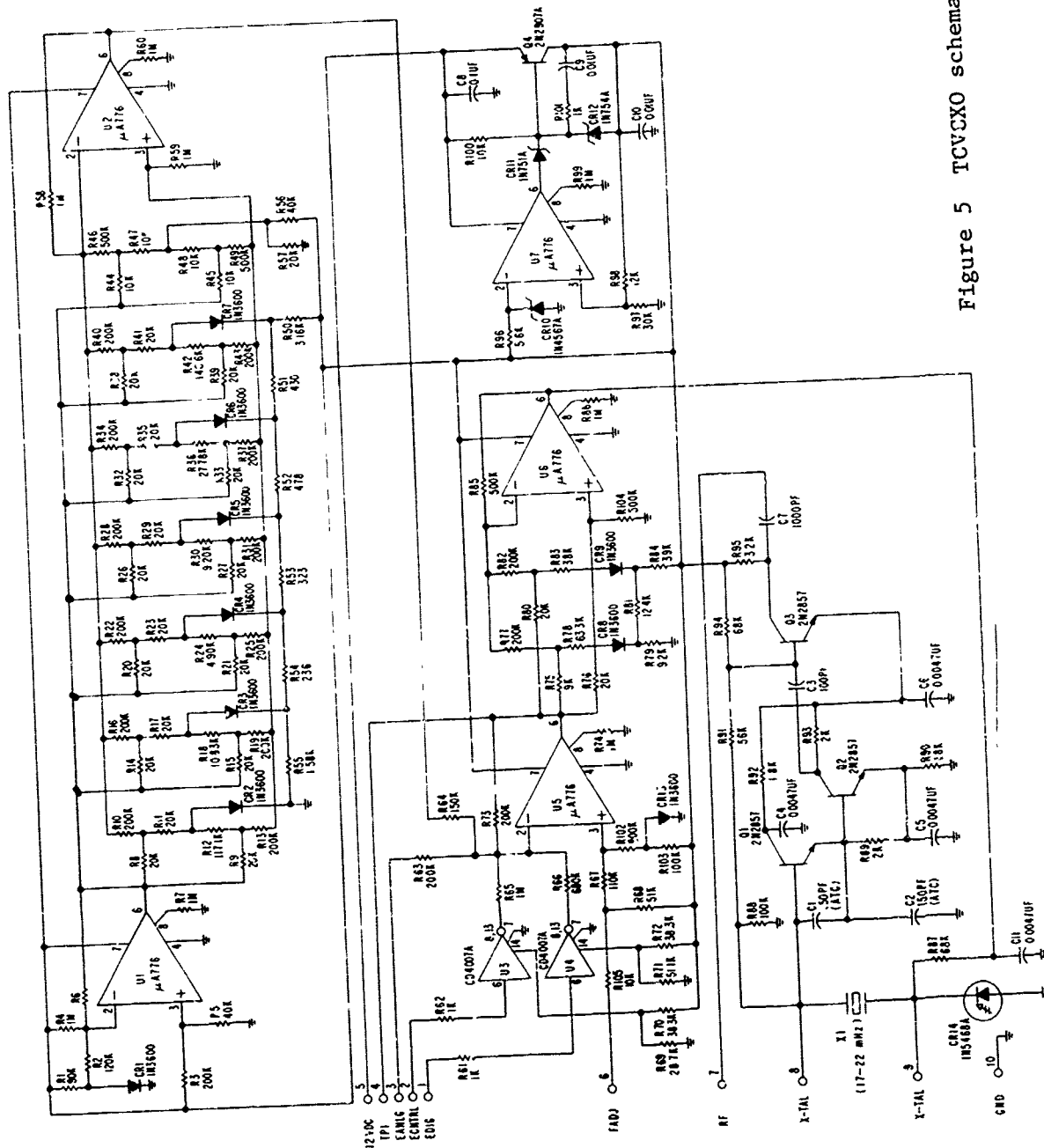


Figure 5 TCVCXO schematic

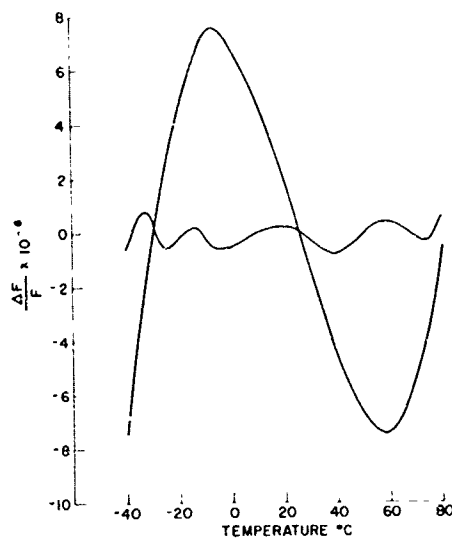


Figure 6. Comparison of compensated and uncompensated TCVCXO characteristics.

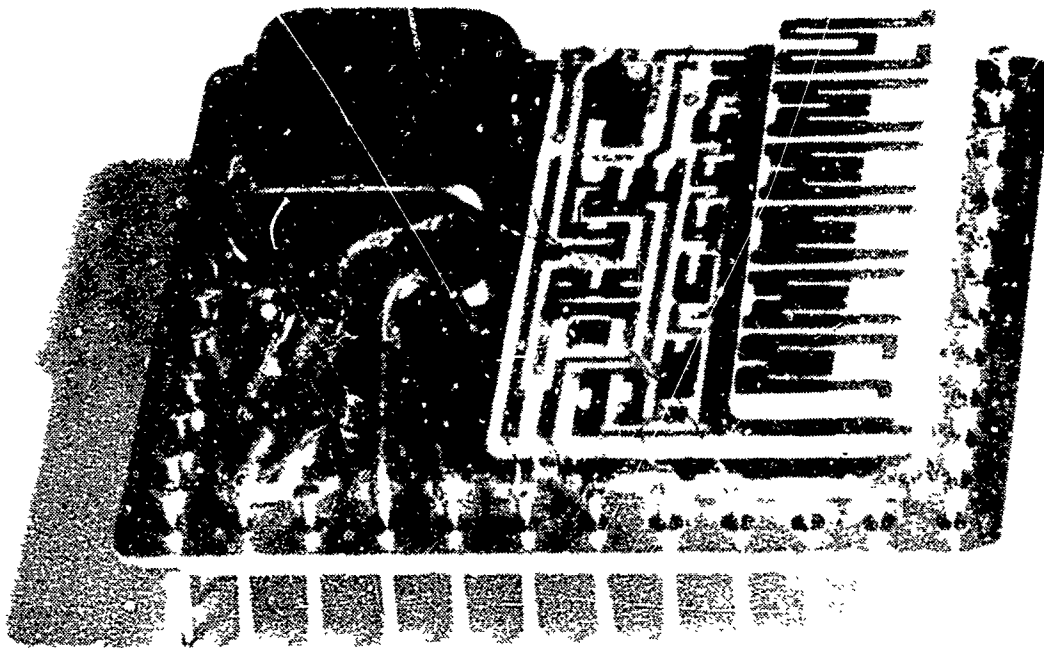


Figure 7. TCVCXO-I.

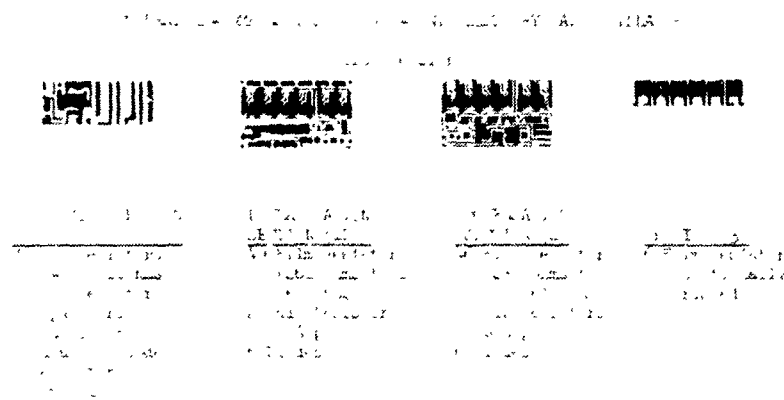


Figure 8. Screen printed substrates for TCVCXO-I.

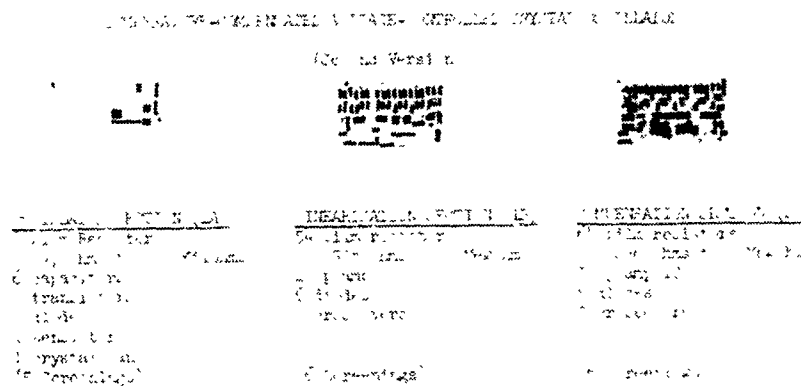


Figure 9. Screen printed substrates for TCVCXO-II.

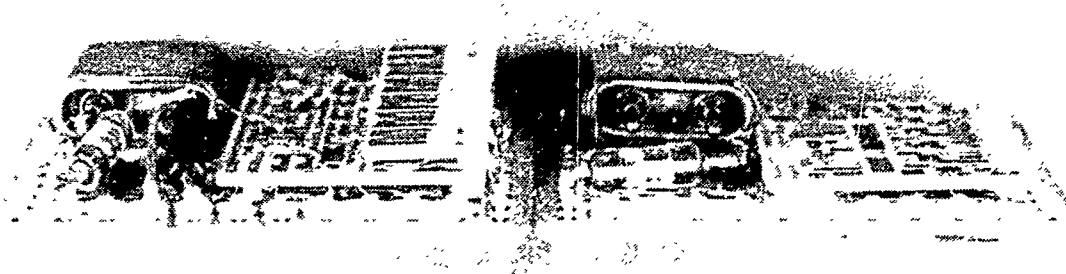


Figure 10. Side views of TCVCXO-I (left) and TCVCXO-II.

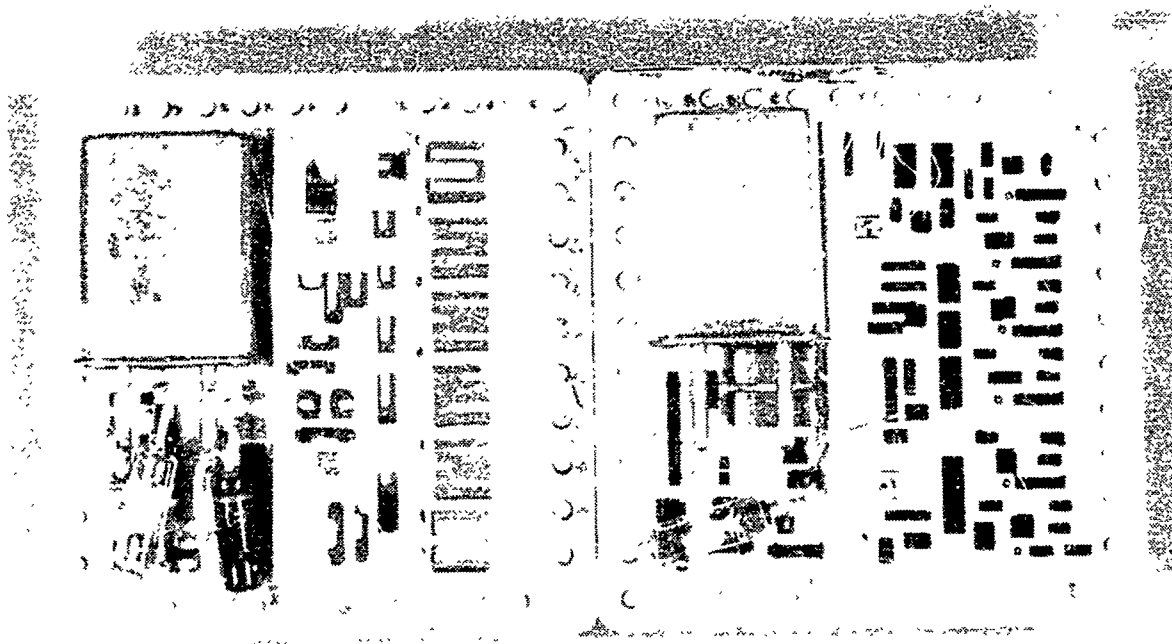


Figure 11. Top views of TCVCXO-I (left) and TCVCXO-II.

SEM/HYBRIDS, PARTNERS FOR LOW COST AVIONICS

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ABSTRACT

The increased complexity of today's electronic systems is frequently reflected in custom designed equipment, expensive to acquire and maintain. Standardization has been partially successful in reducing these costs in ground and shipborne equipments but the weight and volume penalties have been too great to be practical for use in avionics applications. The Department of Defense, through the major military services (Air Force, Army and Navy), are pursuing a coordinated study effort to develop an effective standardization concept for avionics equipments. This paper discusses the use of hybrid microcircuits as a means for minimizing the weight and volume penalties. Also discussed are the potentials of standardization for reducing cost of hybrids through reduced recurring and non-recurring costs.

INTRODUCTION

Advances in electronic concepts and technologies have resulted in the ability to design extremely sophisticated military systems. The military community, in their constant drive to keep ahead, have frequently written system specifications that require the use of these concepts and technologies. The electronic industry has responded to the military needs with a major move to digital design and of course semiconductor technology. The results have been small, lightweight, highly capable but complex custom systems difficult to maintain.

A major approach to semiconductor technology has been through the use of hybrid microcircuits. Results have been extremely successful in reducing weight and volume. Improved reliability is expected but has not yet been proven. High cost of design and manufacture of hybrids has been experienced by most of the industry and acceptance by the designer has been slow. It would appear that major efforts are needed to reduce the cost of hybrid microcircuits if low cost systems are to be achieved.

Standardization has been pursued for a number of years as a means of reducing system cost both from the standpoint of acquiring it as well as maintaining it. Figure I shows the interest generated by various standardization programs during the last 30 years starting in the early 1940s with project Tinkertoy. Progress was slow at first with many technical problems. However, each new program added to the success in lowering system cost where it could be applied. The Micromodule program sponsored by the Army was a major contributor to the development of hybrid microcircuit technology. Its abandonment was due more to its being ahead of its time rather than its

not being feasible. The Navy followed with their Standard Hardware Program (SHP) in the mid 1960's. This program extended the concept of standardization to both the circuit function and the physical format. Results have been extremely successful and many shipborne electronic systems now use many SHP modules. The latest program of interest is the standard electronic module (SEM). This effort is being pursued by DOD through the major military services (Air Force, Army and Navy).

Also shown in Figure I is the interest in Hybrid Microcircuits. Interest started back in the 1950's with hybrids using discrete chip components. Interest increased in the 1960's and early 1970's with hybrids using integrated circuit chip devices. As the circuits became more complex, cost rose rapidly and interest dropped off. Steps must be taken to reduce these costs if interest in hybrid microcircuits is to be revived.

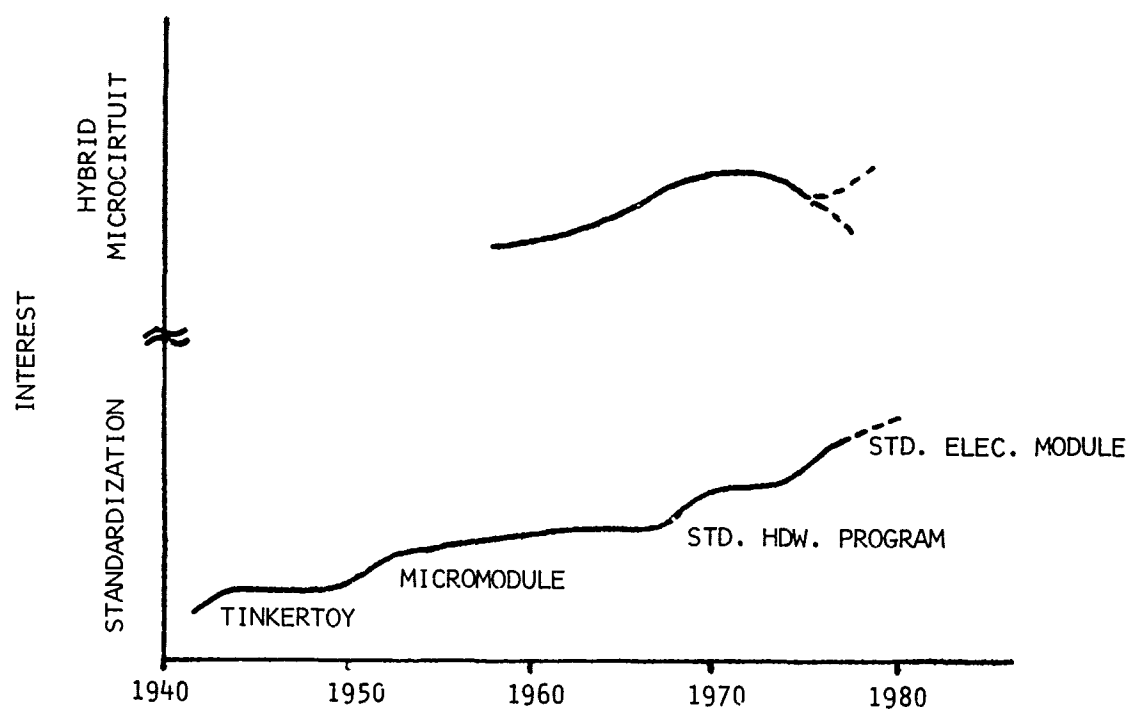


Figure I Interest in Standardization/Hybrids

REDUCING COST

With the apparent success of standardization in lowering cost, it is proposed that standardization be imposed in the design of hybrids as a major means in reducing their cost. Other promising areas should be considered. The program of study should include:

- o Reduce Labor through Simplicity
- o Increase Standardization
- o Increase Reliability
- o Improve Technology

An example of reducing labor on hybrids through simplicity is shown in Figure II. Cost of material and each operation is compared for both design approaches. The original chip and wire design was replaced with Leadless Inverted Devices (LIDs) and thick film resistors. Over 300 wire bonds were eliminated and cost of the simplified hybrid was half of the original design. Figure III shows the LID version. The numbered components are the integrated circuits mounted in ceramic carriers, one of which is shown in the lower left corner. Component attachment is achieved with a low cost solder reflow operation.

Standardization has proven to be an effective way to reduce cost. The original motivation was to reduce maintenance cost but additional savings have been achieved in lowering the acquisition cost through the use of large scale production techniques. Experience has shown that standardization can reduce life cycle cost of electronic equipment from 25% to 50% of the cost of the custom design. Figure IV shows how standardization affects both cost and volume of various packaging technologies. In all cases cost is lower with standardization but volume is greater. It should be noted that the use of standard hybrids will result in cost equivalent to the lowest custom cost with a minimum volume penalty.

Reliability is an added benefit of standardization. Experience on the SHP program has resulted in better than an order of magnitude improvement in reliability over the equivalent custom design. Standard hardware can be rigidly specified and rigidly controlled in its manufacturing cycle at minimum cost. Figure V shows how reliability effects cost. If a custom design has a MTBF of 1, we can expect the standard design to be at least 10. The life cycle cost (the sum of the acquisition cost and the logistic support cost) is shown for both the custom and the standard designs. It is easy to see that the cost of the custom design for an MTBF of 10 would be unreasonably high. The life cycle cost of the standard design with an MTBF of 10 is actually less than the cost of the custom design with an MTBF of only 1.

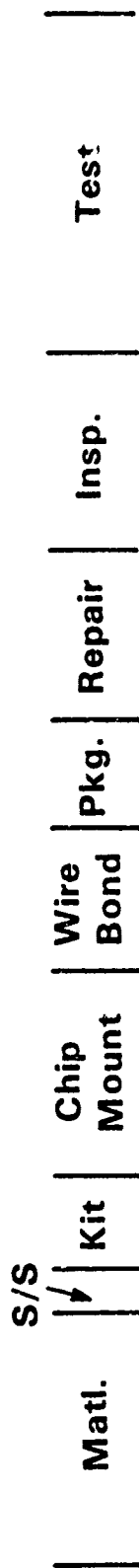
Improving technology is another way to lower cost. Major efforts are now underway by both the military and industry to develop these improvements. Some of the more significant programs of study would include:

Reduced Cost with Simplicity

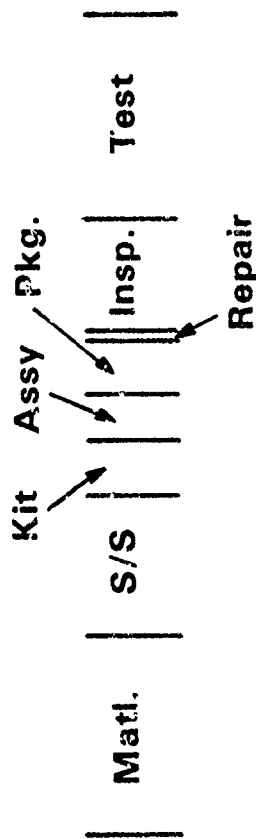
Figure II

Reduced Cost with Simplicity

Chip & Wire



LIDs with Screened Resistors



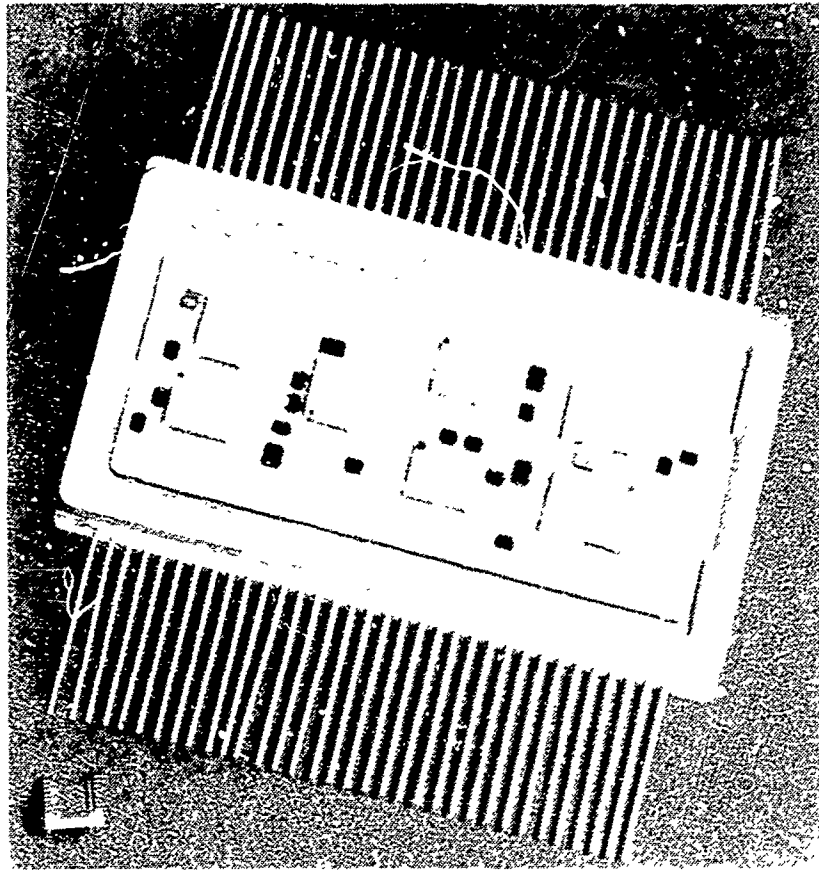


Figure III Hybrid with LIDs

- o Film Carriers
- o Beam Leads/Flip Chips
- o Epoxy Sealing
- o Organic Coatings
- o Encapsulation

Many of these programs have been discussed in detail at this symposium. Figure VI shows an estimate in cost improvement over the standard chip and wire hybrid. Note also that the expected improvement with standardization can be expected with all technologies.

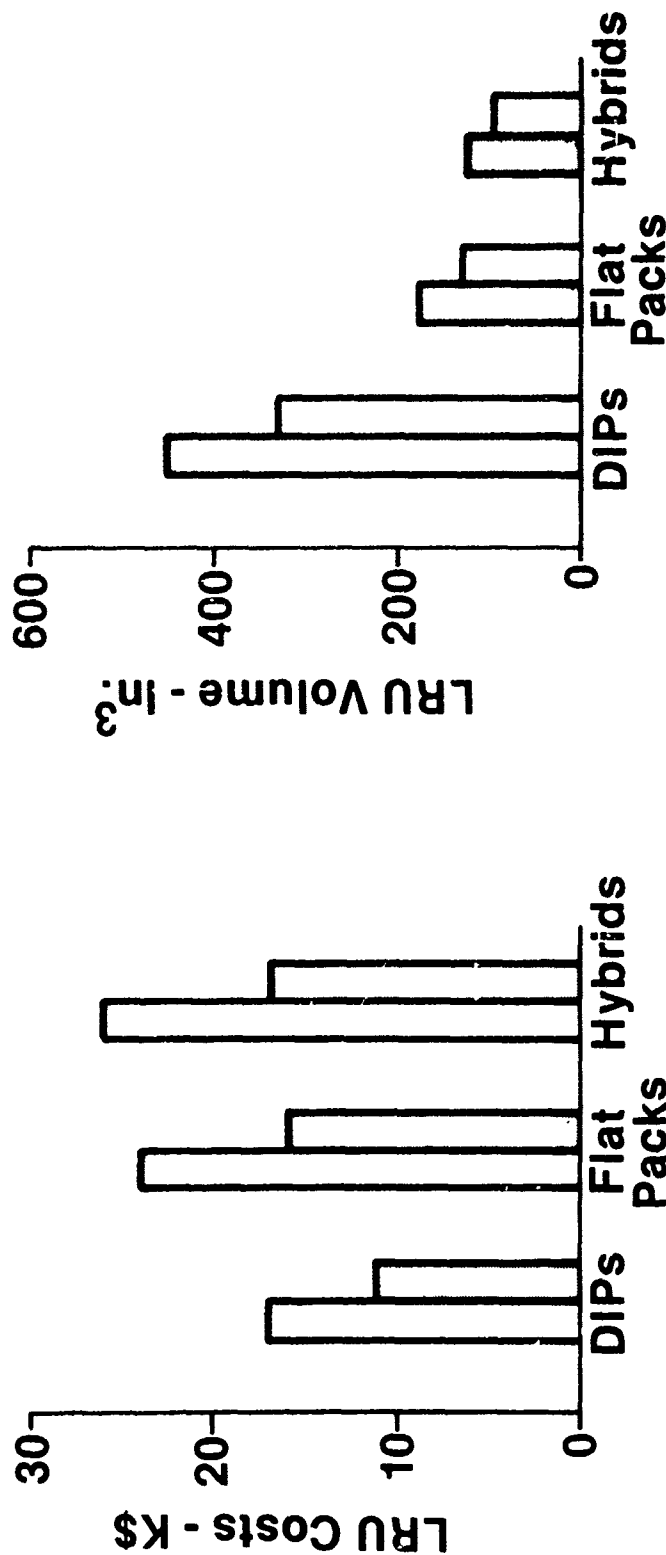
STANDARDIZATION CONCEPT

Assuming that standardization will show a cost benefit, what should the standardization concept be? DOD has established a Tri Services

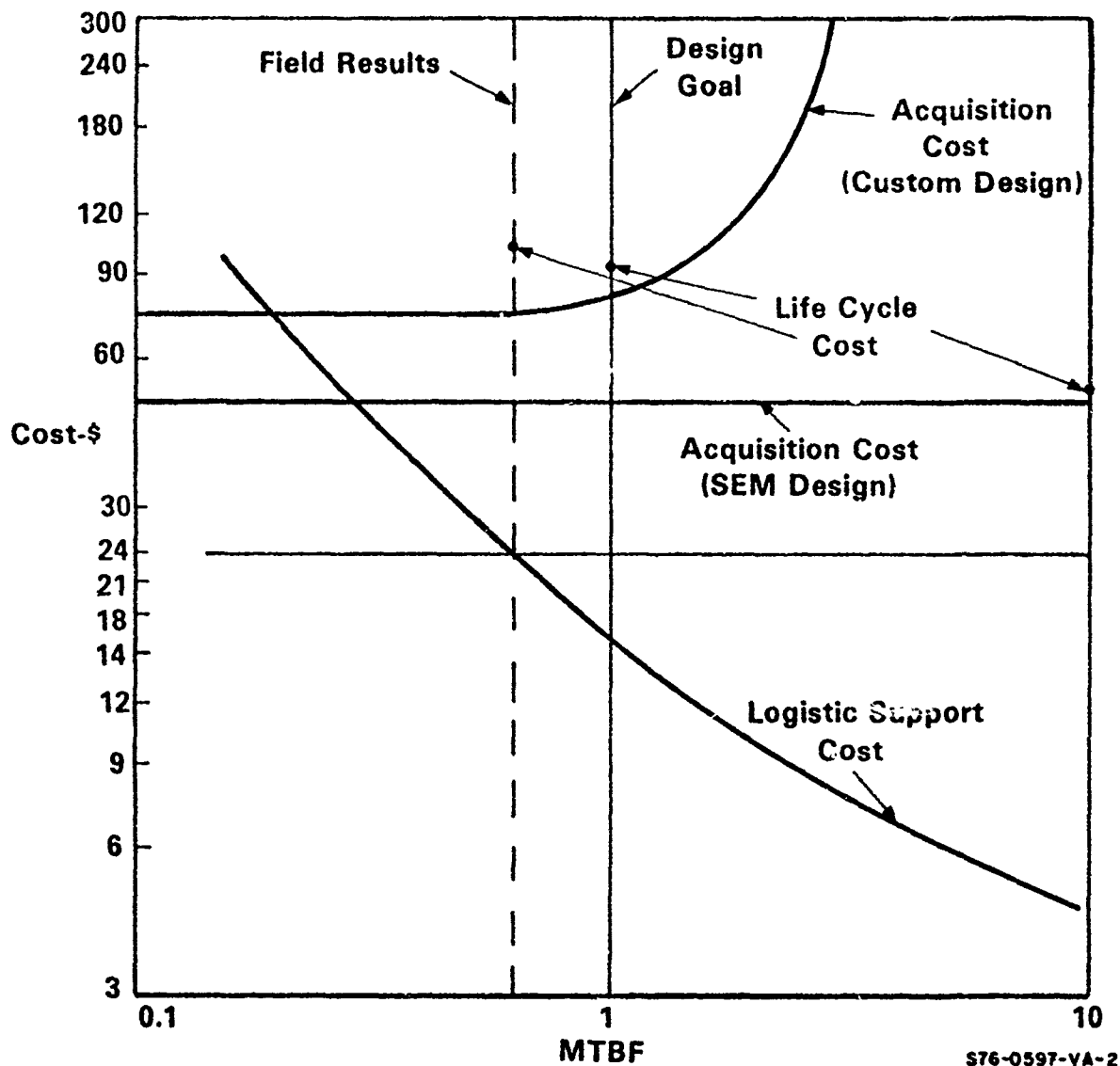
Figure IV

Effects of Standardization on Cost and Volume of Digital LRU

Custom Design
 Standard Design



Reliability vs Cost (Custom/SEM Designs)



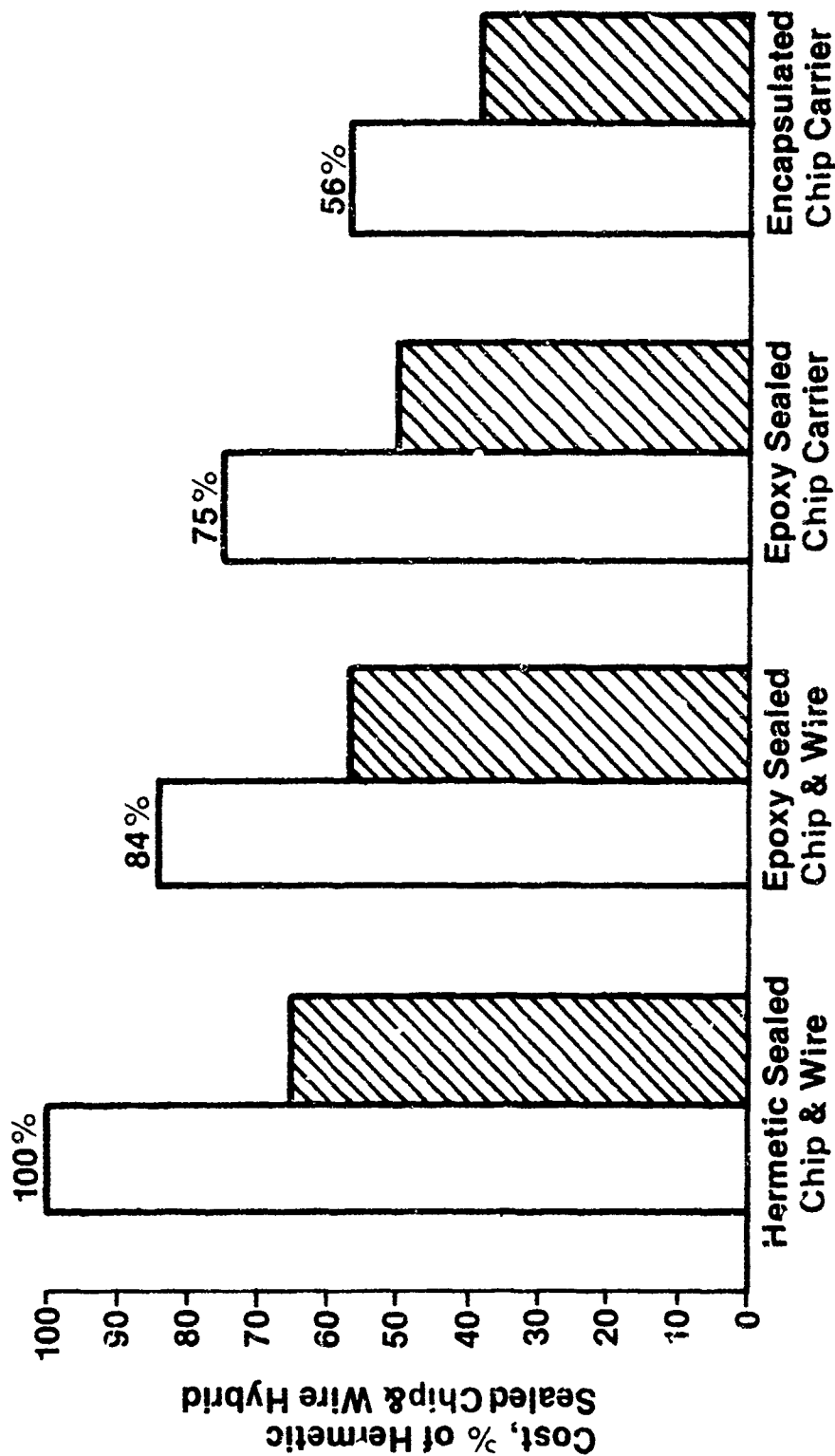
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Figure V

Figure VI

Potential Cost Improvement With Technology

and Standardization



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Committee of the Air Force, Army and Navy to study this problem. Their objective is the development and enforcement of commonality and standardization to reduce maintenance requirements and to improve MTBF, LCC and availability of replacement part. This committee meets periodically to review and coordinate their efforts. To date it has generally been agreed that the current Navy SHP module would be recommended for ground type equipment. It is further agreed that additional effort will be needed to determine a concept for applications where weight and volume are critical requirements.

The proposed concept presented in this paper is currently being evaluated by the Air Force as the standardization candidate for avionics applications. The concept extends to the subsystem chassis level. The Air Transport Racking (ATR) configurations are recommended for the basic chassis. The commercial airlines have a long history of successful use of ATR. Studies have shown minimum penalty with their use in military applications.

Using ATR as the basis for standard sizes it is now possible to establish the corresponding standard printed wiring card sizes shown in Table I.

TABLE I ATR-Maximum Board Sizes

	Width	Height
Full ATR	9.0"	6.2"
3/4 ATR	6.2"	6.2"
1/2 ATR	3.6"	6.2"
1 1/2 ATR	14.2"	6.2"

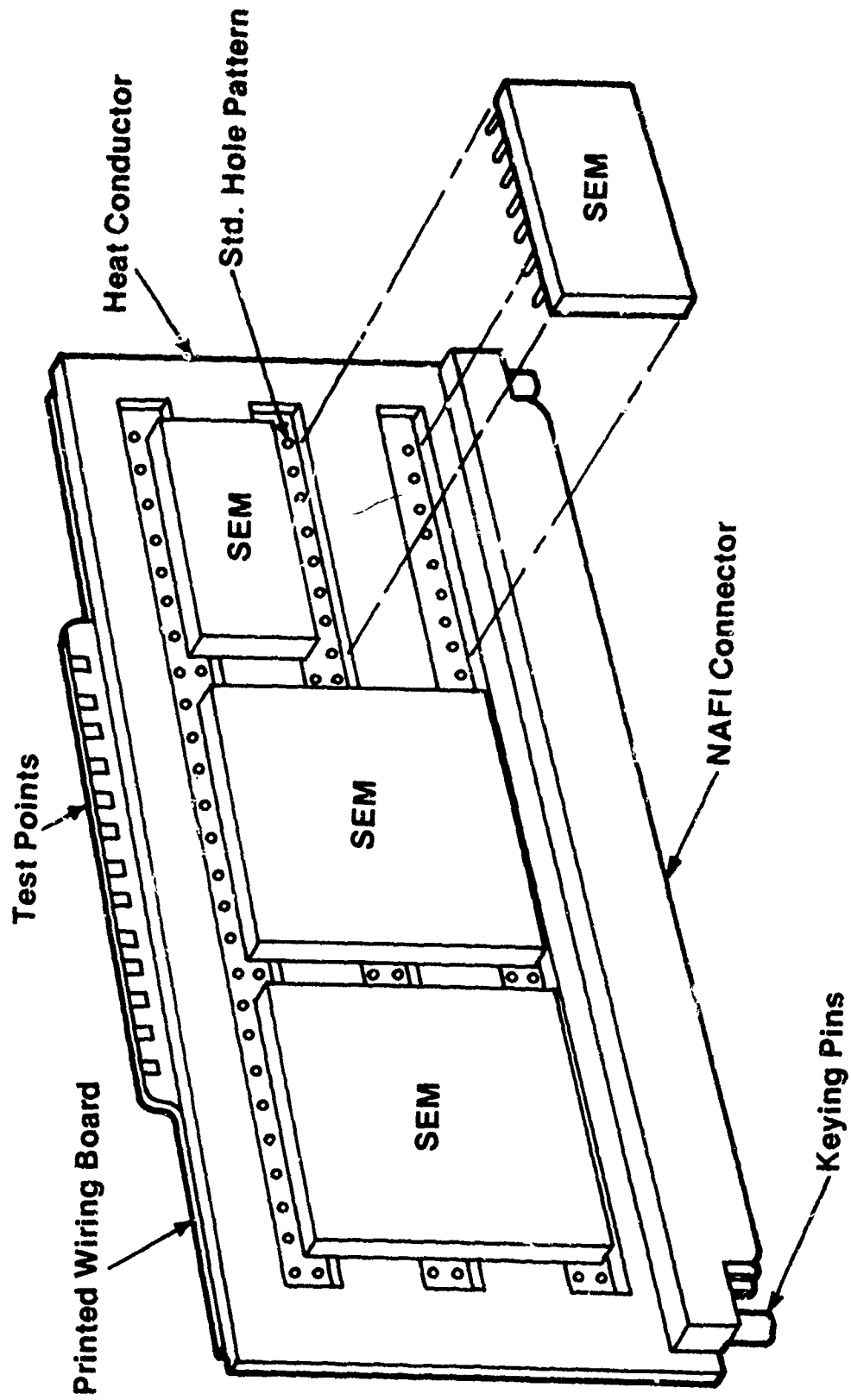
It was originally thought that these boards would be the standard modules (SEMs) but studies show very little commonality of functions at this level of partitioning. It therefore will require circuitry breakdown to a lower level.

Figure VII shows the concept of smaller SEMs mounted on the printed wiring board. The standard hole pattern of the board has been established based on the dual-in-line (DIP) pin configuration. All SEM pin configurations match this standard pattern. A family of SEM sizes has been established based on several partitioning studies of digital signal processors. These sizes in hybrid form are shown in Figure VIII. Although it is not necessary that the SEMs be in hybrid form, it is recommended that they be for avionics applications. Note that the heat is conducted through a metal plate as an overlay on the printed wiring board. The clearance slots of the overlay can be a standard pattern to match the board hole pattern.

A weight and volume study was made on a beam controller (digital). Table II shows the results of three custom and two standard concepts.

Avionics "SEM"

Figure VIJ



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Figure VIII

SEM - Hybrid Configuration

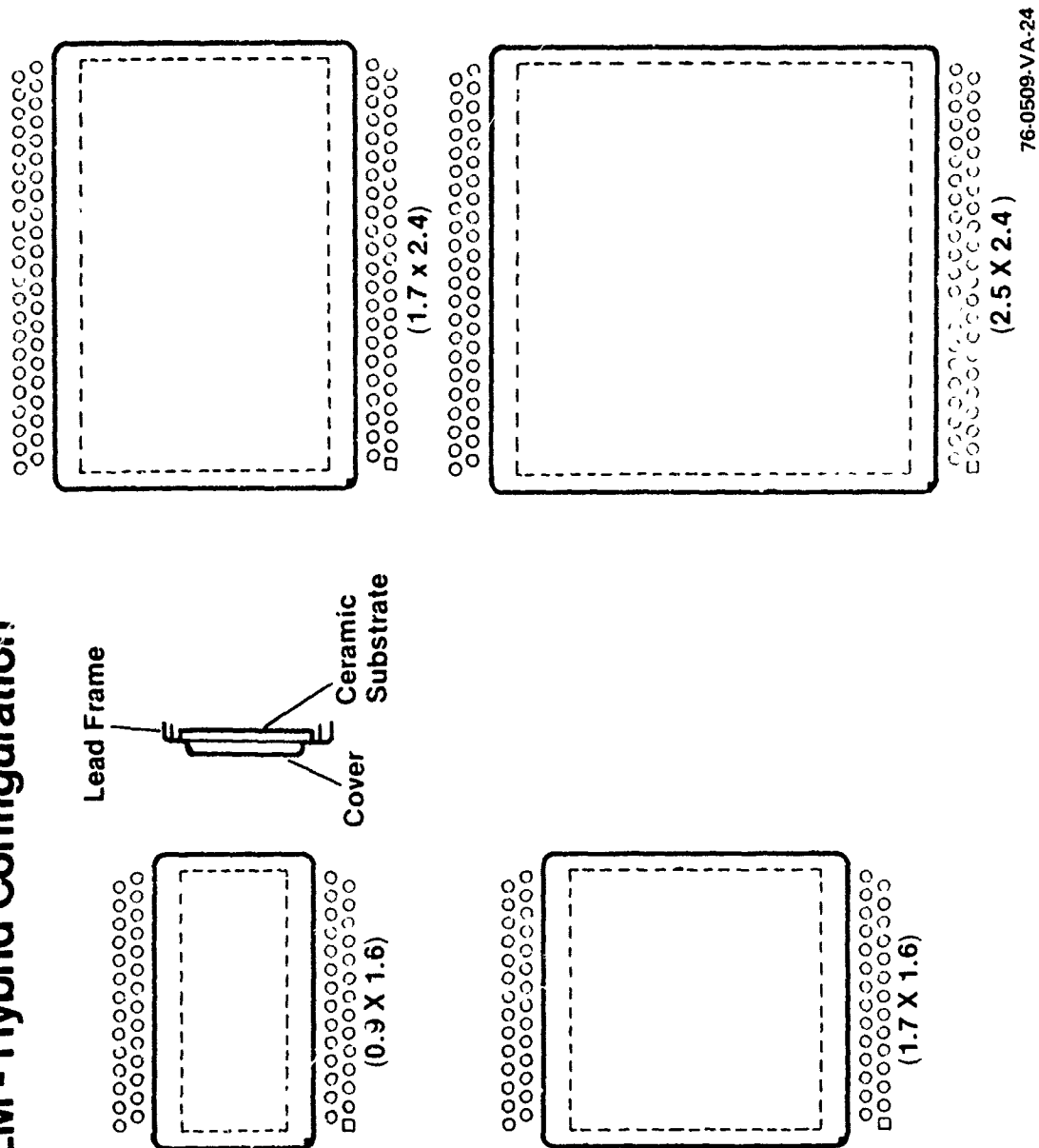


TABLE II Weight and Volume (Custom vs Standardization)

	Volume	Weight
DIPs (Custom)	330 in ³	14.4#
Flat Packs (Custom)	132	4.8
Hybrids (Custom)	98	3.9
SHP/DIPs	450	19.7
SEM/Hybrid	123	4.9

It is apparent that the SHP modules in their present format of DIP devices would be too great of a weight and volume penalty for avionic applications. In contrast however the proposed SEM concept using hybrid technology would be quite acceptable in most applications.

Since we have an acceptable standardization concept at a lower cost the question is to what extent can standard functional circuits be utilized. Several studies are currently underway to repartition existing custom design systems for the proposed SEM concept. The data looks promising as shown in Figure IX. The results show that the SEM approach only requires about 25% more devices than the custom design. Of the SEMs about 80% appear to be functional standard circuits with a potential for multiple use in other applications.

Work is continuing to more completely finalize the SEM concept. Additional efforts will be needed to develop the SEM family of standard circuits. Other studies that must be performed include establishing documentation, specification, and quality procedures. This latter effort can be simplified with help from the current SHP procedures which have already been proven.

Studies have shown that logistic support cost of custom design systems frequently represented 50% or greater of the life cycle cost in avionics applications. Recent studies of systems designed with the proposed SEM concept show that this has dropped to the 10% to 15% level. Since the acquisition cost is now the greater part of the life cycle cost, we should be concentrating more of our efforts on improving manufacturing. The potential of large production requirements for standard circuits now make lower cost possible through the use of mass production techniques, something never possible before with hybrid microcircuits.

REPARTITIONING FOR SEMS
(DIGITAL SIGNAL PROCESSOR)

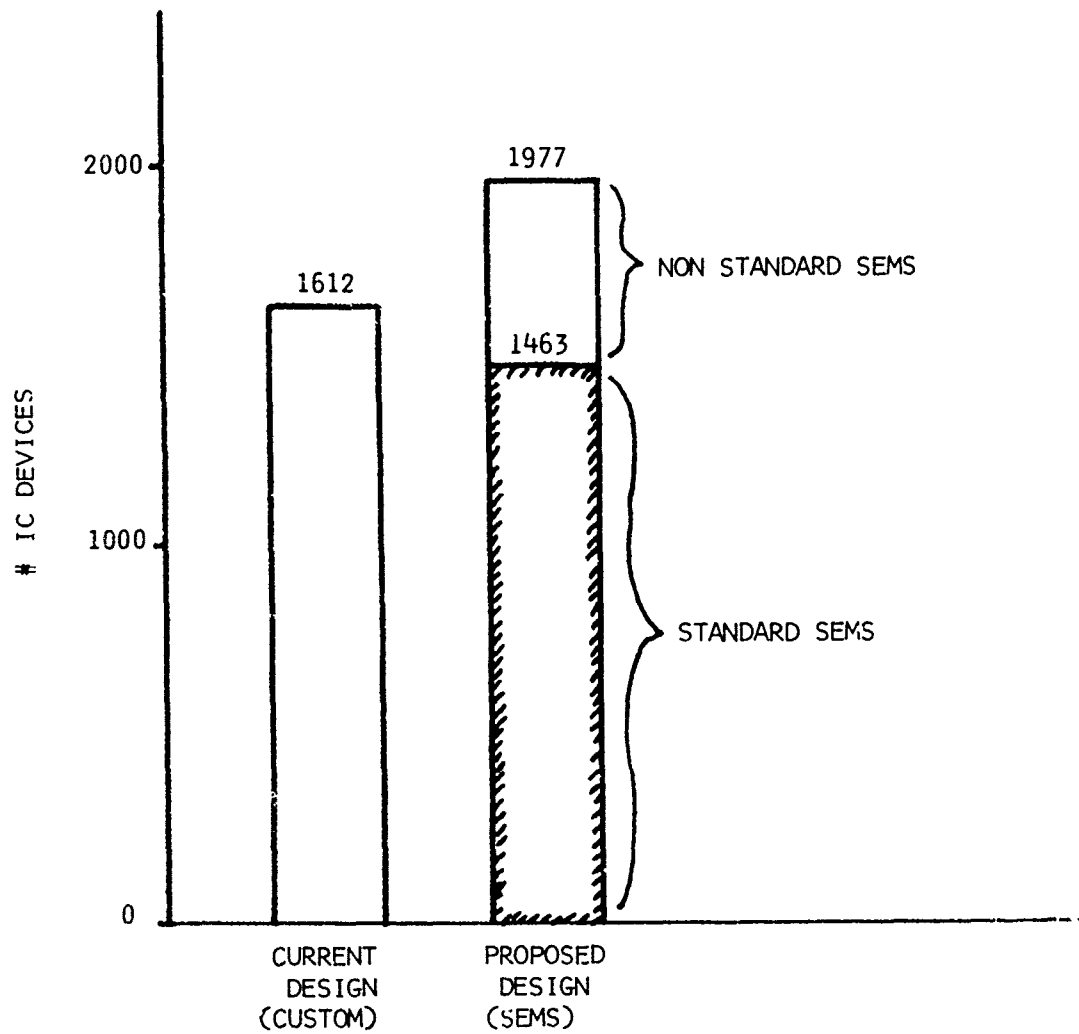


Figure IX

SEM MODULES

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INTRODUCTION

Hybrid microcircuit technology provides methods to further the objectives of the Standard Hardware Program as introduced by the Navy. At this point in time, we can study what has already been achieved and thereby develop a foundation from which future achievements can be anticipated.

As a prelude, a review of the hybrid microcircuit state of the art is advisable because there are numerous processes and procedures which are currently practiced.

A discussion regarding cost effectiveness to achieve electronic functions in the Standard Hardware Program is also very germane and will influence how widely acceptable this program will eventually become.

HYBRID CIRCUIT STATE OF THE ARTS

Hybrid microcircuit electronics which started out as a technology to provide miniaturization in those relatively small number of applications where monolithic devices were not available or were not economically feasible, has matured into a fully developed industry. During the last several years, the industry has perfected a variety of machines to perform the necessary manufacturing steps.

We now have printing, drying and firing equipment to handle ceramic substrates and/or snap-strates up to 2" x 2" or larger. We have resistor trimming equipment with automatic unloading, with servo controlled nozzles, with direct read-out capability. We have available laser trimming systems which when working in conjunction with specifically dedicated control systems can measure and adjust the values of a variety of resistors effectively and efficiently.

In the semiconductor dice area, in addition to automatic probing of wafers, we now have equipment to do precision wafer cutting using a fine blade where the devices are pre-attached to a mylar film. We have machines that can pick and place directly from the mylar film to glass dice holders.

Eutectic die bonding equipment is available which provides local hot gas heating for each specific die bond, eliminating the need to maintain the entire substrate at the eutectic temperature. Methods have been per-

fectured to attach ceramic chip capacitors to the substrate and to attach the substrate into the package using noble metals which are free from contamination and which provide lasting stability.

The combination of Polaroid film and X-ray equipment provide a means to assure that chip attachment and substrate attachment have been achieved with acceptable contact area.

Complex monolithic integrated circuit chips are attached to the substrate using gold-filled epoxy. The epoxy attachment provides mechanical and thermal properties which have been established as acceptable. Eliminating the need to conduct current through the epoxy contact avoids the possibility of aging problems due to the change of resistivity of the epoxy.

Bonding equipment has now been developed which allows one to use gold or aluminum wire and to use thermo compression or ultrasonic bonding. The machines provide flexibility as regards to different heights of chips, excellent control of ball size and automatic tail pulling. Also available is non-destructive inline bond pull equipment which can be used for continuous sampling of work done on each bonder.

Package sealing can now be accomplished either by the use of gold-tin preforms in a nitrogen filled belt furnace or by solid state seam welding which is done in a drybox. The microcircuits can be dried and outgassed in a vacuum oven, transferred directly into a drybox which is back-filled with nitrogen. The drybox is equipped with both moisture and oxygen monitoring equipment to guarantee the cleanliness of the internal package.

In addition to the conventional helium leak detector and Krypton gas leak detector equipments, one can now perform a spectrographic gas analysis on a sample from each sealing lot.

Electrical test equipment has been developed by Hewlett Packard and other companies that provide a means to program a series of tests, read and record hard copy a sequence of parameters, and place these parameters into the machine's memory. One can then subject the parts to a sequence of operating burn-ins, reading and recording the parameters automatically after each step in the sequence. This procedure assures that the parts shipped are from production lots which exhibit no signs of deterioration.

Automatic testing also allows effective inspection of circuits which have one or more complex monolithic devices.

A second significant result of this maturing technology has been the growing availability of more highly developed materials. In the area of conductors, resistors, and dielectric paste materials we see a proliferation of new companies. These companies are making available materials which are more stable with time, more predictable as to their characteristics and easier to store and use. In addition, the materials have been developed for use by application; i.e., lower cost for commercial use and higher cost for Military use.

A third significant development has been the MIL-STD-38510 and MIL-STD-883, MIL-STD-28787 sections specifically directed at the hybrid microelectronic industries. We now have a base line of methods and criteria on which to develop standardization which is necessary for an orderly development of the industry.

SEM MODULE COST EFFECTIVENESS

It is the author's opinion that the proper combination of the Standard Hardware Program format coupled with hybrid and monolithic techniques can provide a universal and cost effective procedure to accomplish complex electronic system functions. The SEM connector format, its standard pin arrangement, mounting and heat conductor, and guide pin concept, when combined with the versatility inherent in the hybrid electronic technique results in a very high performance module. The SEM module allows us to attach a 1" x 2" ceramic substrate to each side of the heat sink fin. This ceramic substrate can be printed to have any number of multi-layers which achieve the needed complex interconnections. In attaching the ceramic substrate it can have printed resistor patterns of up to hundreds of resistors on each side which can be pretrimmed to value or actively trimmed. In addition, this substrate will follow with traditional soldering techniques, attachment of ceramic capacitors, tantalum capacitors, multi-lead ceramic chip carriers and hybrid circuit flat packs. What I am pointing out is that this 1" x 2" ceramic is now effectively the same as a miniature multi-layer printed circuit board on to which we can readily attach a variety of components and hybrid microcircuits. However, the ceramic substrate can also accomodate a large number of printed resistors. In addition, the ceramic substrate does not require plated through holes and does provide excellent thermal heat transfer to the heat fin.

Another important quality and reliability advantage results from the ability to hermetically seal this entire assembly after it has been completely tested, burned-in. There is no need for conformal coatings or other plastic type protection. The assembly can be thoroughly cleaned, dried, hermetically sealed with an inert gas atmosphere.

There are several other inherent advantages. The hybrid circuits used can be manufactured in flat packs which are not excessively complex and thereby provide high yield and low unit cost. The flat packs are easily pre-tested and pre-screened for latent defects. Any flat pack which for some reason is found to be defective after assembly can be replaced without compromise to reliability.

The flat pack metal case containing the active circuits can be grounded or left floating whichever proves most desirable in reducing noise pick-up.

The 1" x 2" substrate can have a metal grid printed on its reverse side which will be connected to a ground. This grid in combination with the metal cover used to seal the assembly provides a total grounding shield for each substrate on either side of the frame. The substrate ground can either be attached or insulated from the frame ground. Another major consideration is the ability to actively trim and adjust the control resistor networks after

all of the active components have been assembled. This can be done in a straight forward effective manner and in many cases, can eliminate the need for tight tolerance resistors and capacitors.

Circuit Technology Incorporated has utilized all of the above techniques in the manufacture of a number of standard key codes, primarily in the area of active filters. These standard key code modules are being used in the Fleet and have gone through several years of qualification at the Crane test facility. The information presented in this paper is based upon this factual experience.

CONCLUSION

There seems little doubt that the inherent advantages of the standardization program when combined with the versatility of hybrid microcircuits provide a powerful technique for high performance, cost effective electronic modules. There is much more that can be done, particularly in the area of higher power applications and in the area of repairable modules.

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ABSTRACT

Tactical portable radio systems under development at ITT Aerospace/Optical Division (ITT-A/OD) for military customers employ hybrid microelectronics and large scale integration (LSI) to achieve equipment with lower cost, greater reliability, smaller size, less weight, and minimum power consumption. This paper describes the microelectronic techniques developed and the studies which verified performance of these techniques for advanced military radio equipment.

INTRODUCTION

ITT-Aerospace/Optical Division (ITT-A/OD) at Fort Wayne, Indiana is a major supplier of VHF/UHF radio sets to the military. Currently under development is a family of advanced portable transceivers for multi-purpose military applications.

In the early 1970's, programs were initiated to develop componentry and packaging techniques of radio systems which would achieve the performance, size, reliability and maintainability requirements of the 1980's. After a study of the possible use of hybrid thin film, hybrid thick film and monolithic fabrication techniques, it was concluded that these requirements were best met by the hybrid thick film fabrication technique incorporated with LSI type devices. Engineering objectives based on military customer needs were to verify the size and weight advantages of the hybrid thick film technology in tactical communication radio equipment design and to determine cost and reliability of using thick film technology in these radio systems.

A thick film material selection study was performed to improve product reliability (per MIL-STD-883 and MIL-M-38510) and producibility. LSI was incorporated in the advanced designs to achieve ultra-high reliability, extremely small size, and state-of-the-art performance.

MILITARY RADIO DESIGN

ITT-A/OD has worked with the United States Air Force and the FAA to develop a family of air traffic control radios which are highly reliable, easily maintainable, capable of multiple operation in close proximity and close frequency spacing, and which take advantages of all recent advances in technology applicable to this usage.

These radios designated the Joint Service UHF Modernization Program (JUMP), shown in Figure 1, were designed for world-wide deployment by the USAF, Army, Navy, and FAA in air traffic control service. They operate on any one of 3500 channels between 225 and 399.95 MHz. They are completely solid-state and contain modular construction permitting simple conversion to a multiplicity of bandwidths for 25 KHz channel spacing or wide bandwidth data handling. Figure 2 illustrates the extent of modularization and the ease of replacement of the modules in the radio equipment.

ADVANCED MILITARY TACTICAL AND NON-TACTICAL PORTABLE RADIO SYSTEM

To meet forecasted military radio operational requirements, ITT-A/OD is currently developing the technology required for a range of advanced portable transceivers which can provide multi-platform operations for all the military services.

SYSTEM CONSIDERATIONS AND REQUIREMENTS

Prime goals of portable military radios are size reduction and increased functional capabilities, within the bounds of cost-of-ownership figures which are budgetable and achievable.

Ease of maintainability, along with sound human engineering concept, must be incorporated in the construction of military radio equipment. These concepts, along with appropriate environmental considerations, must be considered all through the design and development stages.

In addition to the above considerations, the advanced military radio system must provide for:

- 1) A cost effective design,
- 2) A flexible package design that accommodates frequency band, operating mode, and platform changes,
- 3) Secure voice/data capability,
- 4) Low acquisition and life cycle cost, and
- 5) Reliability and availability improvement.

The system requirements for the advanced portable radios to be used as development goals are shown in Table 1.

TABLE 1. ADVANCED PORTABLE RADIO OPERATIONAL OBJECTIVES

Frequency Bands	30 to 80 MHz, 136 to 174 MHz, 406 to 430 MHz
Power Output	1 to 5W
Sensitivity	≤ 0.5 Microvolt
CONSEC	16 Kbits Interface
ECCM	Anti-Jamming Required
Channels	Up to Approximately 2400 Channels
Control	Local and Remote
Preset	4 to 6 Channels

Platform	Manpack/Vehicular/Airborne
MTBF	>3000 Hours
Environment	-50°F to +155°F
Size	200 to 300 IN ³

From the above described system considerations and requirements, it is evident that thick film micropackaging technology is necessary to achieve the ultra-high reliability and extremely small sizes now required without cost increases. This technique allows MSI/LSI chips of all types to be interconnected and "married" with thick film resistors and unencapsulated capacitors in a miniature assembly.

HYBRID MICROELECTRONICS PROJECTS

RADIO TECHNOLOGY PROGRAM

ITT-A/OD has been committed since 1970 to a long term research and development program which effectively utilizes advanced hybrid thick film techniques. The transceiver functional block diagram in Figure 3 (shaded blocks) shows modules selected for the radio technology development program. A photograph of the engineering model compact transceiver is shown in Figure 4. Figure 5 shows a portion of the assembled modules with the module cover off.

The results of this R&D program has demonstrated reduced size and cost, improved performance, and more reliable circuits when designed as thick film modules.

DESCRIPTION OF RADIO FUNCTIONAL MODULES

- 1) Frequency Synthesizer - Of the 14 modules in the synthesizer, 11 were selected for hybridization. These 11 were thoroughly evaluated and redesigned both circuit-wise and mechanically, so that the circuit which was thick filmed also had reliability and performance superior to the module being replaced (Figure 6). Using today's semiconductor technology, the entire synthesizer is being replaced by three or four LSI chips under development at ITT-A/OD.
- 2) Power Modulator - The power modulator portion of the transceiver consists of the following thick film hybrid modules: 1) Audio Frequency (AF) Compressor and Preamplifier, 2) AF Filter Limiter, 3) Automatic Power Control, and 4) Transmit Receive Control.
- 3) Receiver Modules - The receiver was partitioned into nine modules. Four used standard IC's and five used hybrid circuits as shown in Figure 7.
- 4) Power and Driver Amplifier Modules - Figure 8 shows the initial thick film designs of the power and driver amplifier modules. The Pd-Ag conductor paste used in these circuits resulted in very low gain performance. Therefore, these two modules were replaced with microstrip designs having the required performance.

Resulting size and weight savings using thick film technology are listed in Table 2. Further size and weight reductions are anticipated in our current portable radio program due to component improvements with LSI technology.

TABLE 2. SIZE AND WEIGHT COMPARISON

Function	Size (IN ³)		Weight (Oz)	
	Conventional	Hybrid	Conventional	Hybrid
Driver Amplifier	37	7	32	10
RF Amplifier	13.5	2.5	10	2
Audio/Control Circuit	320	30	16	4
Frequency Synthesizer	105	28	80	16

STUDY OF MATERIALS FOR THICK FILM TECHNOLOGY

To control hybrid thick film processing and to achieve product reliability and producibility, a thorough understanding of the materials used and interactions among them during processing must be established. For this reason, an in-depth study of materials aspects of the thick film technology was conducted. The study was concerned with the compositions and structural aspects of commercial thick film pastes and substrates and their resulting components to establish reliable criteria for choosing commercial paste preparations and substrates. The work has enabled ITT-A/OD to anticipate material compatibility problems in thick film technology from resistor-conductor-substrate interactions to soldering and bonding problems as well as problems associated with chip mounting. In the case of resistor pastes, it is possible to indicate those compositions that are most promising for a given application and to avoid expensive statistical testing of basically unpromising compositions.

METHOD OF MATERIAL ANALYSIS

To identify the various components present in a particular thick film material (conductors, resistors, and alumina substrates) both before and after processing, a variety of analytical and evaluation techniques were used. These were:

- 1) Gas Chromatography,
- 2) Spectrographic Analysis,
- 3) Atomic Absorption Spectroscopy,
- 4) X-Ray Diffraction, and
- 5) Electron Probe Microanalysis and Scanning Electron Microscopy (SEM).

ANALYSIS OF RESISTOR PASTES

Four thick film resistor paste systems from three different manufacturers were analyzed. The results of the quantitative chemical analysis are shown in Table 3 below.

TABLE 3. QUANTITATIVE CHEMICAL ANALYSIS

Major Element (% Weight)	Paste System A	Paste System B	Paste System C	Paste System D
Silver (Ag)	21.8			
Palladium (Pd)	23.1			
Lead Oxide (PbO)	20.1	13.6	6.6	10.1
Lead Sulfate (PbSO ₄)	8.9		35.1	
Boron Oxide (B ₂ O ₃)	8.6	5.2	14.7	
Silicone Dioxide (SiO ₂)		6.4	7.7	
Bismuth Oxide (Bi ₂ O ₃)		43.0		
Ruthenium BiOxide (RuO ₂)		23.6	26.9	
Aluminum Oxide (Al ₂ O ₃)	0.05	3.3		
Gold (Au)			<0.05	0.01
Iridium Dioxide (IrO ₂)			Trace	24.6
Manganese (Mn)				3.44

Samples of fired resistors were analyzed by X-ray diffraction. The results are listed in Table 4.

TABLE 4. X-RAY DIFFRACTION ANALYSIS

Paste System A	Paste System B	Paste System C	Paste System D
Presence of PbO and PdAg	Diffraction pattern identical before and after firing.	Resistive pigment essentially unchanged, but the diffraction lines had disappeared and a new phase appeared.	Presence of Au and IrO ₂ .

The X-Ray Diffraction Analysis indicated that the earliest thick film systems were based on Pd-Ag-O (Paste System A) and sensitive to processing conditions, since the temperature and atmosphere of firing altered the ratio of PdAg to PdO to change the resistivity.

It is, therefore, not surprising to find that in the "second generation" resistor systems analyzed (Paste Systems B and C) manufacturers are using more stable conducting pigments. These are based mainly on ruthenium dioxide, but iridium dioxide is also used (Paste System D). To achieve a wide variety of sheet resistivities, other preformed ruthenates are used, (e.g., lead ruthenate, for a high resistivity). The need to add metal pigments to achieve low sheet resistivity in ruthenium dioxide based pastes was observed. The success of using RuO_2 and bismuth ruthenate to control sheet resistivity compared with other systems was also established.

The evaluation using SEM with energy analysis attachment discovered that in both Paste System A and B there was some interaction between the conducting phase and the glass such that particles which were apparently separated still had a conducting path.

ANALYSIS OF ALUMINA SUBSTRATES

The compositions of alumina substrates were determined by atomic absorption spectroscopy, giving the percentage Al_2O_3 present plus the main fluxing constituents usually a mixture of SiO_2 and MgO or CaO . The surface finish and microstructure were examined by both optical and scanning electron microscopes. Results are shown in Table 5.

TABLE 5.

	Vendor A	Vendor B	(% Weight)		
			Vendor C	Vendor D	Vendor E
Aluminum Oxide (Al_2O_3)	94.3	96.7	96.45	95.10	95.4
Silicon Dioxide (SiO_2)	3.01	0.96	1.78	2.33	2.2
Ferric Oxide (Fe_2O_3)	0.08	0.09	0.07	0.05	0.092
Titanium Dioxide (TiO_2)	0.03	0.003	0.017	0.005	0.069
Sodium Oxide (Na_2O)	0.07	0.004	0.06	0.03	0.097
Potassium Oxide (K_2O)	<0.01	<0.01	<0.01	<0.01	0.0136
Calcium Oxide (CaO)	0.22	0.48	1.16	<0.01	1.91
Magnesium Oxide (MgO)	2.26	1.83	0.10	1.94	0.018

The chemical analysis results in the table on this page show that for the materials supplied by the five different manufacturers, alumina contents were between 94.3 and 96.7 percent. But it is the composition of the remaining few percent in which the essential differences lie. It is important to note that it is these fluxes on which the adhesion of a thick film composition is primarily based.

EFFECT OF SUBSTRATE ON RESISTIVITY

The effect of the substrate on the resistivity of resistor pastes has found to be significant only on high resistivity pastes. (Table 6).

TABLE 6. EFFECT OF SUBSTRATE ON FIRED RESISTIVITY

Vendor B Paste Ω /Square	Bulk Resistivity, Ω /Square Substrate Vendors		
	A	B	C
10	21.3	20.3	21.5
10^2	167.5	162.5	170.0
10^4	173,000	148,000	17,300
10^6	3,200,000	3,100,000	5,100,000

From the chemical analysis, the important major and minor constituents have been identified, X-ray diffraction techniques provided information on the crystalline components, which are usually the conducting particles in the resistor, and, by comparing the patterns produced before and after firing, showed what chemical reactions may have occurred during firing.

Scanning electron microscopy combined with electron probe microanalysis has also been found to be a very powerful technique in the analytical investigation, although it will not be discussed in detail here.

In summary, the combination of analytical and evaluation techniques provided a powerful means of identifying the composition and detail of thick film materials. The methods outlined above provide the comprehensive picture of thick film resistors and substrates which is necessary to understand the conduction mechanisms involved.

COST ANALYSIS

Although light weight, small size, high reliability are extremely important, these requirements must always be considered in relation to achieving a low cost radio product.

The cost of circuits using conventional assembly techniques is compared to thick film modules in Table 7.

TABLE 7. A COMPARISON OF APPROXIMATE COSTS

Module Function	Conventional Discrete Form (\$)	Thick Film Hybrid Form (\$)
Frequency Synthesizer	1,100	700
Power Amplifier	600	400
Driver Amplifier	165	90
Audio Modulator (Transmitter)	170	100
RF Amplifier	90	50
Audio Modulator (Receiver)	75	95
Noise Limiter	110	98
IF Amplifier	100	50
UHF Mixer	90	50

In Table 8 there is a cost comparison of hybrid microcircuits from different sources.

TABLE 8. PROCUREMENT COST TABULATION

	<u>1" X 1"</u>	<u>1" X 2"</u>	<u>1" X 3"</u>	<u>Average</u>
Source A	\$91	\$205	\$182	\$151
Source B	34	114	72	73
Source C	46	209	74	110
Source D	23	70	96	63
Average	49	150	106	99

Total non-recurring costs quoted by four sources on these modules were \$34,000, \$36,000, \$67,000 and \$66,000 for 29 module types.

The three specific hybrid thick film modules used in the cost modules were selected as representative of a 1" X 1" simple family of modules, a 1" X 2" nominal complexity family of modules and a 1" X 3" complex family of modules. The system usage and circuit complexity are listed below:

<u>Substrate Size</u>	<u>System Usage</u>	<u>Components (Capacitors/Inductors/IC's)</u>
1" X 1"	13	12-25
1" X 2"	12	25-36
1" X 3"	4	36-50
Total	29	Substrate/System

For simplicity, the cost analysis of the three sample modules referenced above were made for a quantity of 5,000 each to match a price break point.

The wide price range variation shown in Table 8 confirms that applied microelectronics for military product application is not yet mature. Manufacturing processes have not yet stabilized in the industry.

The cost tables were the result of extensive studies, conducted by joint engineering and manufacturing staff, verified the cost effectiveness of thick film hybrid techniques.

CONCLUSIONS

Hybrid thick film technology was shown to be an effective means of integrating an entire radio system. It provides the advantages of high performance, small size, and low cost. It employs portions of semiconductor technology (either LSI chips or individually optimized transistor chips in unpackaged chip form), adds economy, and provides increased packaged density.

A thorough understanding of thick film materials and their interaction during processing was shown to be necessary for the successful application of the thick film technology. Various methods of material analysis and evaluation have been devised to ensure circuit reliability and reproducibility.

ITT-A/OD will also use its LSI System Support Center (LSSC) to provide expertise and experience in the latest LSI techniques and technologies. At the start of current development programs, applications engineers from the center are working with radio design engineers to assist in a systems partitioning study and analysis of potential LSI applications.

ACKNOWLEDGEMENTS

Appreciation is extended to the Materials and Components Group, Standard Telecommunication Laboratories, Harlow, England, for the outstanding support provided in the study of thick film materials.

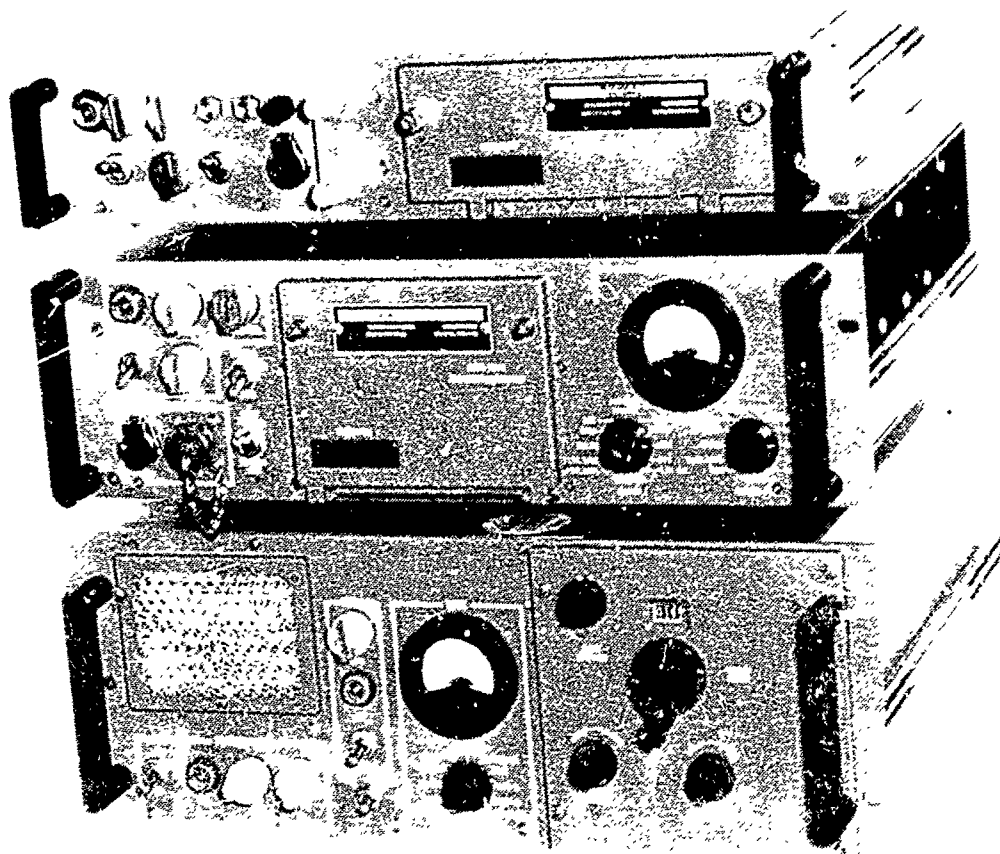


FIGURE 1. JUMP COMMUNICATIONS RADIOS

CONCLUSIONS

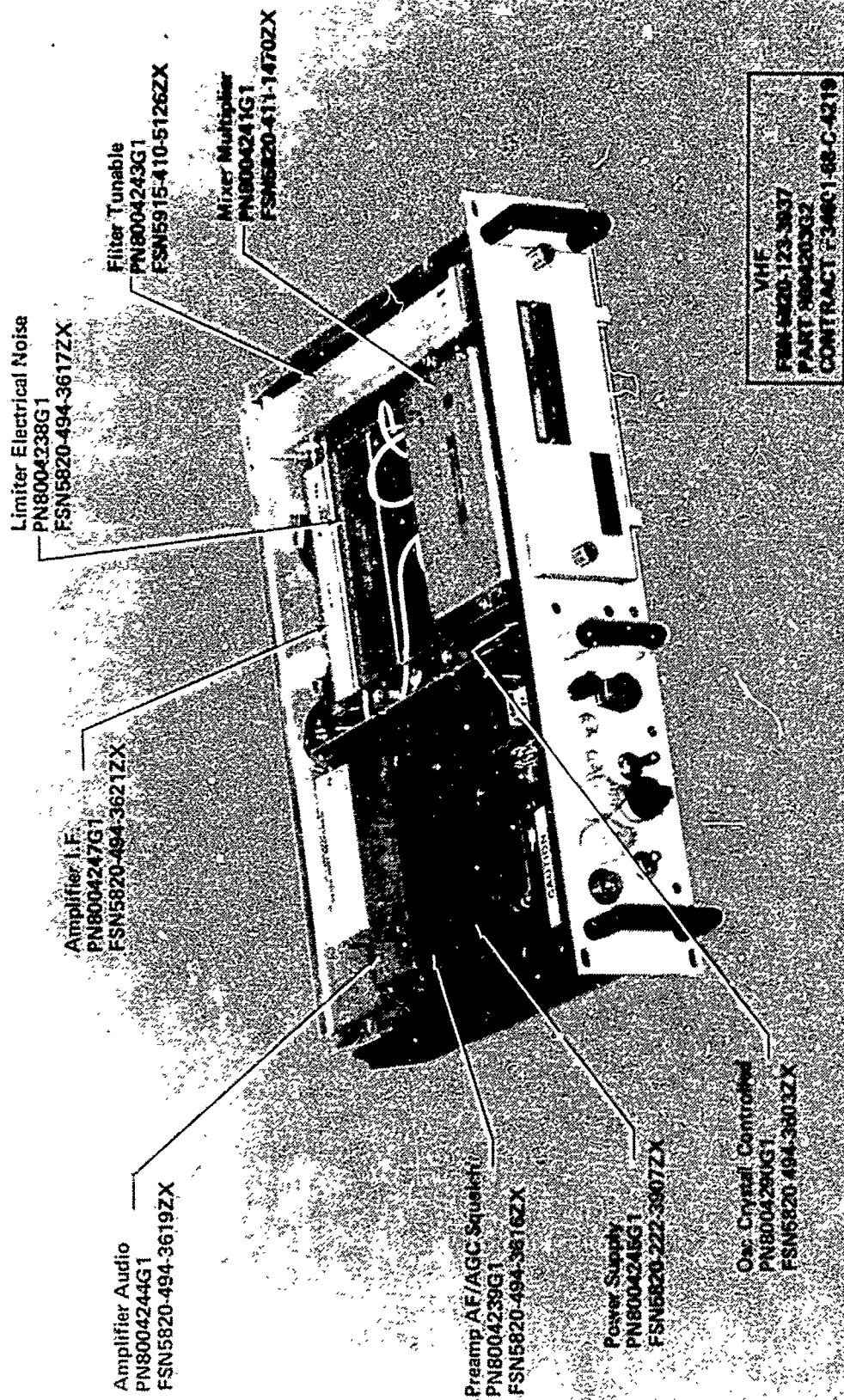
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RECEIVER RADIO AN/GRR 25

FIGURE 2. MODULAR CONSTRUCTION OF JUMP COMMUNICATIONS RADIO

AEROSPACE OPTICAL DIVISION
ELECTRO-OPTICAL OPERATIONS
2500 C. PORTAC BLVD., FORT WAYNE, IND. 46823

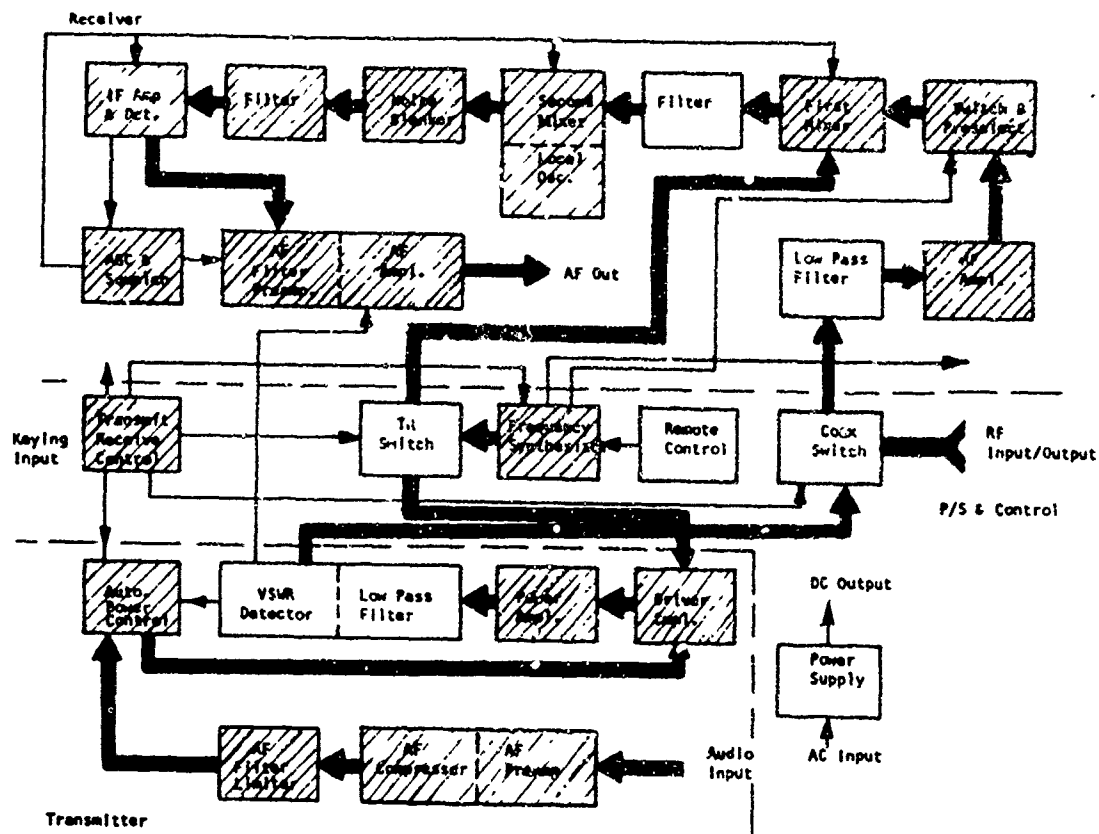


Figure 3. Transceiver Block Diagram

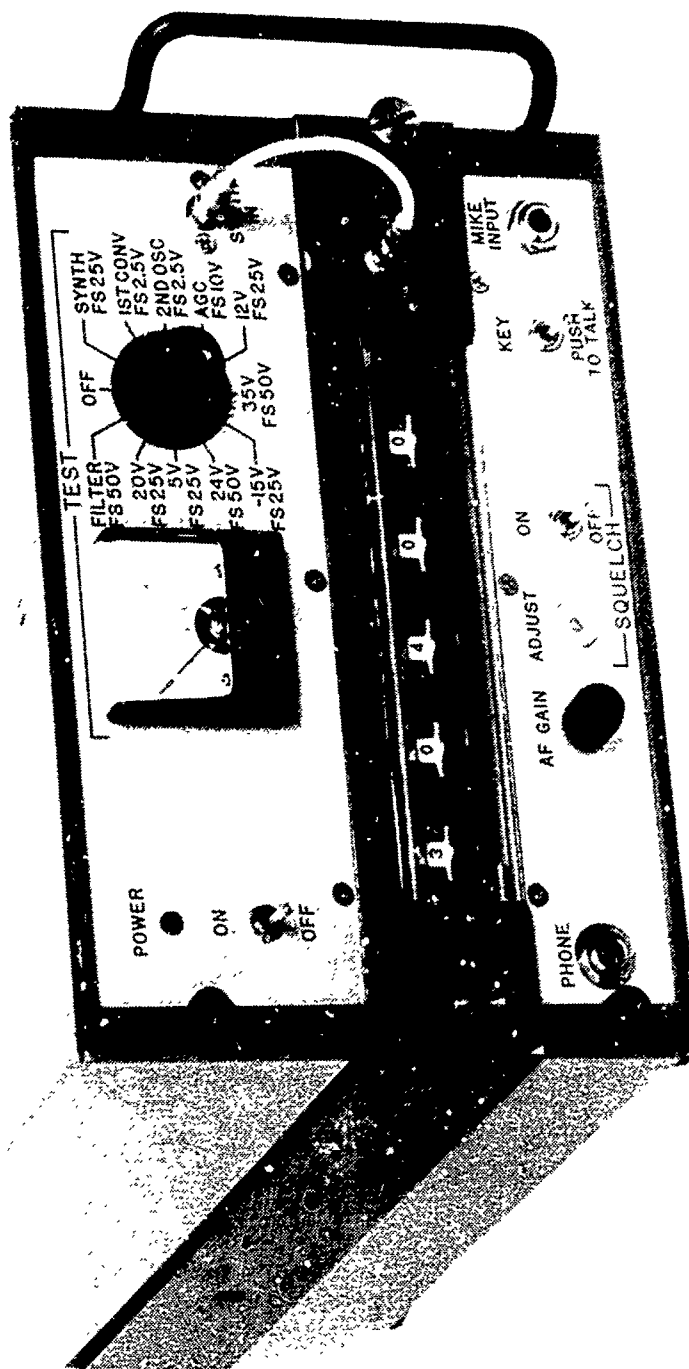


FIGURE 4.
ENGINEERING MODEL MICROELECTRONIC TRANSCEIVER

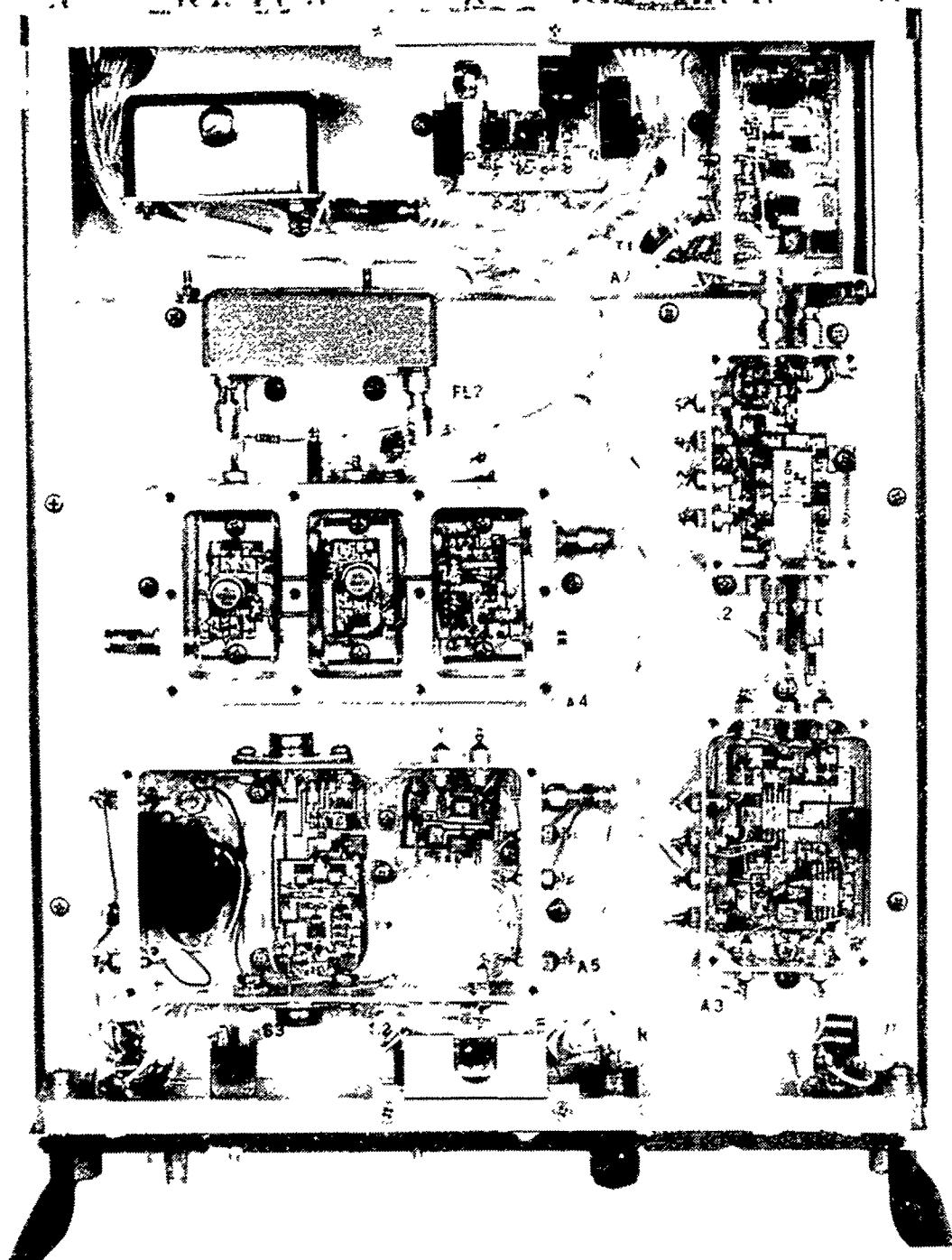


FIGURE 5.

MICROELECTRONIC TRANSCEIVER

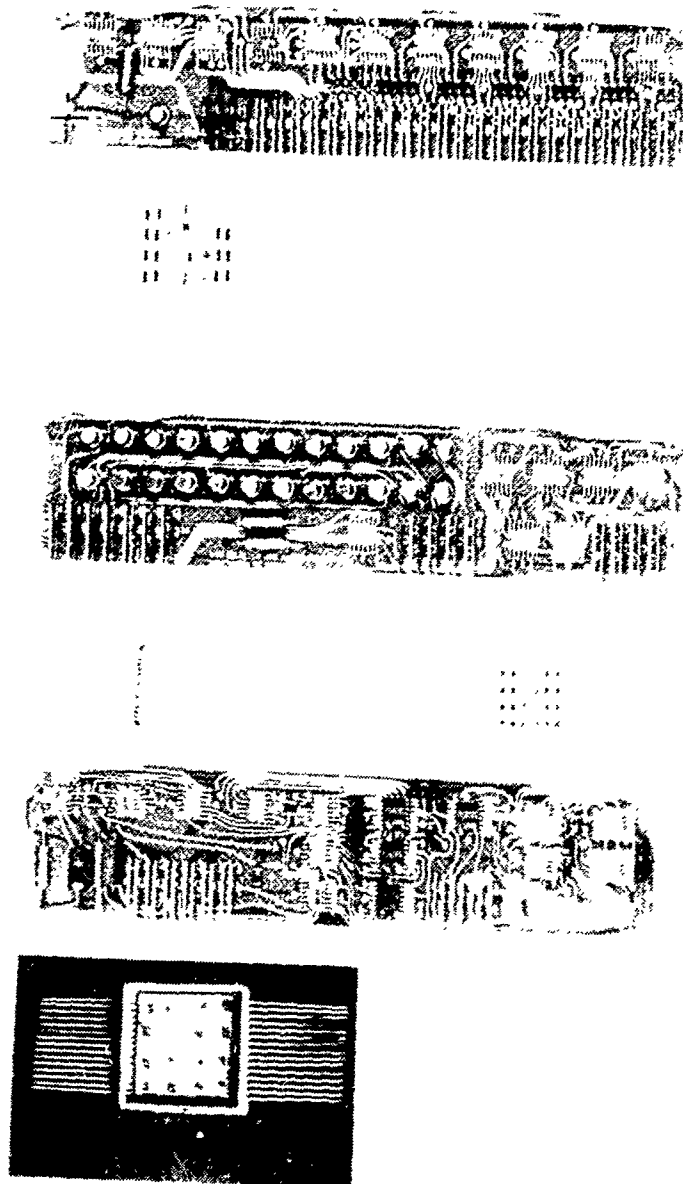


FIGURE 6.
SYNTHESIZER HYBRID MODULES

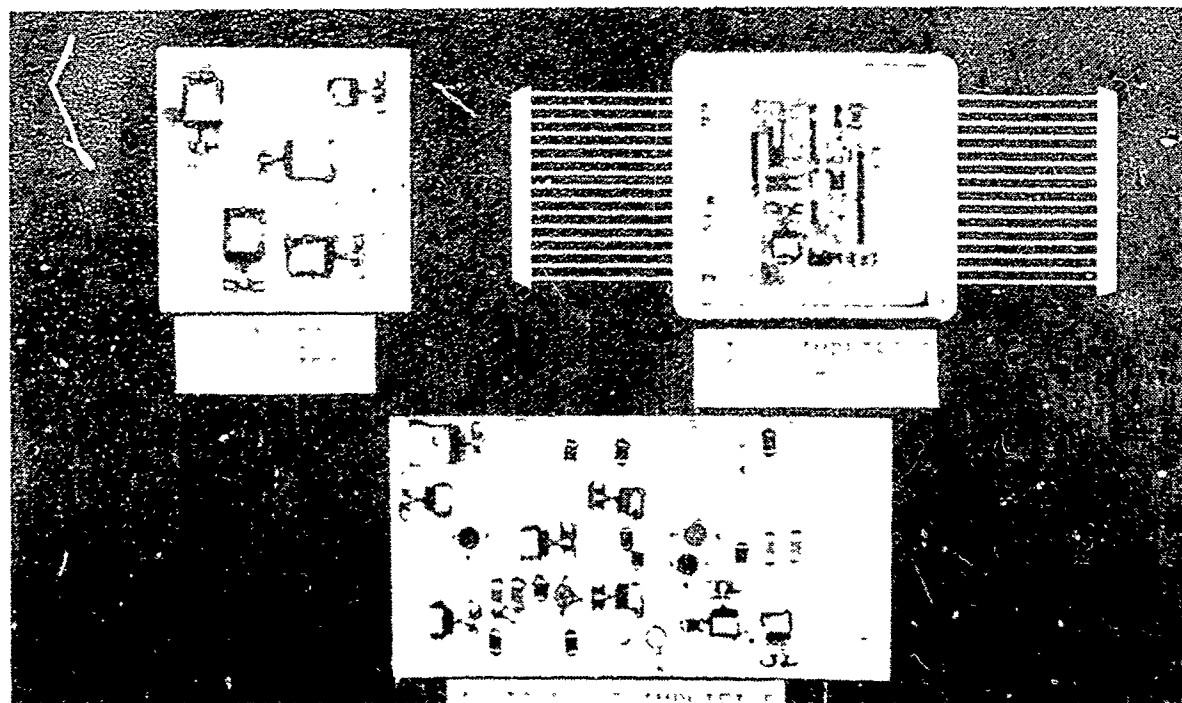
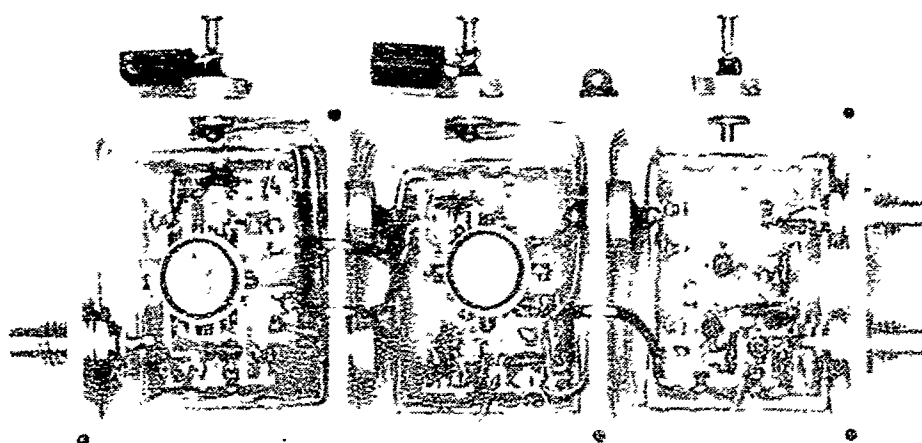
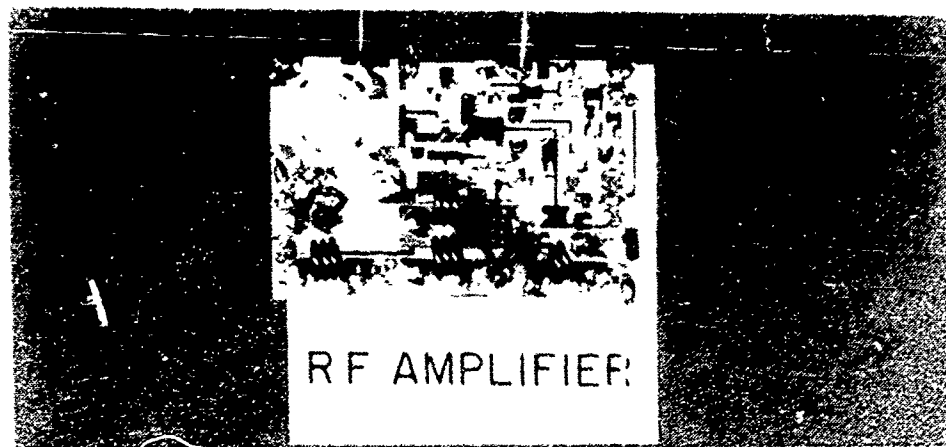


FIGURE 7. RECEIVER HYBRID MODULES

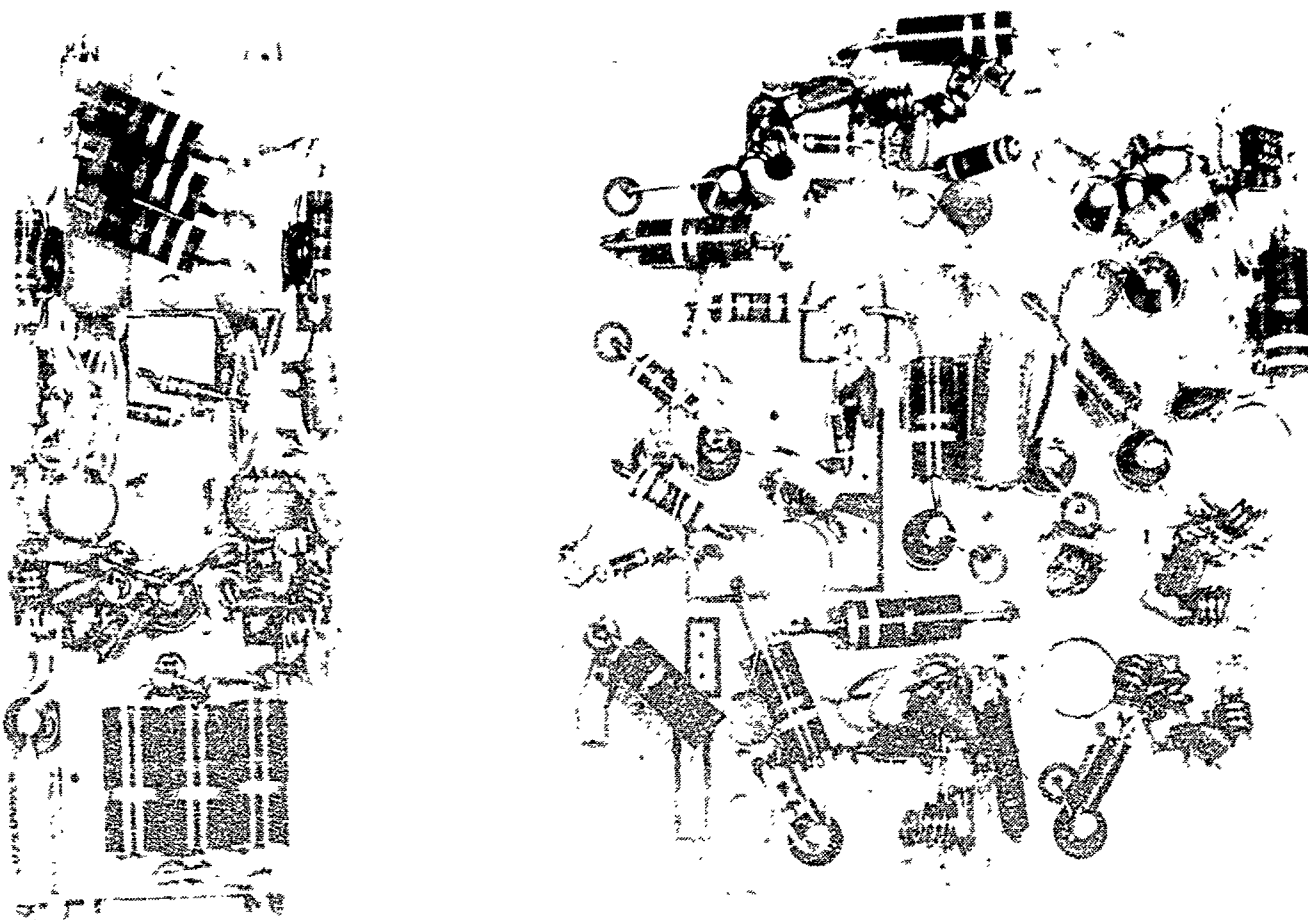


FIGURE 8.
POWER AND DRIVER AMPLIFIER MODULES